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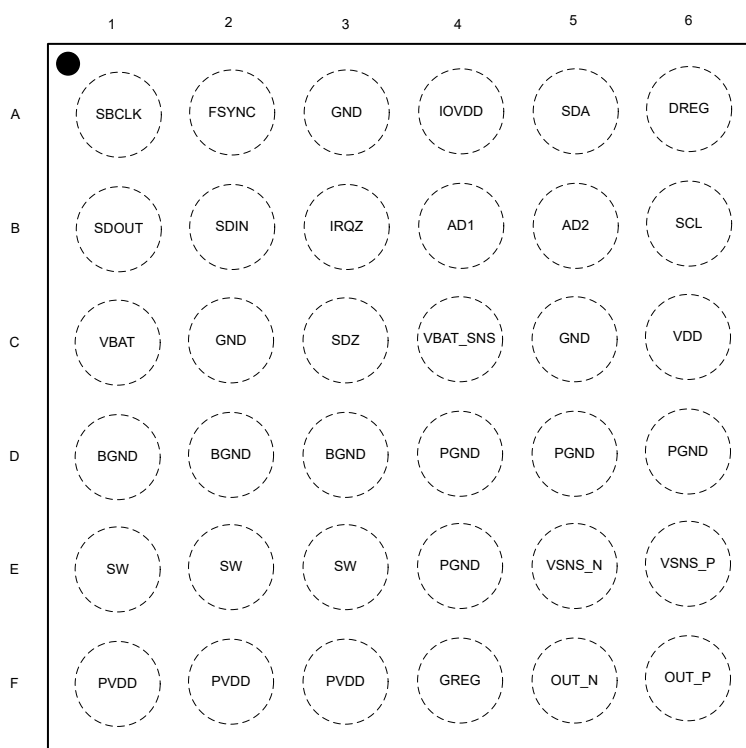
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE      | REVISION | NOTES           |
|-----------|----------|-----------------|
| Nov, 2022 | v0.1     | Initial Release |

## 5 Pin Configuration and Functions



Notes: - Not to Scale

**Figure 5-1. Package Top Level View Pinout**

### Pin Functions

| PIN      |     | I/O <sup>1</sup> | DESCRIPTION                                                                                                                                    |
|----------|-----|------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME     | NO. |                  |                                                                                                                                                |
| AD1      | B4  | I                | I <sup>2</sup> C address pin LSB.                                                                                                              |
| AD2      | B5  | I                | I <sup>2</sup> C address pin LSB+1.                                                                                                            |
| BGND     | D1  | P                | Boost ground. Connect to PCB GND plane strongly with multiple vias.                                                                            |
|          | D2  |                  |                                                                                                                                                |
|          | D3  |                  |                                                                                                                                                |
| DREG     | A6  | P                | Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to external load.                                        |
| FSYNC    | A2  | I                | I <sup>2</sup> S word clock or TDM frame sync.                                                                                                 |
| GREG     | F4  | P                | High-side gate CP regulator output. Do not connect to external load.                                                                           |
| GND      | A3  | P                | Digital ground. Connect to PCB GND plane. Strong connection to ground plane required through multiple vias.                                    |
|          | C2  |                  |                                                                                                                                                |
|          | C5  |                  |                                                                                                                                                |
| IOVDD    | A4  | P                | 1.2-V or 1.8-V Digital IO supply. Decouple to GND with capacitor.                                                                              |
| IRQZ     | B3  | O                | Open drain, active low interrupt pin. Pull up to IOVDD with resistor if optional internal pullup is not used.                                  |
| OUT_N    | F5  | O                | Class-D negative output.                                                                                                                       |
| OUT_P    | F6  | O                | Class-D positive output.                                                                                                                       |
| PGND     | D4  | P                | Class-D Power stage ground. Connect to PCB GND plane strongly through multiple vias.                                                           |
|          | D5  |                  |                                                                                                                                                |
|          | D6  |                  |                                                                                                                                                |
|          | E4  |                  |                                                                                                                                                |
| PVDD     | F1  | P                | Integrated boost output and Class-D power stage supply.                                                                                        |
|          | F2  |                  |                                                                                                                                                |
|          | F3  |                  |                                                                                                                                                |
| SBCLK    | A1  | I                | I <sup>2</sup> S/TDM serial bit clock.                                                                                                         |
| SCL      | B6  | I                | I <sup>2</sup> C Clock Pin. Pull up to IOVDD with a resistor.                                                                                  |
| SDA      | A5  | IO               | I <sup>2</sup> C Data Pin. Pull up to IOVDD with a resistor.                                                                                   |
| SDIN     | B2  | I                | I <sup>2</sup> S or TDM serial data input.                                                                                                     |
| SDOUT    | B1  | IO               | I <sup>2</sup> S or TDM serial data output.                                                                                                    |
| SDZ      | C3  | I                | Active low hardware shutdown.                                                                                                                  |
| SW       | E1  | P                | Boost converter switch input.                                                                                                                  |
|          | E2  |                  |                                                                                                                                                |
|          | E3  |                  |                                                                                                                                                |
| VBAT     | C1  | P                | Battery power supply input. Connect to 2.5-V to 5.5-V supply and decouple with a cap.                                                          |
| VBAT_SNS | C4  | I                | Battery sense terminal. Connect to 1S or 2S battery supply for remote battery sensing. Ground the pin if remote sensing is not used.           |
| VDD      | C6  | P                | Analog, digital power supply. Connect to 1.8-V supply and decouple to GND with cap.                                                            |
| VSNS_N   | E5  | I                | Voltage sense negative input. Connect to speaker negative terminal as close to speaker as possible. Add series resistor if EMI filter is used. |
| VSNS_P   | E6  | I                | Voltage sense positive input. Connect to speaker positive terminal as close to speaker as possible. Add series resistor if EMI filter is used. |

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| PTAS2572YCGR     | ACTIVE        | DSBGA        | YCG                | 36   | 3000           | TBD             | Call TI                              | Call TI              | -40 to 85    |                         | <a href="#">Samples</a> |
| TAS2572YCGR      | ACTIVE        | DSBGA        | YCG                | 36   | 3000           | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | TAS257X                 | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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