SN65HVD10x IO-Link PHY for Device Nodes

1 Features

- Configurable CQ Output: Push-Pull, High-Side, or Low-Side for SIO Mode
- Remote Wake-Up Indicator
- Current Limit Indicator
- Power-Good Indicator
- Overtemperature Protection
- Reverse Polarity Protection
- Configurable Current Limits
- 9-V to 36-V Supply Range
- Tolerant to 50-V Peak Line Voltage
- 3.3-V/5-V Configurable Integrated LDO (SN65HVD101 ONLY)
- 20-pin QFN Package, 4 mm × 3.5 mm

2 Applications

- Suitable for IO-Link Device Nodes

3 Description

The SN65HVD101 and 'HVD102 IO-Link PHYs implement the IO-Link interface for industrial point-to-point communication. When the device is connected to an IO-Link master through a 3-wire interface, the master can initiate communication and exchange data with the remote node while the SN65HVD10X acts as a complete physical layer for the communication.

The IO-Link driver output (CQ) can be used in push-pull, high-side, or low-side configurations using the EN and TX input pins. The PHY receiver converts the 24-V IO-Link signal on the CQ pin to standard logic levels on the RX pin. A simple parallel interface is used to receive and transmit data and status information between the PHY and the local controller.

The SN65HVD101 and 'HVD102 implement protection features for overcurrent, overvoltage and overtemperature conditions. The IO-Link driver current limit can be set using an external resistor. If a short-circuit current fault occurs, the driver outputs are internally limited, and the PHY generates an error signal (SC). These devices also implement an overtemperature shutdown feature that protects the device from high-temperature faults.

The SN65HVD102 operates from a single external 3.3-V or 5-V local supply. The SN65HVD101 integrates a linear regulator that generates either 3.3 V or 5 V from the IO-Link L+ voltage for supplying power to the PHY as well as a local controller and additional circuits.

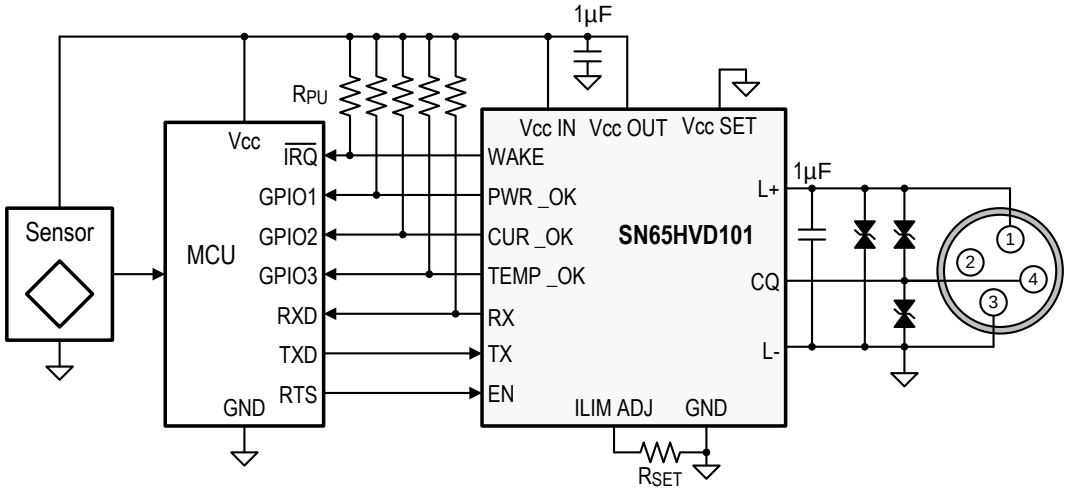
The SN65HVD101 and 'HVD102 are available in the 20-pin RGB package (4 mm × 3,5 mm QFN) for space-constrained applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD101	QFN (20)	4.00 mm × 3.50 mm
SN65HVD102		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2017) to Revision D — **Page**

- Changed From: 950 mW To: 950 W, and From: 475 mW To: 475 W in the *TVS Evaluation* section ... 16

Changes from Revision B (April 2015) to Revision C — **Page**

- Changed pin 1 of the SN65HVD102 From: nc To: Vcc SET ... 3

Changes from Revision A (March 2013) to Revision B — **Page**

- Added *Device Information* and *ESD Rating* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed front-page Simplified Schematic image. ... 1
- Changed Pin Functions table format ... 4
- Re-write detailed description section. ... 9
- Re-write application information section. ... 14

Changes from Original (May 2011) to Revision A — **Page**

- Changed the devices From: Product Preview To: Production ... 1

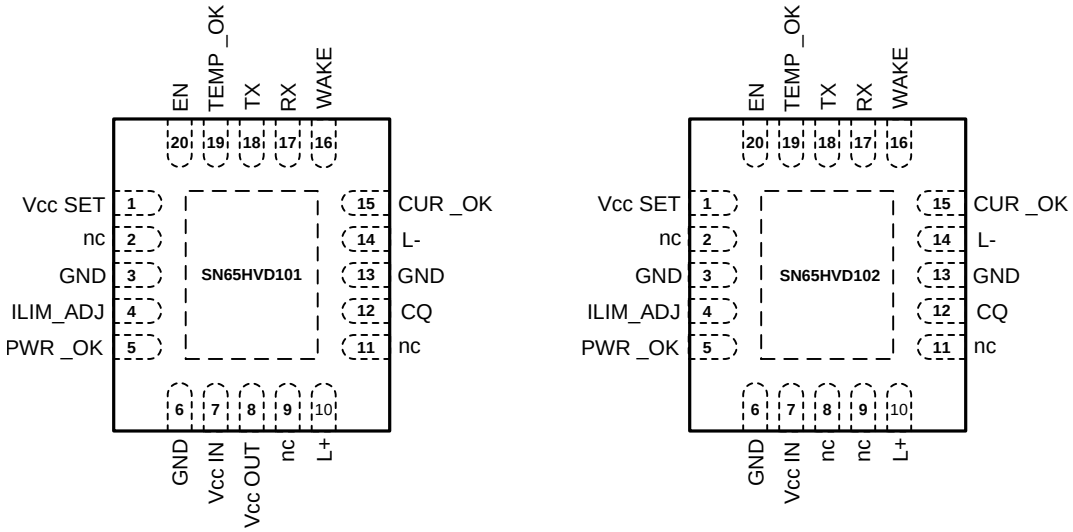
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5 Device Comparison Table

DEVICE	VOLTAGE REGULATOR
SN65HVD101	Yes
SN65HVD102	No

6 Pin Configuration and Functions

RGB Package
20-Pin QFN with Thermal Pad
Top View



Pin Functions

PIN			DESCRIPTION
NAME	NUMBER	TYPE(1)	
IO-Link Interface			
L+	10	P	IO-Link supply voltage (24V nominal)
CQ	12	I/O	IO-Link data signal (bi-directional)
L–	14	P	IO-Link ground (connect to board ground)
Local Controller Interface			
CUR_OK	15	OD	High-CQ-current fault indicator output signal from PHY to the microcontroller. Connect this pin via pull-up resistor to Vcc OUT. A LOW level indicates over-current condition.
WAKE	16	OD	Wake up indicator from the PHY to the local controller Connect this pin via pull-up resistor to Vcc OUT.
RX	17	O	PHY receive data output to the local controller
TX	18	I	PHY transmit data input from the local controller
EN	20	I	Driver enable input signal from the local controller
Power Supply Pins			
V_{CC} IN	7	A	Voltage supply input for SN65HVD102 Voltage sense feedback input for the voltage regulator of the SN65HVD101. Connect this pin to pin 8 either directly or through a current boost transistor.
V_{CC} OUT	8	P	Not connected in SN65HVD102 Linear regulator output of SN65HVD101. Connect this pin to pin 7 either directly or through a current boost transistor.
GND	3, 6, 13	P	Logic ground potential

(1) Type definitions: I = Input, I/O = Input/Output, A = Analog, O - CMOS Output, OD = Open Drain Output, P = Power

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Pin Functions (continued)

PIN			DESCRIPTION
NAME	NUMBER	TYPE(1)	
Special Connect Pins			
V_{CC} SET	1	I	Connect this pin to ground to make Vcc OUT = 3.3V. Leave this pin floating to make Vcc OUT = 5V.
ILIMADJ	4	A	Input for current limit adjustment. Connect resistor RSET between this pin and ground. For R_{SET} values see Figure 2.
PWR_OK	5	OD	Power-Good indicator. Connect this pin via pull-up resistor to Vcc OUT. A HIGH at this pin indicates that L+ and Vcc OUT are at correct levels.
Temp_OK	19	OD	Temperature-Good indicator. Connect this pin via pull-up resistor to Vcc OUT. High-impedance at this pin indicates that the internal temperature is at a safe level. A low at this pin indicates the device is approaching thermal shutdown.
NC	2, 9, 11	–	No Connection. Leave these pins floating (open)

In normal operation, the PHY sets the output state of the CQ pin when the driver is enabled. During fault conditions, the driver may be disabled by internal circuits.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Line voltage	L+, CQ	Steady state	–40	40 (2) (3)	V
		Transient pulse width <100 µs	–50	50	V
Voltage difference	|VL+ – VCQ|			40	
Supply voltage	V_{CC}		–0.3	6	V
Input voltage	TX, EN, V_{CC}_SET, ILIMADJ,		–0.3	6	V
Output voltage	RX, CUR_OK, WAKE, PWR_OK		–0.3	6	V
Output current	RX, CUR_OK, WAKE, PWR_OK		–5	5	mA
Storage temperature, T_{stg}			–65	150	°C
Junction temperature, T_J				180	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with reference to the GND pin, unless otherwise specified.
(3) GND pin and L– line should be at the same DC potential

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM, all pins), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{L+}	Line voltage(1)		9	24	30	V
V_{CC}	Logic supply voltage (3.3V nominal)		3	3.3	3.6	V
V_{CC}	Logic supply voltage (5V nominal)		4.5	5	5.5	V
V_{IL}	Logic low input voltage				0.8	V
V_{IH}	Logic high input voltage		2			V
I_O	Logic output current		–4		4	mA
$I_{CC(OUT)}$	Logic supply current (HVD101)				20	mA
$I_{O(LIM)}$	CQ driver output current limit		100		450	mA
R_{SET}	External resistor for CQ current limit		0		20	kΩ
C_{COMP}	Compensation capacitor for voltage regulator (HVD101)		3.3			µF
$1/t_{BIT}$	Signaling rate	IO-Link mode			250	kbps
		SIO mode			10	
T_A	Ambient temperature		–40		105	°C
T_J	Junction temperature		–40		150	°C

(1) These devices will operate with line voltage as low as 9V and as high as 36V, however, the parametric performance is optimized for the IO-Link specified supply voltage range of 18V to 30V.

7.4 Thermal Information

THERMAL METRIC(1)		SN65HVD10x RGB 20 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	10.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	10.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

over all operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver								
I_{IN}	Input current (TX, EN)		VIN = 0V to V_{CC}		–100		100	µA
V_{RQH}	Residual voltage across the driver high side switch		ICQ = –250 mA	18 < V_{L+}	1.5		3	V
				V_{L+} < 18			3.5	V
			ICQ = –200 mA	18 < V_{L+}			2	V
				V_{L+} < 18			2.5	V
V_{RQL}	Residual voltage across the driver low side switch		ICQ = 250 mA	18 < V_{L+}	1.5		3	V
				V_{L+} < 18			3.5	V
			ICQ = 200 mA	18 < V_{L+}			2	V
				V_{L+} < 18			2.5	V
$\lvert I_{O(LIM)} \rvert$	Driver output current limit		R_{SET} = 20 kΩ		60	95	130	mA
			R_{SET} = 0 kΩ		300	400	480	mA
$I_{(OZ)}$	CQ leakage current with EN = L		VCQ = 8 V		–2		2	µA
Receiver								
V_{THH}	Input threshold “H”		18 V < V_{L+} < 30 V		10.5		13	V
V_{THL}	Input threshold “L”				8		11.5	V
V_{HYS}	Receiver Hysteresis (V_{THH} – V_{THL})				0.5	1		V
V_{THH}	Input threshold “H”		9 V < V_{L+} < 18 V		Note (1)		Note (2)	V
V_{THL}	Input threshold “L”				Note (3)		Note (4)	V
V_{HYS}	Receiver Hysteresis (V_{THH}–V_{THL})				0.25			V
V_{OL}	Output low voltage	RX	I_{OL} = 4 mA				0.4	V
		OD outputs	I_{OL} = 1 mA				0.4	
V_{OH}	Output high voltage	RX	I_{OH} = –4 mA		V_{CC}–0.5			V
I_{OZ}	Output leakage current	OD outputs	Output in Z state, V_O = V_{CC}			0.03	1	µA
Protection Thresholds								
V_{PG1}	V_{L+} threshold for PWR_OK				8		10	V
V_{PG2}	V_{CC} threshold for PWR_OK		V_{CC} Set = GND		2.45	2.75	3	V
			V_{CC} Set = OPEN		3.9	4.25	4.6	
V_{POR1}	Power-on Reset for V_{L+}					6		V
V_{POR2}	Power-on Reset for V_{CC}					2.5		V
Voltage Regulator (HVD101)								
V_{CC_OUT}	Voltage regulator output		9 V < V_{L+} < 30 V	V_{CC} SET = OPEN	4.5	5	5.5	V
				V_{CC} SET = GND	3	3.3	3.6	
V_{DROP}	Voltage regulator drop-out voltage (V_{L+} – V_{CC_OUT})		I_{CC} = 20 mA load current			3.2	3.9	V
	Line regulation (dV_{CC_OUT} /dL+)		9 V < V_{L+} < 30 V, I_{VCC} = 1 mA			4		mV/V
	Load regulation (dV_{CC_OUT} /V_{CC_OUT})		V_{L+} = 24 V, I_{VCC} = 100 µA to 20 mA			1.3%	5%	
PSRR	Power Supply Rejection Ratio		100 kHz, I_{VCC} = 20 mA		30	40		dB
Supply Current								
I_{L+}	Quiescent supply current		Driver disabled, No Load	HVD102		1	2	mA
				HVD101		1.3	3	
	Dynamic supply current			HVD102		2		
				HVD101		1.5		

(1) V_{THH}(min) = 5V + (11/18)[V_{L+} - 9V]
(2) V_{THH}(max) = 6.5V + (13/18)[V_{L+} - 9V]
(3) V_{THL}(min) = 4V + (8/18)[V_{L+} -9V]
(4) V_{THL}(max) = 6V + (11/18)[V_{L+} -9V]

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7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_{PLH}, t_{PHL}	Driver propagation delay	TX to CQ	Figure 1, Figure 2, Figure 3, R_L= 2kΩ, C_L = 5 nF, R_{SET} = 0 Ω		1	2	µs
$t_{P(skew)}$	Driver propagation delay skew				0.2		µs
t_{PZH}, t_{PZL}	Driver enable delay (EN to CQ)	18 V < V_{L+} < 30 V				5	µs
		9 V < V_{L+} < 18 V				8	
t_{PHZ}, t_{PLZ}	Driver disable delay	18 V < V_{L+} < 30 V				5	µs
		V_{L+} < 18 V				8	
t_r, t_f	Driver output rise, tall time	18 V < V_{L+}				869	ns
$\|t_r - t_f\|$	Difference in rise and fall time					300	
Receiver							
t_{WU1}	Wake-up recognition begin	Figure 16		45	60	75	µs
t_{WU2}	Wake-up recognition end			85	100	135	
t_{pWAKE}	Wake-up output delay					155	
t_{ND}	Noise suppression time(1)					250	ns
t_{PR}	Receiver propagation delay	Figure 4	18 V < V_{L+}		300	600	ns
			V_{L+} < 18 V			800	
Protection Thresholds							
T_{SD}	Shutdown temperature	Die temperature		160	175	190	°C
T_{RE}	Re-enable temperature(2)			110	125	140	
	Thermal warning temperature (TEMP_OK)			120	135	150	
t_{pSC}	Current limit indicator delay			85		175	µs

(1) Noise suppression time is defined as the permissible duration of a receive signal above/below the detection threshold without detection taking place.
(2) T_{RE} is always less than T_{WARN} so TEMP_OK is de-asserted (high impedance) when the device is re-enabled.

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7.7 Typical Characteristics

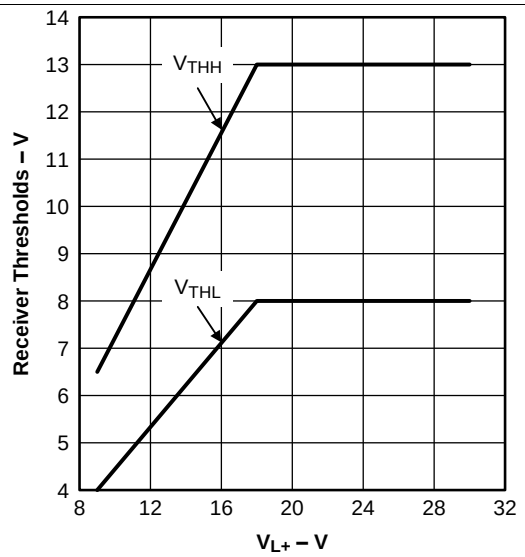


Figure 1. Receiver Threshold Boundaries

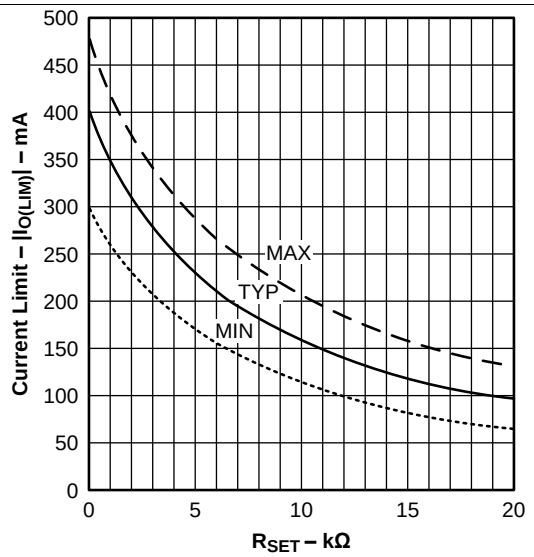


Figure 2. Typical Current Limit Characteristics

8 Parameter Measurement

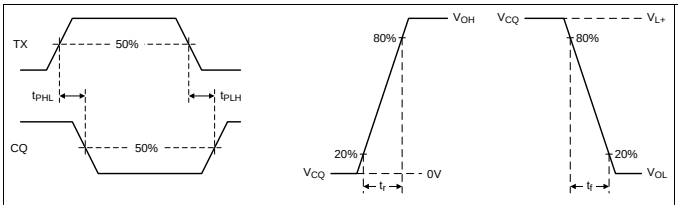


Figure 3. Waveforms for Driver Output Switching Measurements

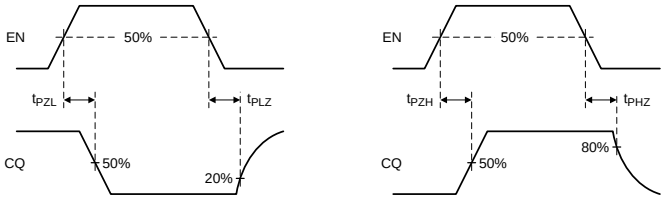


Figure 4. Waveform for Driver Enable/Disable Time Measurements

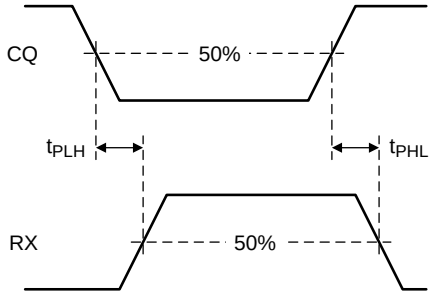
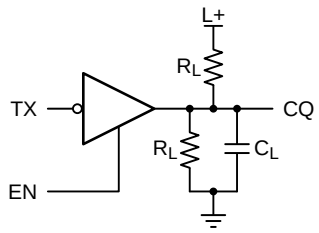


Figure 5. Receiver Switching Measurements



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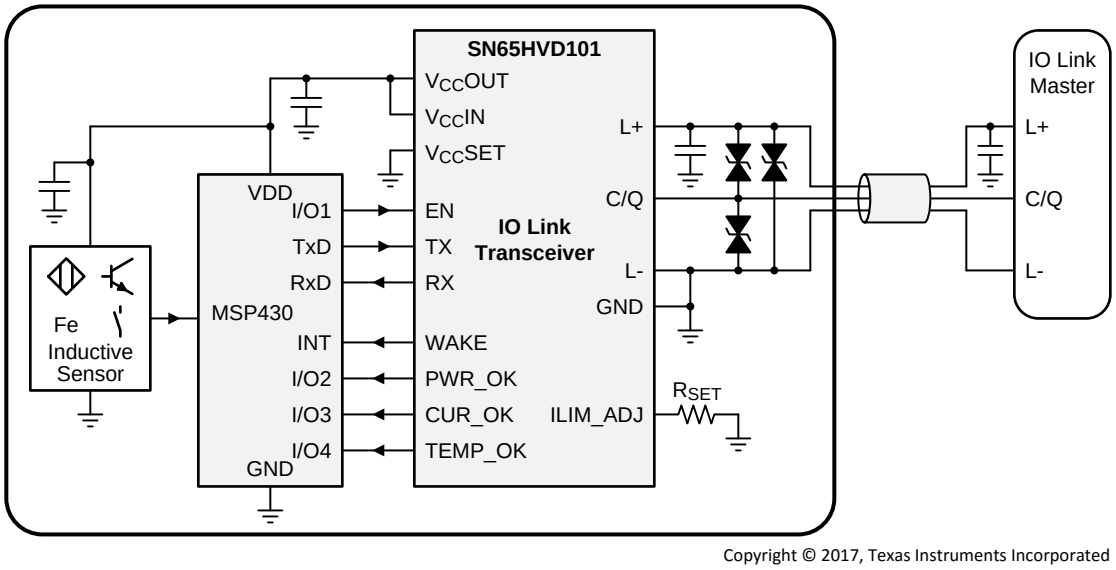
Figure 6. Test Circuit for Driver Switching

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9 Detailed Description

9.1 Overview

An IO-Link device comprises a transducer or physics to digital converter and the device transceiver (Figure 7). When the device is connected to an IO-Link master through the three-wire interface, the master can initiate communication and exchange data with a remote node with the SN65HVD101 or SN65HVD102 IO-Link transceiver acting as a complete physical layer for the communication.



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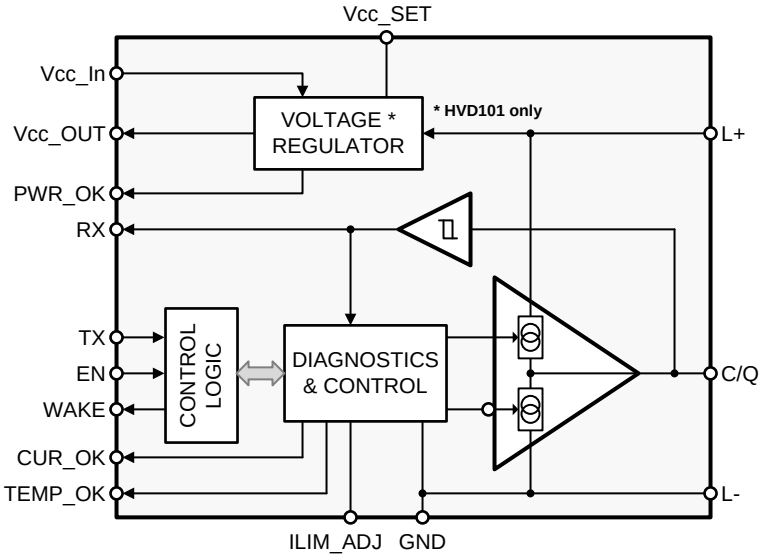
Figure 7. IO-Link Device-to-Master Interface

The functional block diagram shows that the device driver output (CQ) can be used in push-pull, high-side, or low-side configurations using the enable (EN) and transmit data (TX) input pins. The internal receiver converts the 24-V IO-Link signal on the CQ line to standard logic levels on the receive data (RX) pin. A simple parallel interface is used to receive and transmit data and status information between the slave and the local controller.

IO-Link transceivers commonly implement protection features for overcurrent, overvoltage and overtemperature conditions. They also provide a current-limit setting of the driver output current using an external resistor. If a short circuit (SC) occurs, the driver outputs are internally limited, and the slave generates an error signal.

The transceiver also possesses an overtemperature shutdown feature that protects the device from high-temperature faults. A modern transceiver can operate either from an external 3.3-V or 5-V low-volt supply, or derives the low-volt supply from the IO-Link L+ voltage (24V nominal) via a linear regulator, to provide power to the local controller and sensor circuitry.

9.2 Functional Block Diagram



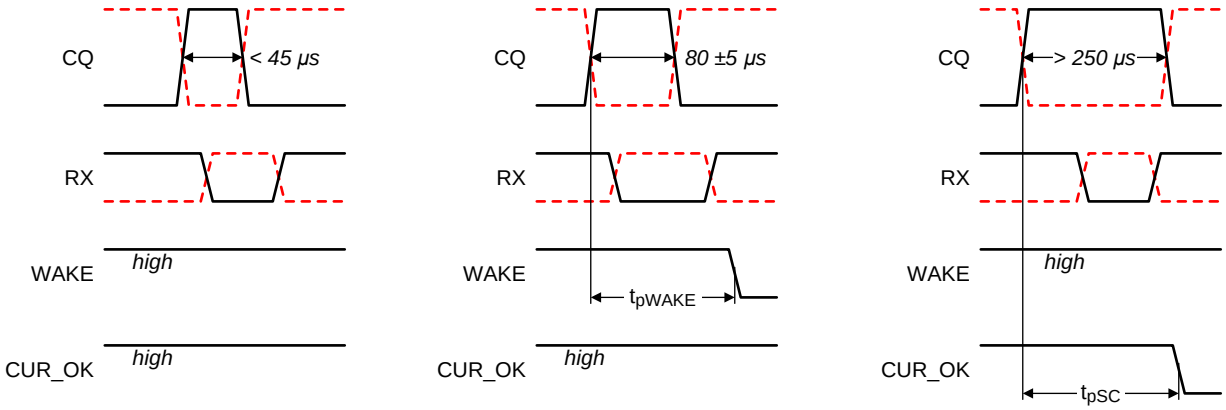
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9.3 Feature Description

9.3.1 Wake-up Detection

The device may be in IO-Link mode or SIO mode. If the device is in SIO mode and the master node wants to initiate communication with the device node, the master drives the CQ line to the opposite of its present state, and will either sink or source the wake up current (IQWU is typically up to 500 mA) for the wake-up duration (t_{WU} is typically 80 µs) depending on the CQ logic level as per the IO-Link specification. The SN65HVD1XX IO-Link PHY detects this wake-up condition and communicates to the local microcontroller via the WAKE pin. The IO-Link Communication Specification requires the device node to switch to receive mode within 500 µs after receiving the Wake-Up signal.

For over-current conditions shorter or longer than a valid Wake-Up pulse, the WAKE pin will remain in a high-impedance (inactive) state. This is illustrated in Figure 8, and discussed in the following paragraph.



a) Over-current due to transient **b) Wake-up pulse from master** **c) Overcurrent due to fault condition**

Figure 8. Over-current and Wake Conditions for EN = H, TX = H (full lines); and TX = L (red dotted lines)

9.3.2 Current Limit Indication – Short Circuit Current Detection

The internal current limit indicator is gated with the wake logic and thus becomes active only under certain conditions of the CQ-voltage (see Table 4).

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Feature Description (continued)

9.3.3 Active Current Limit Condition: $V_{THL} > V_{CQ} \geq V_{THH}$

If the output current at CQ remains at the internally set current limit IO(LIM) for a duration longer than a wake-up pulse (longer than 80 μs), the CUR_OK pin is driven logic low, indicating an over-current condition. The CUR_OK pin returns to the high-impedance (inactive) state when the CQ pin is no longer in a current limit condition. The state diagram shown in Figure 9 illustrates the various states; and, under what conditions the device transitions from one state to another.

9.3.4 Inactive Current Limit Condition: $V_{THL} < V_{CQ} < V_{THH}$

If the voltage at CQ is between the upper and lower receiver input threshold, CUR_OK remains high-impedance.

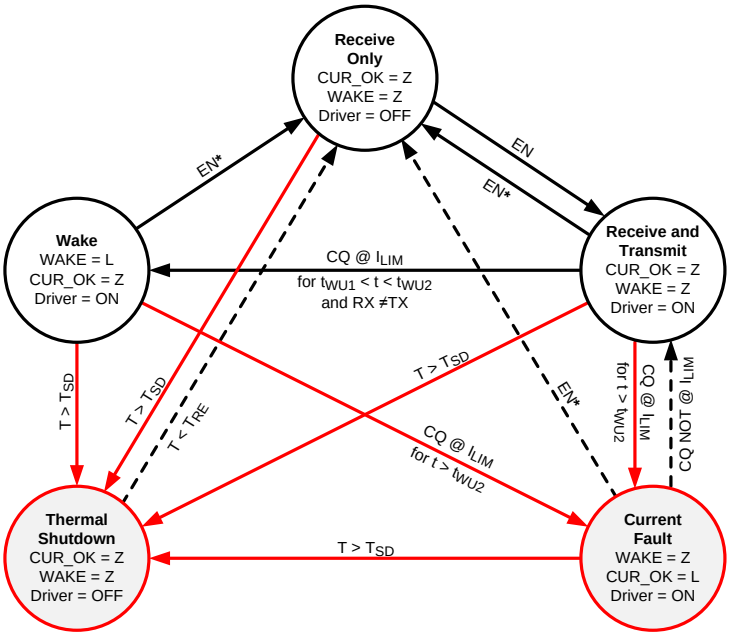


Figure 9. State Diagram of Device Transceiver

9.3.5 Over-temperature Detection

If the transceiver's internal temperature exceeds its over-temperature threshold θT_{SD}, the CQ driver and the voltage regulator (HVD101) are disabled. As soon as the temperature drops below the temperature threshold, the internal circuit re-enables the voltage regulator (HVD101) and the driver, subject to the state of the EN and TX pins.

9.3.6 CQ Current-limit Adjustment

The CQ driver current-limit is determined by the external resistor, R_{SET}, at the ILIM_ADJ pin. Figure 2 shows the typical current-limit characteristics as a function of R_{SET}.

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Feature Description (continued)

9.3.7 Transceiver Function Tables

Table 1. Driver Function

EN	TX	CQ	COMMENT
L or OPEN	X	Z	PHY is in ready-to-receive state
H	L	H	PHY CQ is sourcing current (high-side drive)
H	H or OPEN	L	PHY CQ is sinking current (low-side drive)

Table 2. Receiver Function

CQ Voltage	RX	COMMENT
$V_{CQ} < V_{CHL}$	H	Normal receive mode, input low
$V_{THL} < V_{CQ} < V_{THH}$	?	Indeterminate output, may be either High or Low
$V_{THH} < V_{CQ}$	L	Normal receive mode, input high
OPEN	H	Failsafe output high

Table 3. Wake-Up Function

EN	TX	CQ VOLTAGE	WAKE	COMMENT
L	X	X	Z	PHY is in ready-to-receive state
H	H	$V_{THH} < V_{CQ}$ (t_{WU})	L	PHY receives High-level wake-up request from Master
H	X	$V_{THL} < V_{CQ} < V_{THH}$	?	Indeterminate output, may be either High or Low
H	L	$V_{THL} > V_{CQ}$ (t_{WU})	L	PHY receives Low-level wake-up request from Master

Table 4. Current Limit Indicator Function ($t > t_{WU}$)

EN	TX	CQ VOLTAGE	CQ CURRENT	CUR_OK	COMMENT
H	H	$V_{CQ} \geq V_{THH}$	$\lvert I_{CQ}\rvert > I_{O(LIM)}$	L	CQ current is at the internal limit
			$\lvert I_{CQ}\rvert < I_{O(LIM)}$	Z	Normal operation
		$V_{CQ} < V_{THH}$	X	Z	Current limit indicator is inactive
H	L	$V_{CQ} < V_{THL}$	$\lvert I_{CQ}\rvert > I_{O(LIM)}$	L	CQ current is at the internal limit
			$\lvert I_{CQ}\rvert < I_{O(LIM)}$	Z	Normal operation
		$V_{CQ} \geq V_{THL}$	X	Z	Current limit indicator is inactive
L	X	X	X	Z	Driver is disabled, Current limit indicator is inactive

Table 5. Temperature Indicator Function

INTERNAL TEMPERATURE	OVER TEMPERATURE	TEMP_OK	COMMENT
$T < T_{WARN}$	Not Over-Temperature	Z	Normal operation
$T_{WARN} < T\uparrow < T_{SD}$	Not Over-Temperature	L	Temperature warning
$T_{SD} < T$	Over-Temperature Disabled	L	Over-Temperature disabled
$T_{WARN} < T\downarrow < T_{RE}$	Not Over-Temperature	L	Temperature recovery

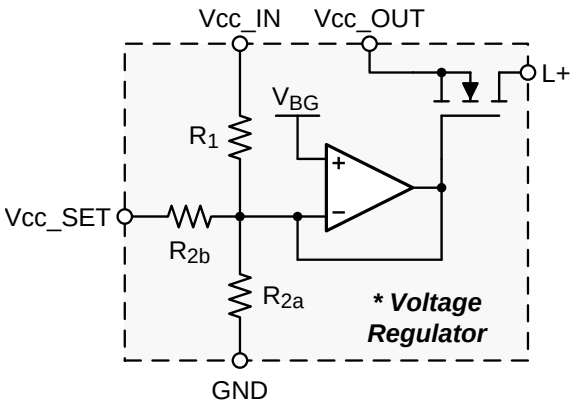
Table 6. Power Supply Indicator Function

V_{L+}	V_{CC}	PWR_OK	COMMENT
$V_{L+} < V_{PG1}$	$V_{POR2} < V_{CC} < V_{PG2}$	L	Both supplies too low
$V_{PG1} < V_{L+}$	$V_{POR2} < V_{CC} < V_{PG2}$	L	V_{CC} too low
$V_{L+} < V_{PG1}$	$V_{PG2} < V_{CC}$	L	V_{L+} too low
$V_{PG1} < V_{L+}$	$V_{PG2} < V_{CC}$	Z	Both supplies correct

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9.3.8 Voltage Regulator (Not Available in SN65HVD102)

The SN65HVD101 integrates a linear voltage regulator which supplies power to external components as well as to the PHY itself. The voltage regulator is specified for L+ voltages in the range of 9V to 30V with respect to GND. The output voltage can be set using the Vcc_SET pin (see Figure 10). When this pin is left open (floating) then the output voltage is 5V. When it is connected to GND then the output voltage is 3.3V.



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* HVD101 only

Figure 10. Voltage Regulator Equivalent Circuit

9.4 Device Functional Modes

The SN65HVD101 and SN65HVD102 can operate in three different modes:

- **N-Switch SIO Mode**
  Set TX pin High and use EN pin as control for realizing the function of an N-switch (low-side driver) on CQ.
- **P-Switch SIO Mode**
  Set TX pin Low and use EN pin as control for realizing the function of a P-switch (high-side driver) on CQ.
- **Push-Pull / Communication Mode**
  Set EN pin high and toggle TX as control for realizing the function of a Push-Pull output on CQ.

Table 7 to Table 9 summarize the pin configurations to accomplish the above functional modes.

Table 7. N-Switch SIO Mode

EN	TX	CQ
L	H	Hi-Z
H	H	N-Switch

Table 8. P-Switch SIO Mode

EN	TX	CQ
L	L	Hi-Z
H	L	P-Switch

Table 9. Push-Pull / Communication Mode

EN	TX	CQ
L	X	Hi-Z
H	H	N-Switch
H	L	P-Switch

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD101 and SN65HVD102 IO-Link transceivers can be used in slave devices communicating with an IO-Link master, or as simple digital I/O to either sense or drive a wide range of sensors and loads.

10.2 Typical Application

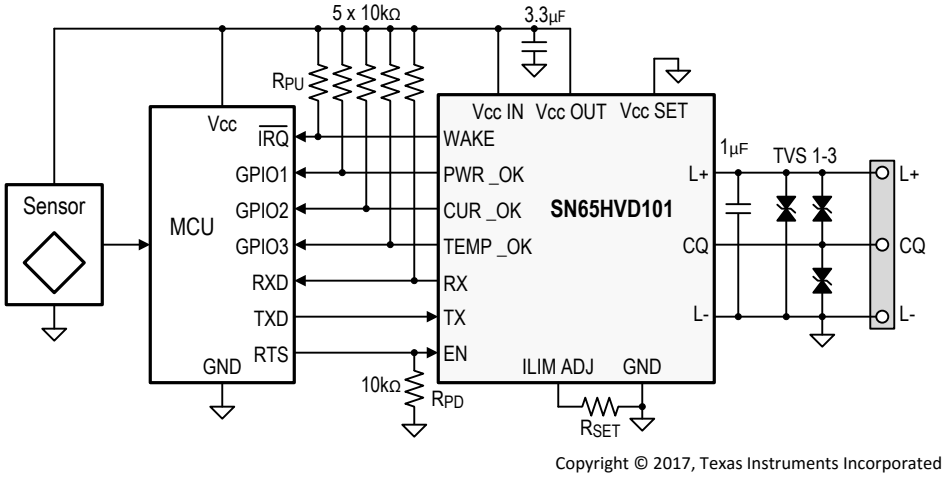


Figure 11. Typical Application Schematic, SN65HVD101 with 3.3V Output Supply

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 10 as design parameters.

Table 10. Design Parameters

DESIGN PARAMETER		EXAMPLE VALUE
TRANSCEIVER	Input voltage range (L+)	24V
	Maximum load current (CQ)	250 mA
	Output voltage (Vcc_OUT)	3.3 V
	Maximum output current (Vcc_OUT)	20 mA
SURGE PROTECTION	Peak Voltage (L+, CQ)	2 kV
(1.2/50 – 8/20µs)	Peak Current via R = 500 Ω, C = 0.5 µF	4 A
	Maximum TVS Clamping Voltage	> 50 V
	Minimum TVS Standoff Voltage	> 30 V
	Maximum Ambient Temperature, TA	100 °C
	Maximum Junction Temperature, TJ	150 °C

10.2.2 Detailed Design Procedure

The following recommendations on device configuration and components selection focus on the design of a digital output driver using SN65HVD101 with protection against surge transients from a 1.2/50 – 8/20 µs combination waveform generator (CWG) with 2 kV peak test voltage and 500 Ω source impedance.

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10.2.2.1 Transceiver Configuration (SN65HVD101)

1. Choose a 24 V nominal dc supply for L+.
2. From the current-limit characteristics in Figure 2 derive the resistor value of R_{SET} = 4 kΩ for a current limit of $I_{O(LIM)}$ = 250 mA.
3. Connect V_{CC_SET} to ground for a 3.3V output at V_{CC_OUT}.
4. Connect V_{CC_IN} to V_{CC_OUT} to assure proper output voltage regulation of V_{CC_OUT}.
5. Buffer V_{CC_OUT} with a 3.3µF, 10V ceramic capacitor.
6. Connect the receiver and diagnostic outputs via 10 kΩ pull-up resistors to V_{CC_OUT} to provide defined voltage potentials to the controller inputs during high-impedance states.
7. Connect the driver enable pin, EN, via a 10 kΩ pull-down resistor to ground to maintain the driver disabled during power up.

10.2.2.2 Maximum Ambient Temperature Check

For a 250 mA current limit, the maximum voltage drop across the high-side switch is given with V_{RQH} = 3 V (taken from *Electrical Characteristics*: **Driver** section). This causes an internal power consumption of:

$$P_{D-INT} = V_{RQH} \cdot I_{O(lim)} = 3\,V \cdot 250\,mA = 750\,mW \quad (1)$$

Multiply this value with the Junction-to-ambient thermal resistance of θ_{JA} = 33.8 °C/W (taken from *Thermal Information*) to receive the difference between junction temperature, T_J, and ambient temperature, T_A:

$$\Delta T = T_J - T_A = P_{D-INT} \cdot \theta_{JA} = 750\,mW \cdot 33.8\,^{\circ}C/W = 25.4\,^{\circ}C \quad (2)$$

Add this value to the maximum ambient temperature of T_A = 100 °C to receive the final junction temperature:

$$T_{J-max} = T_{A-max} + \Delta T = 100\,^{\circ}C + 25.4\,^{\circ}C = 125.4\,^{\circ}C \quad (3)$$

As long as $T_{J\text{-}max}$ is below the recommended maximum value of 150 °C, no overheating will occur.

10.2.2.3 Transient Protection

A commonly applied surge immunity test in digital I/O designs is the application of the 1.2/50 – 8/20 µs combination waveform, specified in IEC61000-4-5, with a source impedance of 500 Ω and a peak test voltage of $V_{O\text{-}pk}$ = 2 kV, which results in a peak surge current of $I_{S\text{-}pk}$ = 4 A.

The test set-up for line-to-line and line-to-ground measurements is shown in Figure 12; the calculation of the surge peak current is shown in Figure 13.

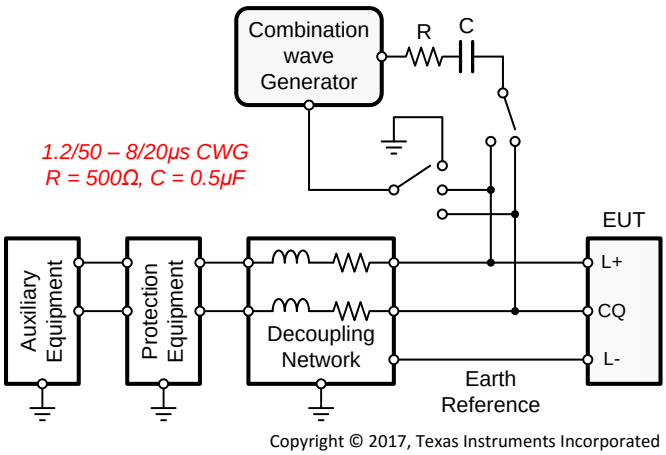
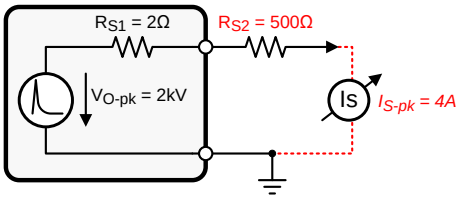


Figure 12. Surge Test Set-up



$$I_{S-pk} \approx \frac{V_{OC-pk}}{R_S} = \frac{2kV}{502\Omega} = 4A$$

Figure 13. Peak Current Calculation

10.2.2.4 TVS Evaluation

Because the maximum transceiver supply at L+ is specified with 30 V, the TVS standoff or peak working voltage must be higher than this value. The standoff voltage is the voltage where the TVS does not conduct yet. Transient voltage suppressors with this high standoff have peak pulse powers starting at 200 W. Their peak pulse power however is usually rated based on a 10/1000 µs current pulse, which is commonly applied in telecom application. It is therefore necessary to derate the peak power value from a 10/1000 µs to a 8/20 µs pulse.

For this example the bidirectional, 200 W TVS, SMF33CA, was selected. Its main parameters and their derated values are listed in Table 11. The peak pulse power rating for a 10/1000 µs pulse is shown in Figure 14.

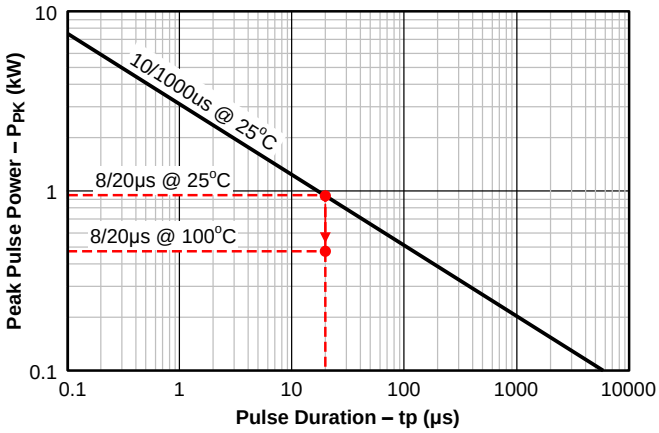


Figure 14. Peak Pulse Power Rating

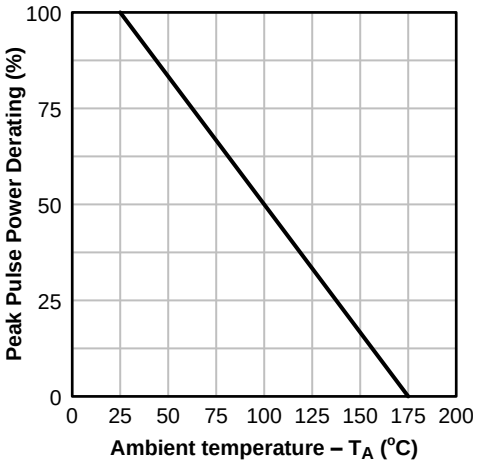


Figure 15. Pulse Derating Curve

At the pulse duration of 1000 µs the device has a peak pulse power rating of 200 W. To determine the peak power for a 8/20 µs pulse, move up the power rating curve until you hit the 20 µs pulse duration. The peak pulse power rating at this point is about 950 W.

Note these values are valid for 25 °C ambient temperature only. Because the operating ambient temperature in this example is specified with 100 °C however, the peak pulse power must be further derated for the higher ambient temperature using the pulse derating curve in Figure 15. This curve shows that the peak power level at 25 °C drops by 50 % when reaching 100 °C, so from 950 W down to 475 W. This drop is shown in Figure 14 through the arrow pointing down to the second peak power level for a 20 µs pulse duration at 100 °C.

Table 11. TVS Parameters

PARAMETER	SYMBOL	SMF33CA	UNIT
Maximum Working Peak Voltage	VWM	33	V
Minimum Breakdown Voltage at 1 mA	VBR	36.7	V
Maximum Clamping Voltage at IPP	VCL	53.3	V
Peak Pulse Power (10/1000 µs) at 25°C	PPK1	200	W
Peak Pulse Current (10/1000 µs) at 25°C	IPP1	3.75	A
Derated Peak Power (8/20 µs) at 25°C	PPK2	950	W
Derated Peak Current (8/20 µs) at 25°C	IPP2	17.76	A
Derated Peak Power (8/20 µs) at 100°C	PPK3	475	W
Derated Peak Current (8/20 µs) at 100°C	IPP3	8.9	A

To determine the peak currents for the various peak power ratings, TVS manufacturers advise to assume the maximum clamping voltage as being constant, because this clamping level also presents the device maximum failing voltage if its value is exceeded. The peak current for a given power rating is therefore calculated via:

$$I_{PP} = P_{PK} / V_{CL} \quad (4)$$

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So for the 8/20 μs peak power of 475 W at 100 °C, the peak pulse current is I_{PP3} = 475 W ÷ 53.3 V = 8.9 A. The new derived values of P_{PK} and I_{PP} in combination with the values for breakdown and clamping voltage, V_{BR} and V_{CL}, from Table 11, yield a new I-V characteristics of the SMF33CA TVS when exposed to a 8/20 μs pulse.

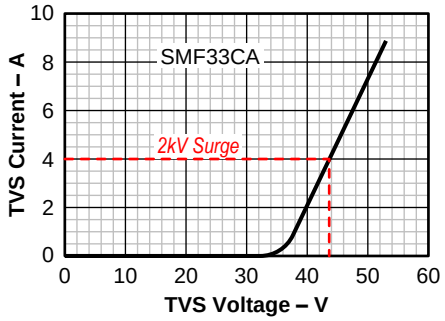
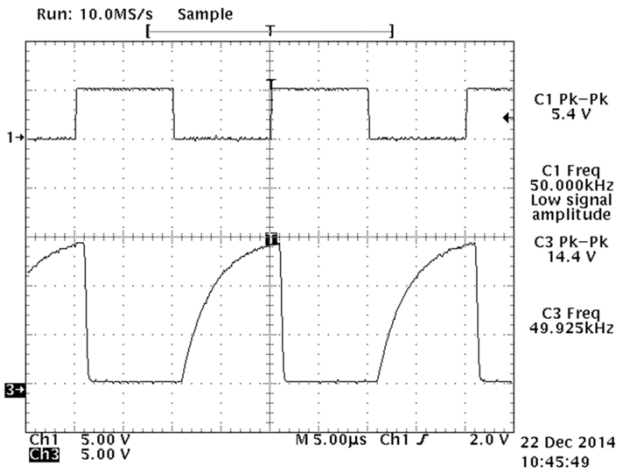


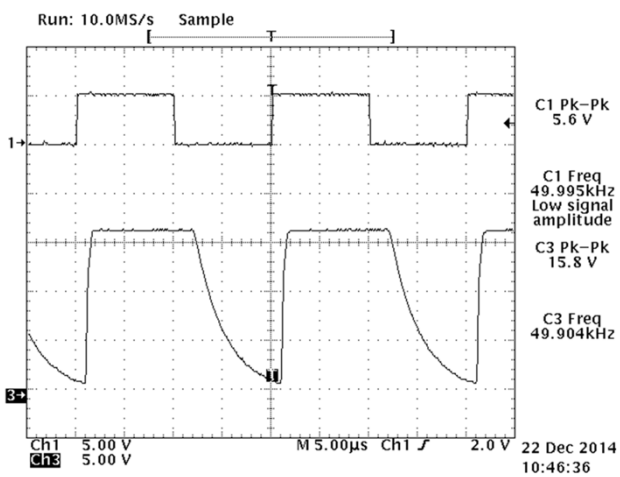
Figure 16. TVS Characteristic for 8/20 μs Current Pulse

Because the maximum surge current of the CWG in Figure 13 is only 4 A at 2 kV test voltage, the TVS clamping voltage at this level is only 44 V. This voltage is sufficiently below the absolute maximum voltage rating of 50 V for a 100 μs pulse at the L+ and CQ terminals of the SN65HVD101 and SN65HVD102 transceivers, causing no device damage.

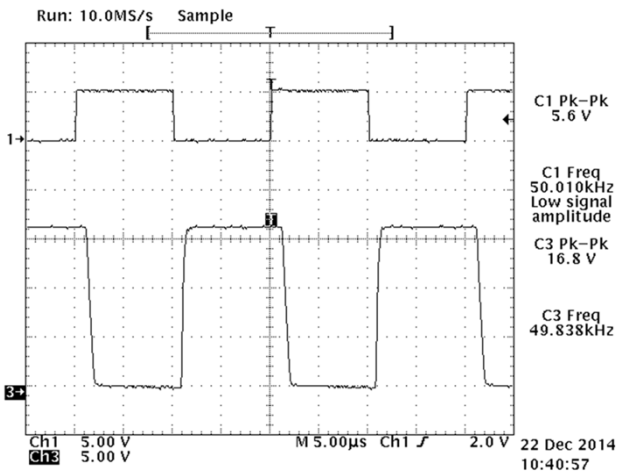
10.2.3 Application Curves



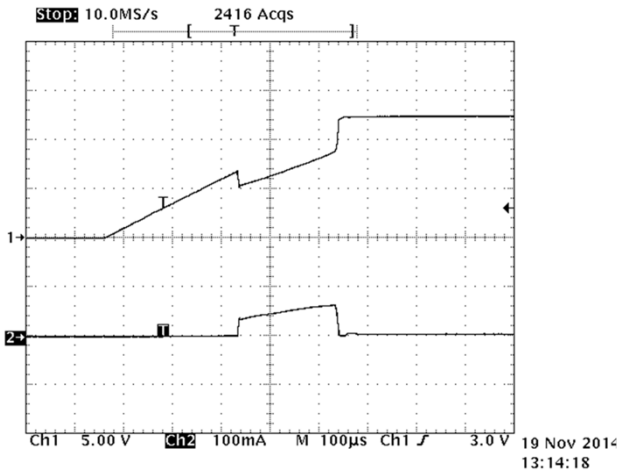
N-Switch Mode
Top waveform = EN
TX pin High
Bottom waveform = CQ



P-Switch Mode
Top waveform = EN
TX pin Low
Bottom waveform = CQ

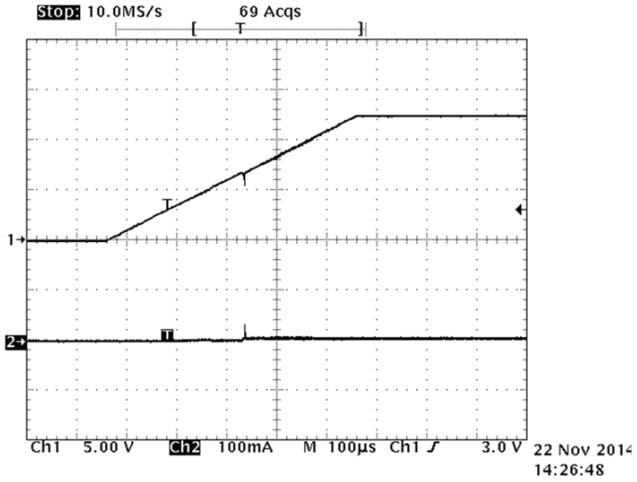


Push-Pull Mode
Top waveform = TX
Bottom waveform = CQ



EN pin High
Bottom waveform = CQ

V_{CC} (top) and I_{CC} (bottom) at Start-Up with 3.3 µF LDO Output Capacitor



V_{CC} (top) and I_{CC} (bottom) at Start-Up without 3.3 µF LDO Output Capacitor

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10.3 System Examples

10.3.1 Driver for Incandescent Lamp Loads

The following circuit shows the SN65HVD101 driving an incandescent lamp load. For this and other types of resistive loads only two TVS diodes are used to protect the CQ and L+ lines to ground.

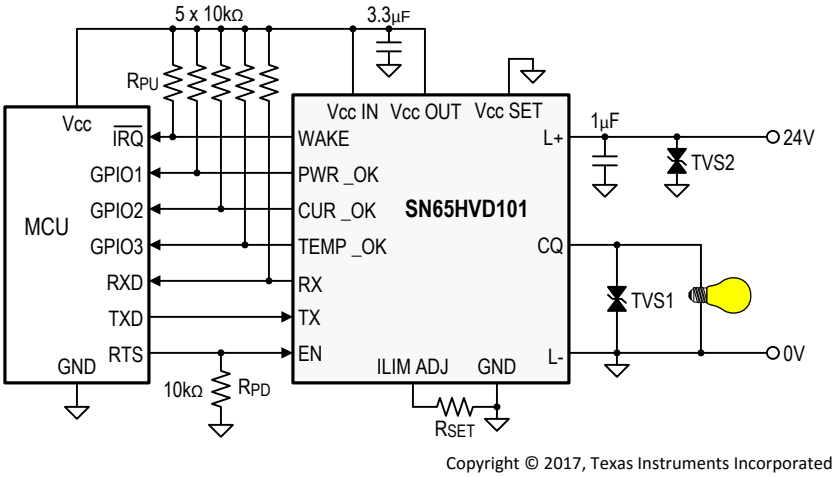


Figure 17. SN65HVD101 Driving Incandescent Lamp Load

The resistance of an incandescent lamp filament varies strongly with temperature. The initial (cold-filament) resistance of tungsten-filament lamps is less than 10% of the steady-state (hot-filament) resistance. For example, a 100-watt, 120-volt lamp has a resistance of 144 Ω when lit, but the cold resistance is much lower (about 9.5 Ω). The initial “in-rush” current is therefore high compared to the steady-state current. Within 3 to 5 ms the current falls to approximately half the hot current.

For typical general-service lamps, the current reaches steady-state conditions in less than about 100 milliseconds. The ‘HVD10x CQ output will remain at the selected current-limit as the filament warms up, and then will stay at the steady-state current level. For example, a 6W, 24VDC indicator lamp has a steady-state current of 250 mA. However, the initial in-rush current could be over 2 Amps if unlimited. If the HVD10x current limit is set to 350 mA, this current will warm up the filament during the initial lamp turn-on, and the final current will be below the current limit. If the CQ output current is at the limit for longer than t_{SC}, the SC output will be active. The local controller can disable the CQ driver if the high current is not expected, or can re-check the SC output after 100 ms if the load is known to be incandescent.

System Examples (continued)

10.3.2 Driver for Inductive Loads

The following circuit shows the SN65HVD101 driving an inductive load. In this case three TVS diodes are necessary to protect L+ to ground and CQ to Ground and to L+.

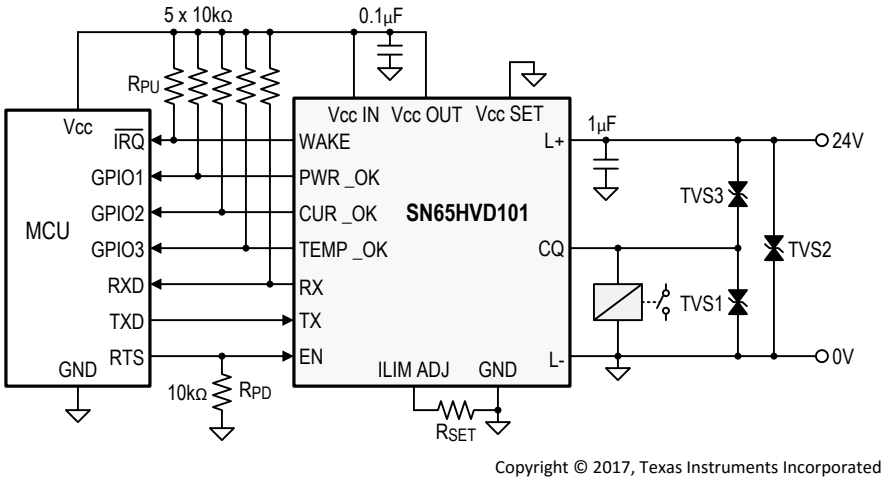


Figure 18. SN65HVD101 Driving Inductive Relay Load

When the high-side switch in the transceiver turns on, TVS1 might conduct when the voltage across the inductive load rises above the TVS breakdown threshold. This might not be desirable but, due to V_L = L × di/dt, can happen if the load inductance is sufficiently high.

When the transceiver turns off, the voltage across the inductance changes polarity to maintain current flow in the same direction. Again, TVS1 might conduct if the peak voltage across the inductor exceeds the TVS breakdown threshold during turn-off.

The main issue however is the voltage difference between the positive supply (L+) and the data line (CQ). Without TVS3 this difference could rise to twice the supply level. At the much lower TVS about lower TVS breakdown threshold however, TVS3 conducts and the voltage difference is limited to the TVS clamping voltage.

11 Power Supply Recommendations

The SN65HVD101 and SN65HVD102 transceivers are designed to operate from a 24 V nominal supply at L+, which can vary by +6 V and –15 V from the nominal value to remain within the device recommended supply voltage range of 9 V to 30 V. This supply should be buffered with at least a 1 µF/60V ceramic capacitor placed close to the device pin.

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12 Layout

12.1 Layout Guidelines

- Use a 4-layer board with Layer 1 (top layer) for control signals, Layer 2 as Power Ground Layer for L– and GND), Layer 3 for the 24 V supply plane (L+), and Layer 4 for the regulated output supply (V_{CC_OUT}).
- Use entire planes for L+, V_{CC_OUT}, and L– and GND to assure minimum inductance during fast load or transient current changes.
- The L+ terminal must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value is 1 μF to 4.7 μF. The capacitor must have a voltage rating of 50 V minimum and a X5R or X7R dielectric.
- The optimum placement is closest to the transceiver's L+ and L– terminals to reduce supply drops during large supply current loads. See Figure 19 for a PCB layout example
- Place TVS diode close to the connector to prevent the transient energy from entering the circuitry.
- Use two vias when connecting TVS diodes or capacitors to the L– and L+ planes to maintain low inductance during fast load or transient current changes.
- Connect all open-drain control outputs and the receiver output via 10 kΩ pull-up resistors to the V_{CC_OUT} plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- Connect the transceiver enable pin via a 10 kΩ pull-down resistor to ground, to assure the driver output is disabled during power-up.
- Connect V_{CC_SET} directly to ground to make V_{CC_OUT} = 3.3 V, or leave it open to make V_{CC_OUT} = 5 V.
- Connect V_{CC_IN} directly to V_{CC_OUT} to assure proper voltage regulation.
- Buffer the regulated output voltage at V_{CC_OUT} to ground with a low-ESR, 3.3μF, ceramic bypass-capacitor. The capacitor should have a voltage rating of 10 V minimum and a X5R or X7R dielectric.

12.2 Layout Example

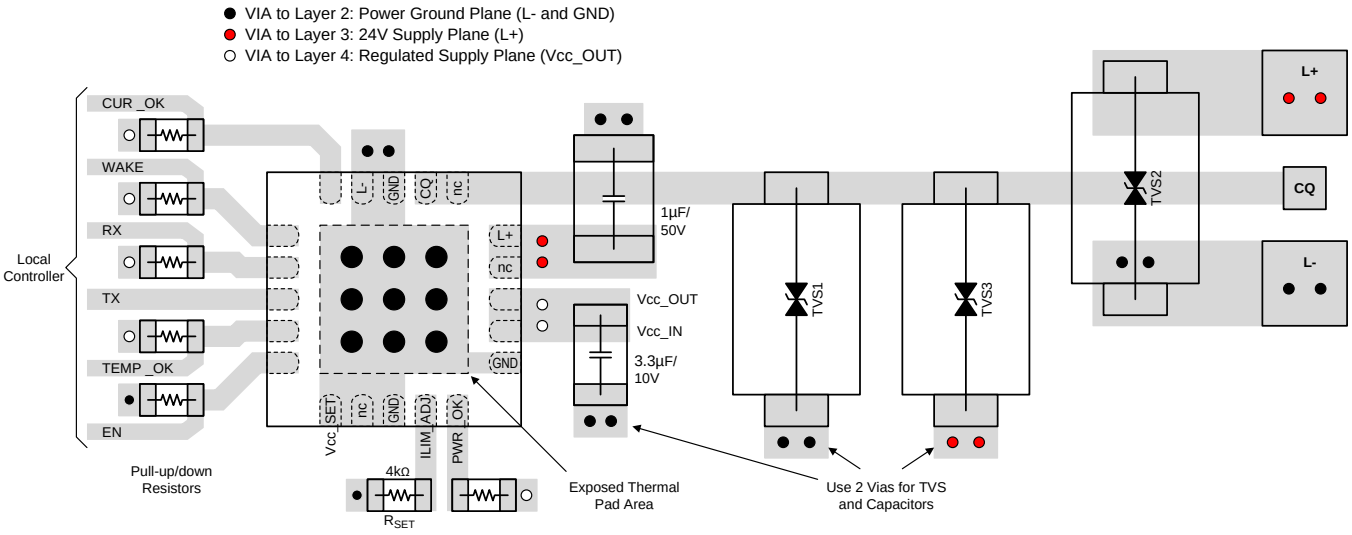


Figure 19. Layout Example

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12. Related Links

PARTS	PRODUCT FOLDER	ODDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD101	Click here	Click here	Click here	Click here	Click here
SN65HVD102	Click here	Click here	Click here	Click here	Click here

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD101RGBR	ACTIVE	VQFN	RGB	20	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD101	Samples
SN65HVD101RGBT	ACTIVE	VQFN	RGB	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD101	Samples
SN65HVD102RGBR	ACTIVE	VQFN	RGB	20	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD102	Samples
SN65HVD102RGBT	ACTIVE	VQFN	RGB	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD102	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

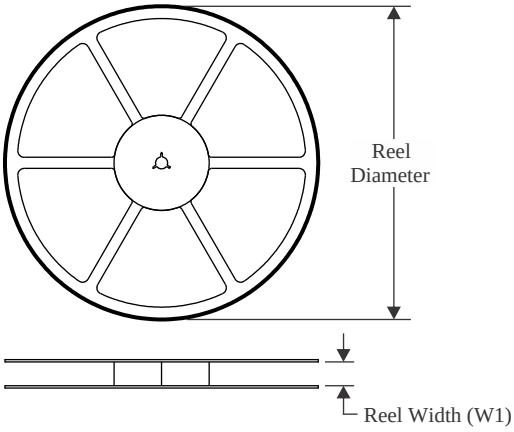
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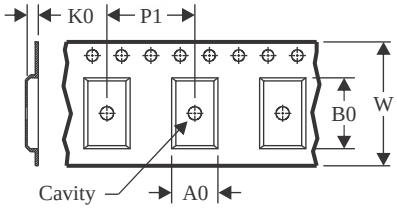
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

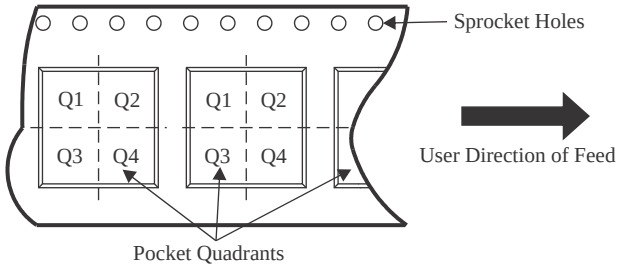


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

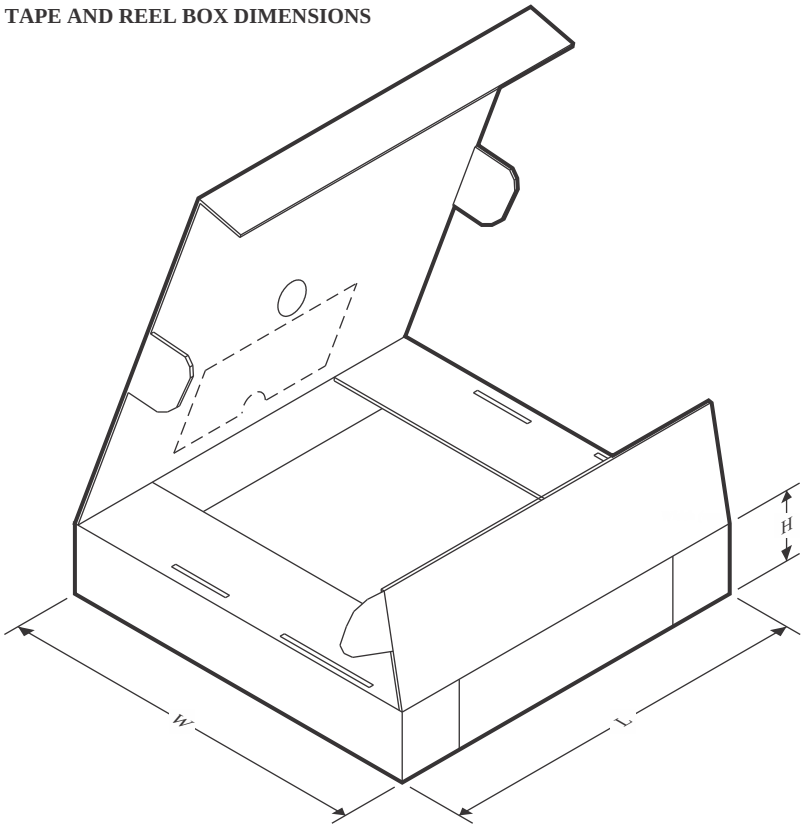
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD101RGBR	VQFN	RGB	20	1000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65HVD101RGBT	VQFN	RGB	20	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65HVD102RGBR	VQFN	RGB	20	1000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65HVD102RGBT	VQFN	RGB	20	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

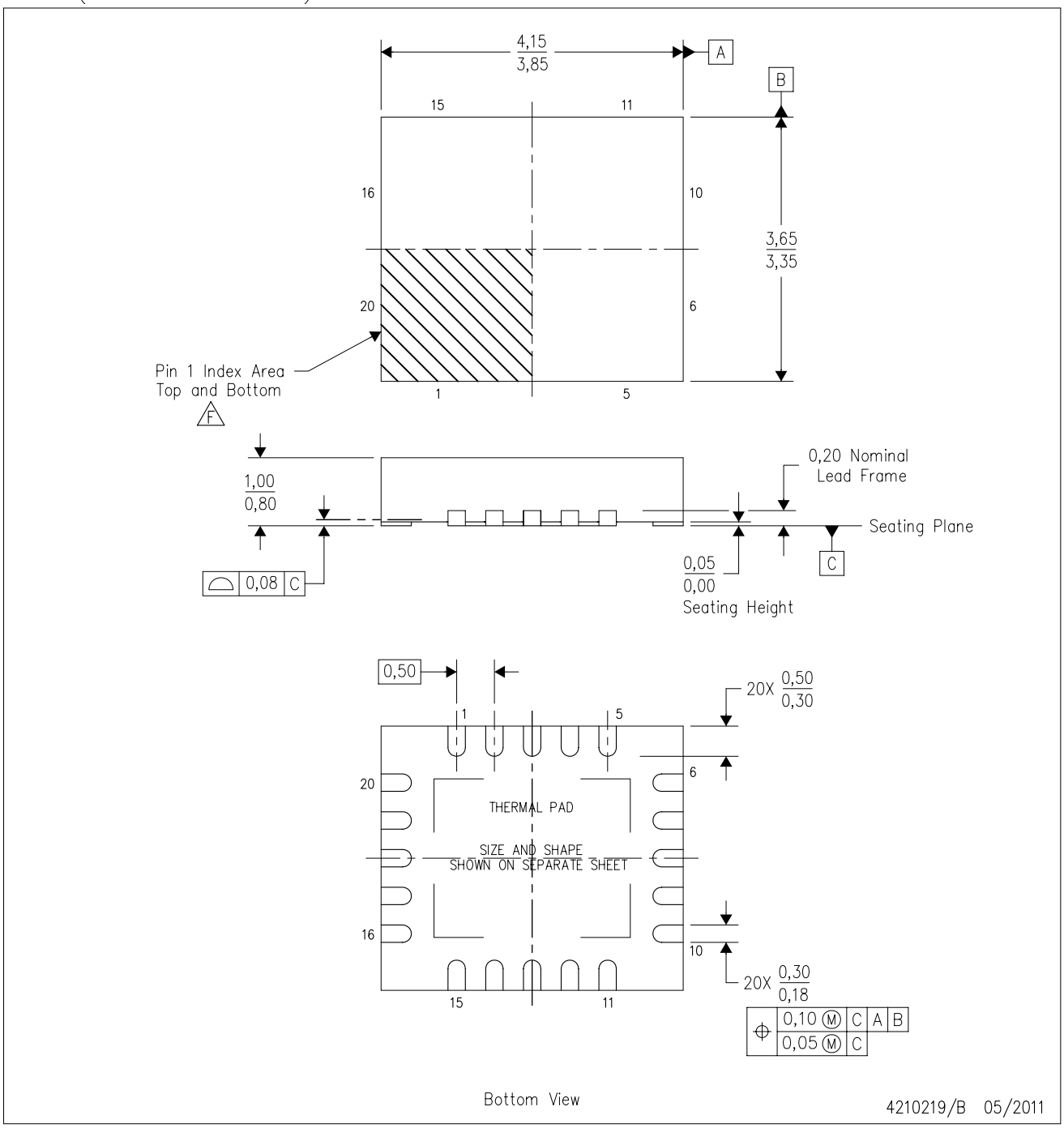
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD101RGBR	VQFN	RGB	20	1000	367.0	367.0	35.0
SN65HVD101RGBT	VQFN	RGB	20	250	210.0	185.0	35.0
SN65HVD102RGBR	VQFN	RGB	20	1000	367.0	367.0	35.0
SN65HVD102RGBT	VQFN	RGB	20	250	210.0	185.0	35.0

RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

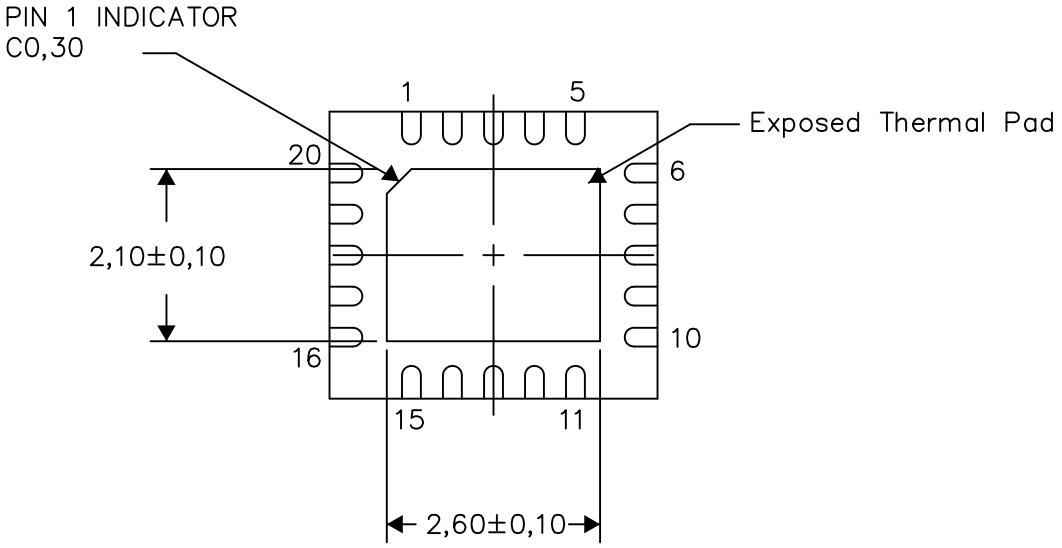
RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



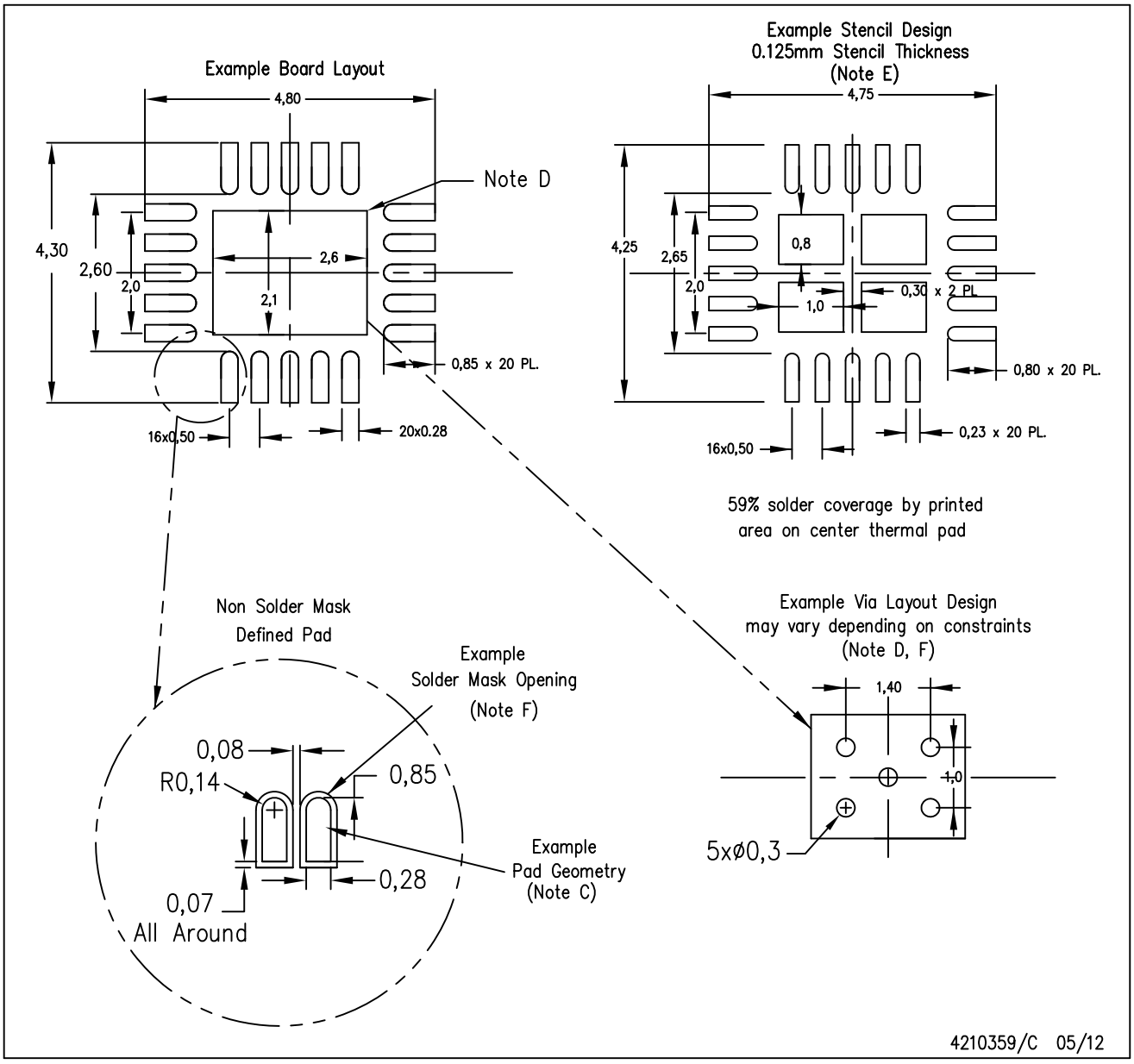
Bottom View

Exposed Thermal Pad Dimensions

4210242/C 05/12

NOTE: All linear dimensions are in millimeters

RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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