ISO772x-Q1 High-Speed, Robust EMC, Reinforced Dual-Channel Digital Isolators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified With the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 3A
  - Device CDM ESD classification level C6
- Functional Safety-Capable
  - Documentation available to aid functional safety system design: ISO7720-Q1, ISO7721-Q1
- 100 Mbps data rate
- Robust isolation barrier:
  - >30-Year projected lifetime at 1.5 kV_{RMS} working voltage
  - Up to 5000 V_{RMS} Isolation Rating
  - Up to 12.8 kV surge capability
  - ±100 kV/µs Typical CMTI
- Wide supply range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V level translation
- Default output *High* (ISO772x) and *Low* (ISO772xF) Options
- Low power consumption, typical 1.7 mA per channel at 1 Mbps
- Low propagation delay: 11 ns typical
- Robust electromagnetic compatibility (EMC)
  - System-Level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Wide-SOIC (DW-16, DWV-8) and Narrow-SOIC (D-8) package options
- Safety-related Certifications
  - VDE reinforced insulation per DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1 certifications

2 Applications

- Hybrid, electric and power train system (EV/HEV)
  - Battery management system (BMS)
  - On-board charger
  - Traction inverter
  - DC/DC converter
  - Inverter and motor control

3 Description

The ISO772x-Q1 devices are high-performance, dual-channel digital isolators with 5000 V_{RMS} (DW and DWV packages) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. This family includes devices with reinforced insulation ratings according to VDE, CSA, TUV and CQC.

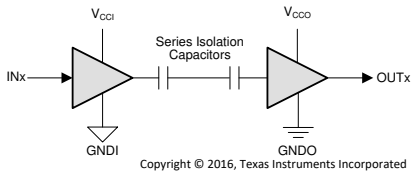
The ISO772x-Q1 devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. The ISO7720-Q1 device has both channels in the same direction while the ISO7721-Q1 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See the *Device Functional Modes* section for further details.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as CAN and LIN, from damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO772x-Q1 devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO772x-Q1 family of devices is available in 16-pin SOIC wide-body (DW), 8-pin SOIC wide-body (DWV), and 8-pin SOIC narrow-body (D) packages.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
ISO7720-Q1 ISO7721-Q1	D (8)	4.90 mm × 3.91 mm
	DW (16)	10.30 mm × 7.50 mm
	DWV (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



V_{CCI}=Input supply, V_{CCO}=Output supply
GNDI=Input ground, GNDO=Output ground

Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2020) to Revision C (December 2023) — **Page**

- Changed standard name from: "DIN V VDE V 0884-11:2017-01" to: "DIN EN IEC 60747-17 (VDE 0884-17)" throughout the document....1
- Removed references to standard IEC/EN/CSA 60950-1 throughout the document....1
- Removed standard revision and year references from all standard names throughout the document....1
- Updated numbering format for tables, figures and cross-references throughout document....1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations....5
- Updated electrical and switching characteristics to match device performance....5
- Updated Climatic category for D package....8
- Updated Maximum working voltages for DW-16 and D-8....10
- Changed working voltage lifetime margin from: 87.5% to: 50%, minimum required insulation lifetime from: 37.5 years to: 30 years and insulation lifetime per TDDB from: 135 years to: 169 years per DIN EN IEC 60747-17 (VDE 0884-17)....26
- Changed Figure 9-6 per DIN EN IEC 60747-17 (VDE 0884-17)....26

Changes from Revision A (April 2020) to Revision B (October 2020) — **Page**

- Added Functional Safety bullets....1
- Added D-8 values for TUV column....10
- Changed minimum CMTI value from 40 kV/µs to 85 kV/µs throughout the document....12

Changes from Revision * (March 2016) to Revision A (April 2020) — **Page**

- Made editorial and cosmetic changes throughout the document....1

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- Changed From: "Isolation Barrier Life: >40 Years" To:">100-Year Projected Lifetime at 1.5 kV_{RMS} Working Voltage" in Section 1 1
- Added "Up to 5000 V_{RMS} Isolation Rating" in Section 1 1
- Added "Up to 12.8 kV Surge Capability" in Section 1 1
- Added "±8 kV IEC 61000-4-2 Contact Discharge Protection across Isolation Barrier" in Section 1 1
- Updated certification-related bullets in Section 1 and changed VDE standard name From: DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 To: DIN VDE V 0884-11:2017-01 throughout the document..... 1
- Updated Section 2 list..... 1
- Updated Figure 3-1 to show two isolation capacitors in series per channel instead of a single isolation capacitor 1
- Added Climatic category to table..... 8
- Updated CSA column and changed DW package to (DW-16)..... 10
- Changed t_{ie} TYP value from 1.5 to 1 throughout the document..... 15
- Switched the line colors for V_{CC} at 2.5 V and V_{CC} at 3.3 V in the *Low-Level Output Voltage vs Low-Level Output Current* graph..... 18
- Deleted EN from the *Common-Mode Transient Immunity Test Circuit* figure..... 20
- Corrected ground symbols for "Input (Devices with F suffix)" in Section 8.4.1 23
- Added Section 9.2.3.1 sub-section under Section 9.2.3 section 26
- Added '*How to use isolation to improve ESD, EFT and Surge immunity in industrial systems*' application report to Section 12.2 section 30

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5 Pin Configuration and Functions

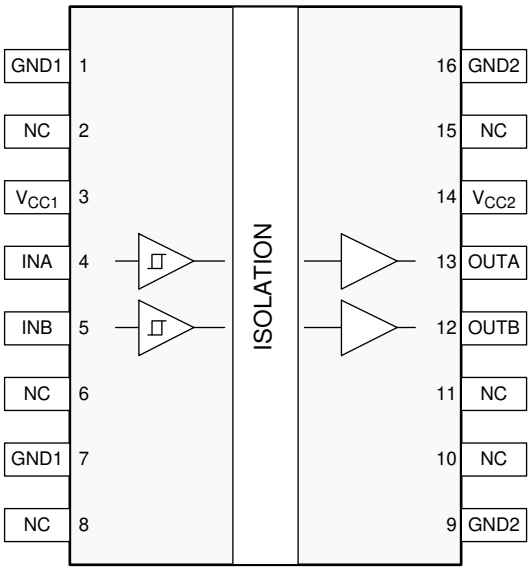

Figure 5-1. ISO7720-Q1 DW Package 16-Pin SOIC Top View

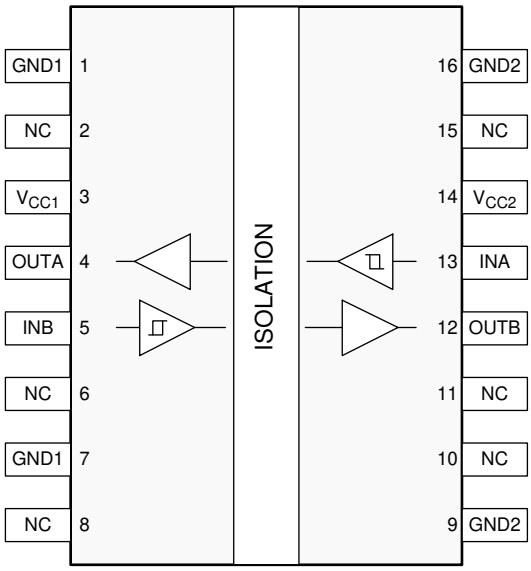

Figure 5-2. ISO7721-Q1 DW Package 16-Pin SOIC Top View

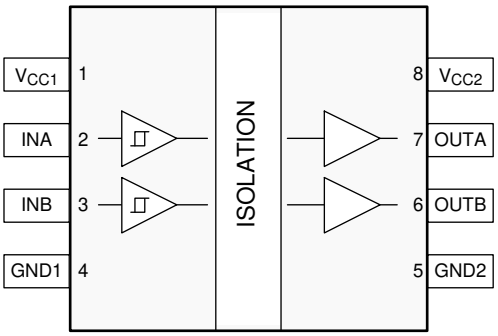

Figure 5-3. ISO7720-Q1 D and DWV Package 8-Pin SOIC Top View

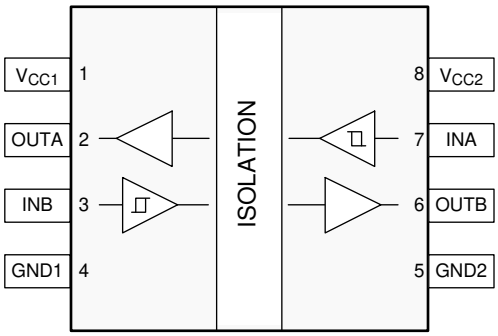

Figure 5-4. ISO7721-Q1 D and DWV Package 8-Pin SOIC Top View

Table 5-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	DW PACKAGE		D, DWV PACKAGE			
	ISO7720-Q1	ISO7721-Q1	ISO7720-Q1	ISO7721-Q1		
GND1	1, 7	1, 7	4	4	—	Ground connection for V_{CC1}
GND2	9 16	9 16	5	5	—	Ground connection for V_{CC2}
INA	4	13	2	7	I	Input, channel A
INB	5	5	3	3	I	Input, channel B
NC	2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	—	—	—	Not connected
OUTA	13	4	7	2	O	Output, channel A
OUTB	12	12	6	6	O	Output, channel B
V_{CC1}	3	3	1	1	—	Power supply, V_{CC1}
V_{CC2}	14	14	8	8	—	Power supply, V_{CC2}

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6 Specifications

6.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)	-0.5	6	V
V	Voltage at INx, OUTx	-0.5	V_{CCX} + 0.5 (3)	V
I_O	Output current	-15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±6000	V
		Charged device model (CDM),per AEC Q100-011	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(2) (3)	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(3) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2} (1)	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High level output current	V_{CCO} = 5 V (2)	-4			mA
		V_{CCO} = 3.3 V	-2			
		V_{CCO} = 2.5 V	-1			
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High level Input voltage		0.7 x V_{CCI} (2)		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
DR(3)	Data Rate		0		100	Mbps
T_A	Ambient temperature		-55	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(3) 100 Mbps is the maximum specified data rate, although higher data rates are possible

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6.4 Thermal Information

THERMAL METRIC(1)		ISO772x-Q1			UNIT
		DW (SOIC)	DWV (SOIC)	D (SOIC)	
		16 PINS	16 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	84.3	137.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.6	36.3	54.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	47.0	71.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	32.3	7.4	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.2	45.1	70.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7720-Q1						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input 50-MHz 50% duty cycle square wave			110	mW
P_{D1}	Maximum power dissipation (side-1)				22	mW
P_{D2}	Maximum power dissipation (side-2)				88	mW
ISO7721-Q1						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-MHz 50% duty cycle square wave			110	mW
P_{D1}	Maximum power dissipation (side-1)				55	mW
P_{D2}	Maximum power dissipation (side-2)				55	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS		VALUE			UNIT
				DW	DWV	D	
IEC 60664-1							
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air		8	8.5	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface		8	8.5	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)		17	17	17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A		>600	>600	>600	V
	Material Group	According to IEC 60664-1		I	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}		I–IV	I–IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}		I–IV	I–IV	I-III	
		Rated mains voltage ≤ 600 V_{RMS}		I–IV	I–IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}		I-III	I-III	n/a	
DIN EN IEC 60747-17 (VDE 0884-17)(2)							
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	ISO772x	2121	2121	637	V_{PK}
			ISO7721B	1414	n/a	n/a	
V_{IOWM}	Maximum working isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test, see Figure 9-6	ISO772x	1500	1500	450	V_{RMS}
			ISO7721B	1000	n/a	n/a	
		DC voltage	ISO772x	2121	2121	637	V_{DC}
			ISO7721B	1414	n/a	n/a	
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)		8000	7071	4242	V_{PK}
V_{IMP}	Maximum impulse voltage (3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	ISO772x	8000	8000	5000	V_{PK}
			ISO7721B	6000	n/a	n/a	
V_{IOSM}	Maximum surge isolation voltage(4)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform, per IEC 62368-1	ISO772x	12800	12800	10000	V_{PK}
			ISO7721B	7800	n/a	n/a	V_{PK}
q_{pd}	Apparent charge(5)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s		≤ 5	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s;	$V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s (ISO772x)	≤ 5	≤ 5	≤ 5	
			$V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s (ISO7721B)	≤ 5	n/a	n/a	
		Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$ (ISO772x) or $V_{pd(m)} = 1.5 \times V_{IORM}$ (ISO7721B) , t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)		≤ 5	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz		~0.5	~0.5	~0.5	pF
R_{IO}	Isolation resistance(6)	V_{IO} = 500 V, T_A = 25°C		> 10^{12}	> 10^{12}	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C		> 10^{11}	> 10^{11}	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C		> 10^9	> 10^9	> 10^9	
	Pollution degree			2	2	2	
	Climatic category			55/125/21	55/125/21	55/125/21	
UL 1577							

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PARAMETER		TEST CONDITIONS	VALUE			UNIT
			DW	DWV	D	
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation (ISO772x) and basic electrical insulation (ISO7721B)* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

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6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 8000 V_{PK} (DW-16), 7071 V_{PK} (DWV-8) and 4242 V_{PK} (D-8); Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW-16, DWV-8, Reinforced), 1414 V_{PK} (DW-16, Basic) and 637 V_{PK} (D-8); Maximum surge isolation voltage, 12800 V_{PK} (DW-16, DWV-8, Reinforced), 7800 V_{PK} (DW-16, Basic) and 10000 V_{PK} (D-8)	600 V_{RMS} (DW-16) and 600 V_{RMS} (DWV-8) reinforced insulation and 400 V_{RMS} (D-8) basic insulation working voltage per CSA 62368-1 and IEC 62368-1, (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V_{RMS} (DW-16, DWV-8) max working voltage	DW-16, DWV-8: Single protection, 5000 V_{RMS}; D-8: Single protection, 3000 V_{RMS}	DW-16, DWV-8: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate,700 V_{RMS} maximum working voltage; D-8: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage	5000 V_{RMS} (DW-16, DWV-8) and 3000 V_{RMS} (D-8) Reinforced insulation per EN 61010-1 up to working voltage of 600 V_{RMS} (DW-16, DWV-8) and 300 V_{RMS} (D-8) 5000 V_{RMS} (DW-16, DWV-8) and 3000 V_{RMS} (D-8) Reinforced insulation per EN 62368-1 up to working voltage of 600 V_{RMS} (DW-16, DWV-8) and 400 V_{RMS} (D-8)
Certificate numbers: 40040142 (Reinforced) 40047657 (Basic)	Master contract number: 220991	File number: E181974	Certificate numbers: CQC21001304083 (DW-16) CQC18001199096 (DWV-8) CQC15001121656 (D-8)	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =86.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 6-1			263	mA
		$R_{\theta JA}$ = 86.5°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 6-1			401	
		$R_{\theta JA}$ = 86.5°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 6-1			525	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 86.5°C/W, T_J = 150°C, T_A = 25°C, see Figure 6-2			1445	mW
T_S	Maximum safety temperature				150	°C
DWV-8 PACKAGE						
I_S	Safety input, output, or supply current (1)	$R_{\theta JA}$ =84.3°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 6-3			270	mA
		$R_{\theta JA}$ = 84.3°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 6-3			412	
		$R_{\theta JA}$ = 84.3°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 6-3			539	
P_S	Safety input, output, or total power (1)	$R_{\theta JA}$ = 84.3°C/W, T_J = 150°C, T_A = 25°C, see Figure 6-4			1483	mW
T_S	Maximum safety temperature (1)				150	°C
D-8 PACKAGE						

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Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current (1)	$R_{\theta JA}$ =137.7°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 6-5			165	mA
		$R_{\theta JA}$ = 137.7°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 6-5			252	
		$R_{\theta JA}$ = 137.7°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 6-5			330	
P_S	Safety input, output, or total power (1)	$R_{\theta JA}$ = 137.7°C/W, T_J = 150°C, T_A = 25°C, see Figure 6-6			908	mW
T_S	Maximum safety temperature (1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in Section 6.4 is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4 mA; see Figure 7-1	V_{CCO} - 0.4 (1)	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 7-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CCI}	0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see Figure 7-3	85	100		kV/µs
C_I	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720-Q1							
Supply current - DC signal	V_I = V_{CCI} (1)(ISO7720-Q1), V_I = 0 V (ISO7720-Q1 with F suffix)		I_{CC1}		0.8	1.6	mA
			I_{CC2}		1.1	2	
	V_I = 0V (ISO7720-Q1), V_I = V_{CCI} (ISO7720-Q1 with F suffix)		I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	2.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.8	2.8	
			I_{CC2}		1.3	2.2	
		10 Mbps	I_{CC1}		1.9	2.9	
			I_{CC2}		2.2	3.5	
		100 Mbps	I_{CC1}		2.5	3.7	
			I_{CC2}		11.6	15.7	
ISO7721-Q1							
Supply current - DC signal	V_I = V_{CCI} (1)(ISO7721-Q1); V_I = 0 V (ISO7721-Q1 with F suffix)		I_{CC1}, I_{CC2}		1	2.2	mA
	V_I = 0 V (ISO7721-Q1); V_I = V_{CCI} (ISO7721-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.2	3.4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.7	2.9	
		10 Mbps	I_{CC1}, I_{CC2}		2.2	3.5	
		100 Mbps	I_{CC1}, I_{CC2}		7.3	9.9	

(1) V_{CCI} = Input-side V_{CC}

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6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA ; see Figure 7-1	V_{CCO} - 0.3(1)	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA ; see Figure 7-1		0.1	0.3	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CCI}	0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see Figure 7-3	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720-Q1							
Supply current - DC signal	V_I = V_{CCI} (1) (ISO7720-Q1), V_I = 0 V (ISO7720-Q1 with F suffix)		I_{CC1}		0.8	1.5	mA
			I_{CC2}		1.1	1.9	
	V_I = 0V (ISO7720), V_I = V_{CCI} (ISO7720-Q1 with F suffix)		I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	2.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.8	2.7	
			I_{CC2}		1.2	2.1	
		10 Mbps	I_{CC1}		1.9	2.8	
			I_{CC2}		1.9	3	
		100 Mbps	I_{CC1}		2.2	3.3	
			I_{CC2}		8.6	11.7	
ISO7721-Q1							
Supply current - DC signal	V_I = V_{CCI} (1) (ISO7721-Q1), V_I = 0 V (ISO7721-Q1 with F suffix)		I_{CC1}, I_{CC2}		1	2.1	mA
	V_I = 0 V (ISO7721-Q1), V_I = V_{CCI} (ISO7721-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.2	3.4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.6	2.8	
		10 Mbps	I_{CC1}, I_{CC2}		2	3.2	
		100 Mbps	I_{CC1}, I_{CC2}		5.6	7.8	

(1) V_{CCI} = Input-side V_{CC}

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6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA ; see Figure 7-1	V_{CCO} - 0.2(1)	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA ; see Figure 7-1		0.05	0.2	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CCI}	0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V, see Figure 7-3	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720-Q1							
Supply current - DC signal	V_I = V_{CCI} (1)(ISO7720-Q1), V_I = 0 V (ISO7720-Q1 with F suffix)		I_{CC1}		0.8	1.5	mA
			I_{CC2}		1.1	1.9	
	V_I = 0V (ISO7720-Q1), V_I = V_{CCI} (ISO7720-Q1 with F suffix)		I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	2.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.8	2.7	
			I_{CC2}		1.3	2	
		10 Mbps	I_{CC1}		1.9	2.7	
			I_{CC2}		1.7	2.8	
		100 Mbps	I_{CC1}		2.2	3.1	
			I_{CC2}		6.8	9.4	
ISO7721-Q1							
Supply current - DC signal	V_I = V_{CCI} (1) (ISO7721-Q1); V_I = 0 V (ISO7721-Q1 with F suffix)		I_{CC1}, I_{CC2}		1	2.1	mA
	V_I = 0 V (ISO7721-Q1); V_I = V_{CCI} (ISO7721-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.2	3.3	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.6	2.7	
		10 Mbps	I_{CC1}, I_{CC2}		1.9	3.1	
		100 Mbps	I_{CC1}, I_{CC2}		4.6	6.5	

(1) V_{CCI} = Input-side V_{CC}

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6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1	6	11	17	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time (2)	Same direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 7-1		2.4	3.9	ns
t_f	Output signal fall time			2.4	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1	6	11	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time (2)	Same direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5	ns
t_r	Output signal rise time	See Figure 7-1		0.7	3	ns
t_f	Output signal fall time			0.7	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1	7.5	12	21	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5.5	ns
t_r	Output signal rise time	See Figure 7-1		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.18 Insulation Characteristics Curves

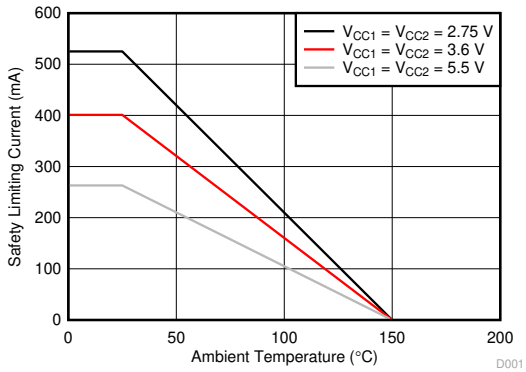

Figure 6-1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

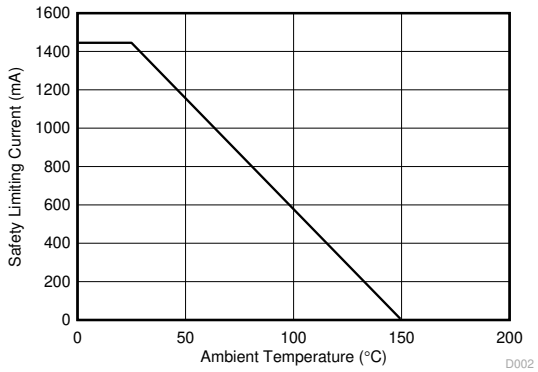

Figure 6-2. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

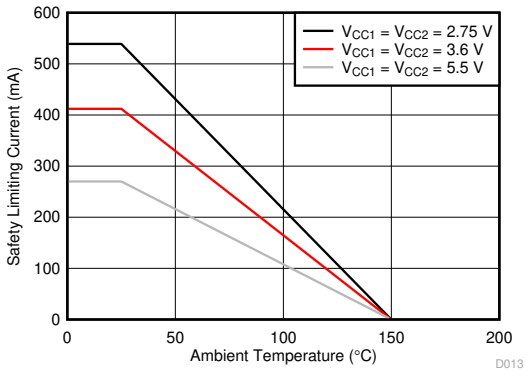

Figure 6-3. Thermal Derating Curve for Limiting Current per VDE for DWV-8 Package

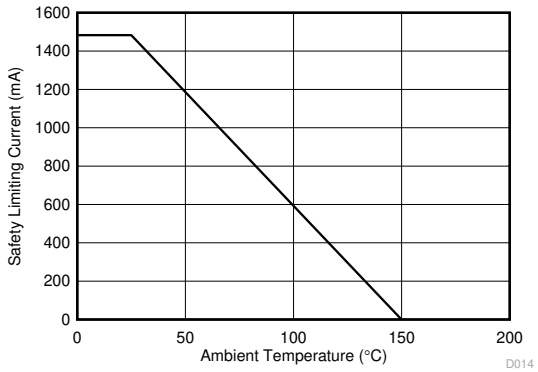

Figure 6-4. Thermal Derating Curve for Limiting Power per VDE for DWV-8 Package

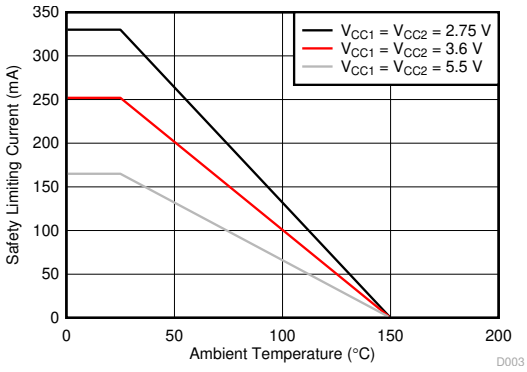

Figure 6-5. Thermal Derating Curve for Limiting Current per VDE for D-8 Package

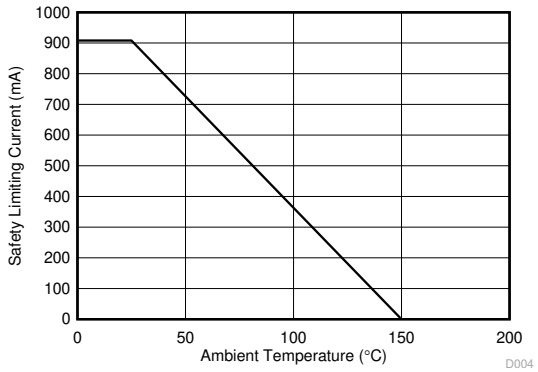

Figure 6-6. Thermal Derating Curve for Limiting Power per VDE for D-8 Package

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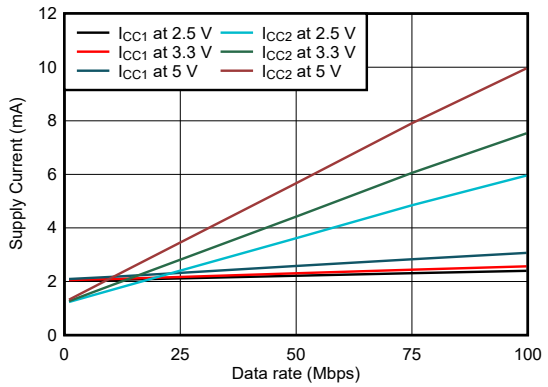
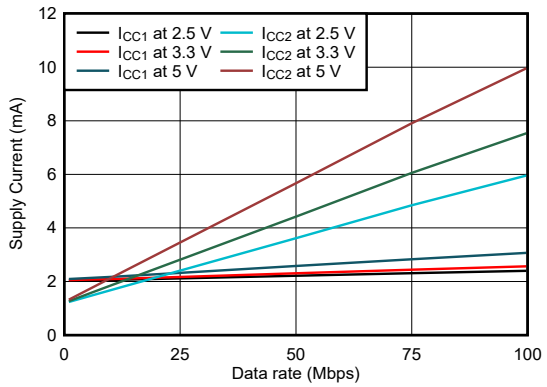
6.19 Typical Characteristics



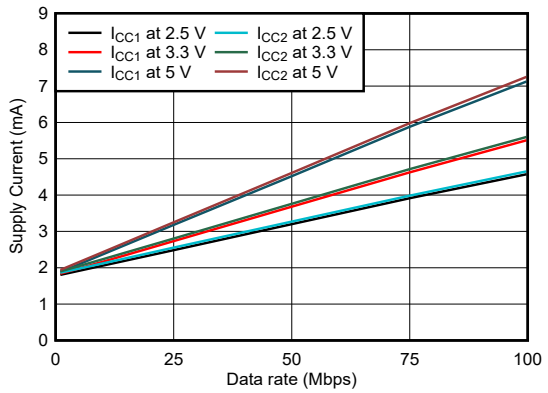
T_A = 25°C C_L = 15 pF

Figure 6-7. ISO7720-Q1 Supply Current vs Data Rate (With 15-pF Load)



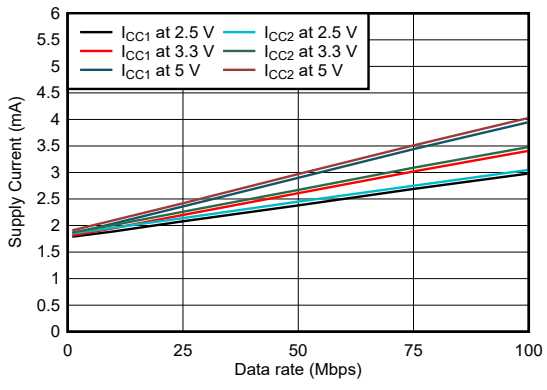
T_A = 25°C C_L = No Load

Figure 6-8. ISO7720-Q1 Supply Current vs Data Rate (With No Load)



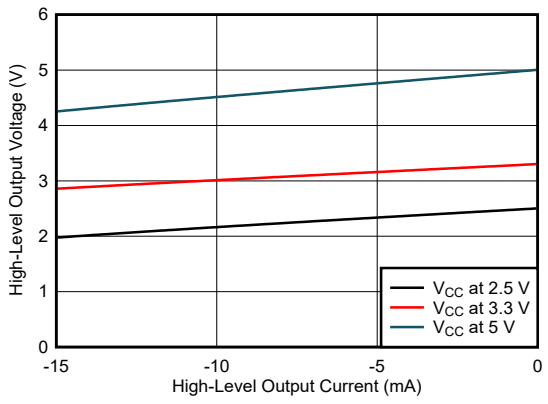
T_A = 25°C C_L = 15 pF

Figure 6-9. ISO7721-Q1 Supply Current vs Data Rate (With 15-pF Load)



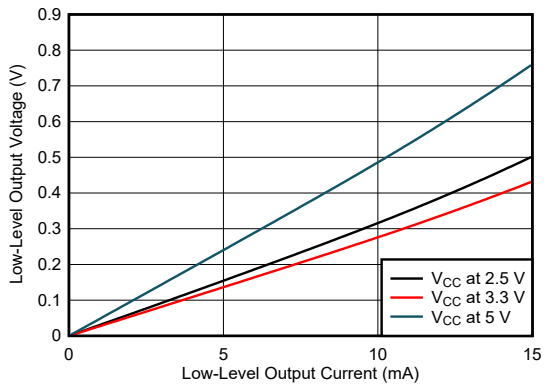
T_A = 25°C C_L = No Load

Figure 6-10. ISO7721-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 6-11. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 6-12. Low-Level Output Voltage vs Low-Level Output Current

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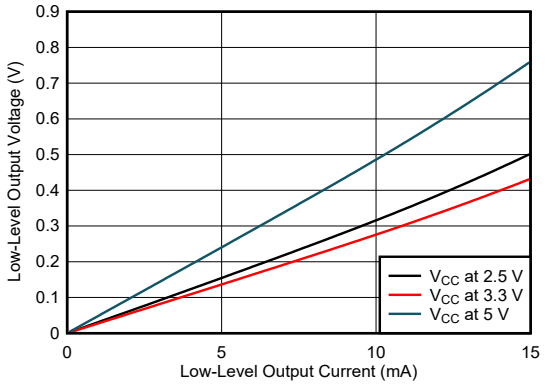


Figure 6-13. Power Supply Undervoltage Threshold vs Free-Air Temperature

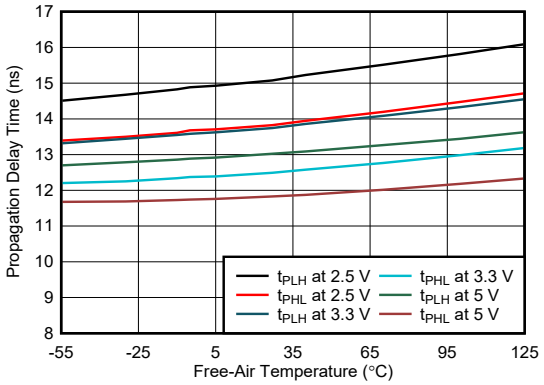
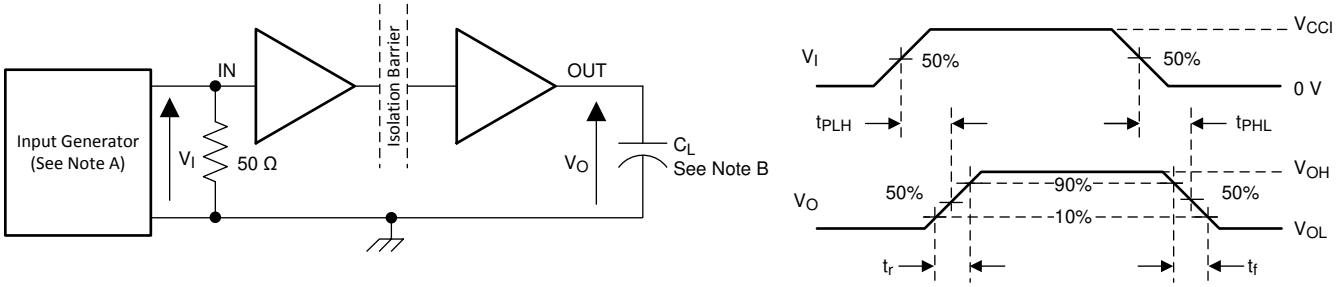


Figure 6-14. Propagation Delay Time vs Free-Air Temperature

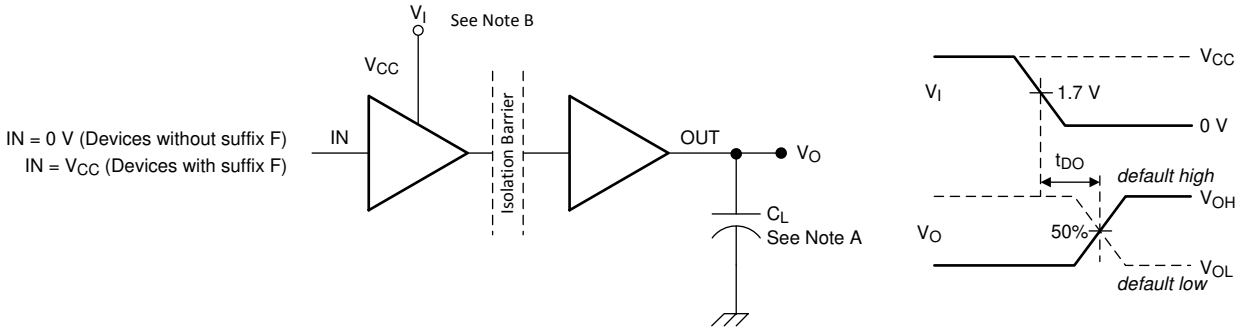
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

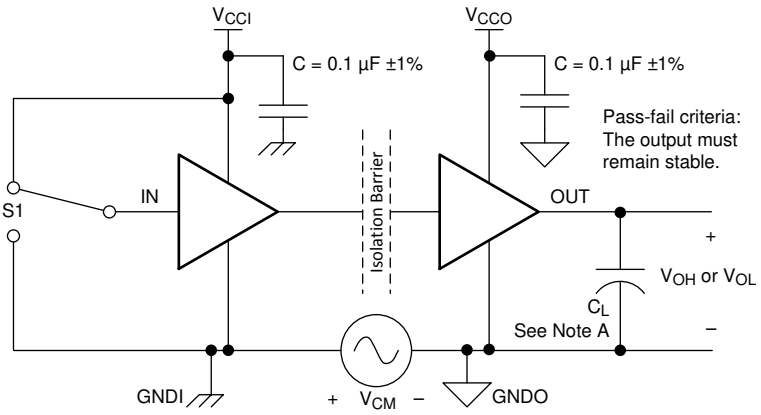
Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

Figure 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 7-3. Common-Mode Transient Immunity Test Circuit

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8 Detailed Description

8.1 Overview

The ISO772x-Q1 family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 8-1, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

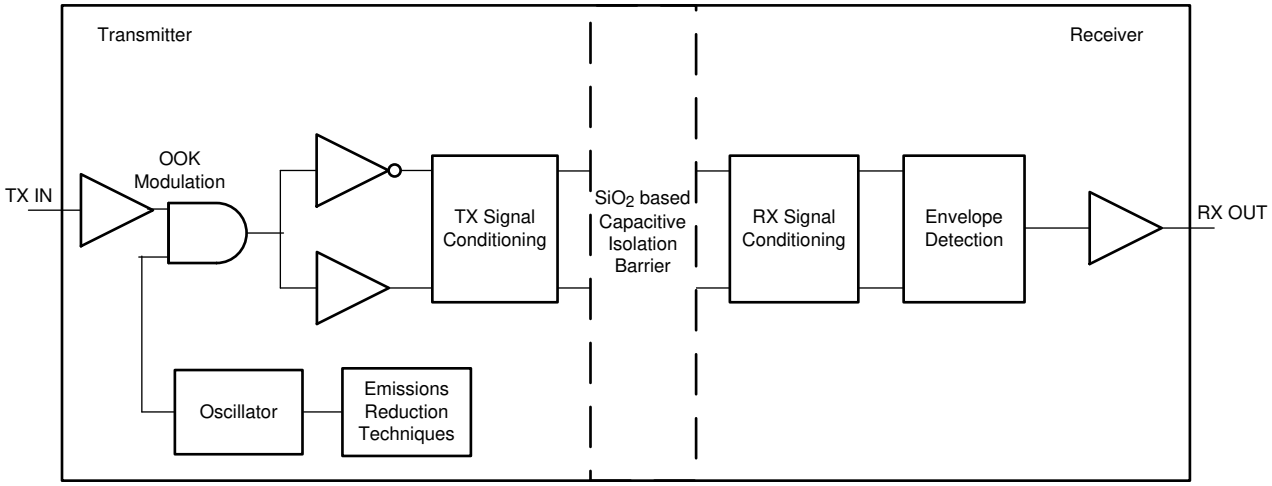

Figure 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 8-2 shows a conceptual detail of how the OOK scheme works.

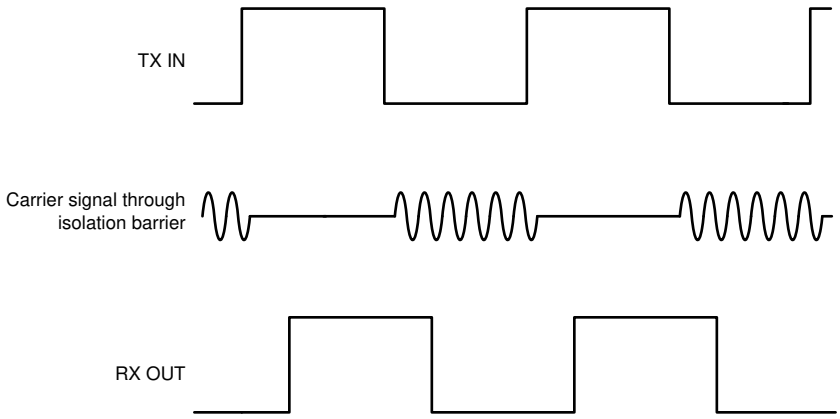

Figure 8-2. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISO772x-Q1 family of devices is available in two channel configurations and default output state options to enable a variety of application uses. Table 8-1 lists the device features of the ISO772x-Q1 devices.

Table 8-1. Device Features

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION(1)
ISO7720-Q1	100 Mbps	2 Forward, 0 Reverse	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DWV-8	5000 V_{RMS} / 7071 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7720-Q1 with F suffix	100 Mbps	2 Forward, 0 Reverse	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DWV-8	5000 V_{RMS} / 7071 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7721-Q1	100 Mbps	1 Forward, 1 Reverse	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DWV-8	5000 V_{RMS} / 7071 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7721-Q1 with F suffix	100 Mbps	1 Forward, 1 Reverse	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DWV-8	5000 V_{RMS} / 7071 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}

(1) See *Section 6.7* section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO772x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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8.4 Device Functional Modes

Table 8-2 lists the functional modes for the ISO772x-Q1 devices.

Table 8-2. Function Table

V_{CCI} (1)	V_{CCO}	INPUT (INx)(3)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. The default is *High* for ISO772x-Q1 and *Low* for ISO772x-Q1 with F suffix.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. The default is *High* for ISO772x-Q1 and *Low* for ISO772x-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level
(2) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.
(3) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.

8.4.1 Device I/O Schematics

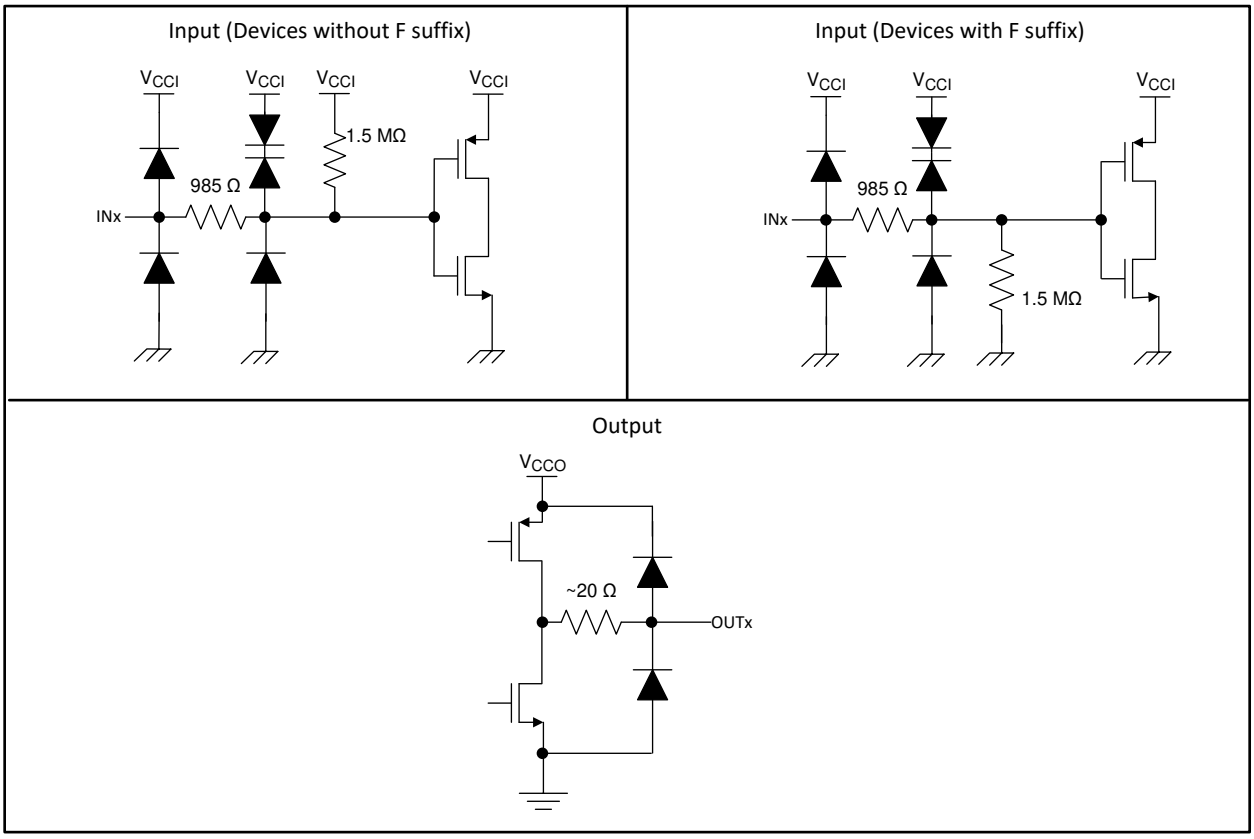

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Figure 8-3. Device I/O Schematics

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ISO772x-Q1 devices are high-performance, dual-channel digital isolators. The devices use single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7721-Q1 device can be used with Texas Instruments' Piccolo™ microcontroller, CAN transceiver, transformer driver, and voltage regulator to create an isolated CAN interface.

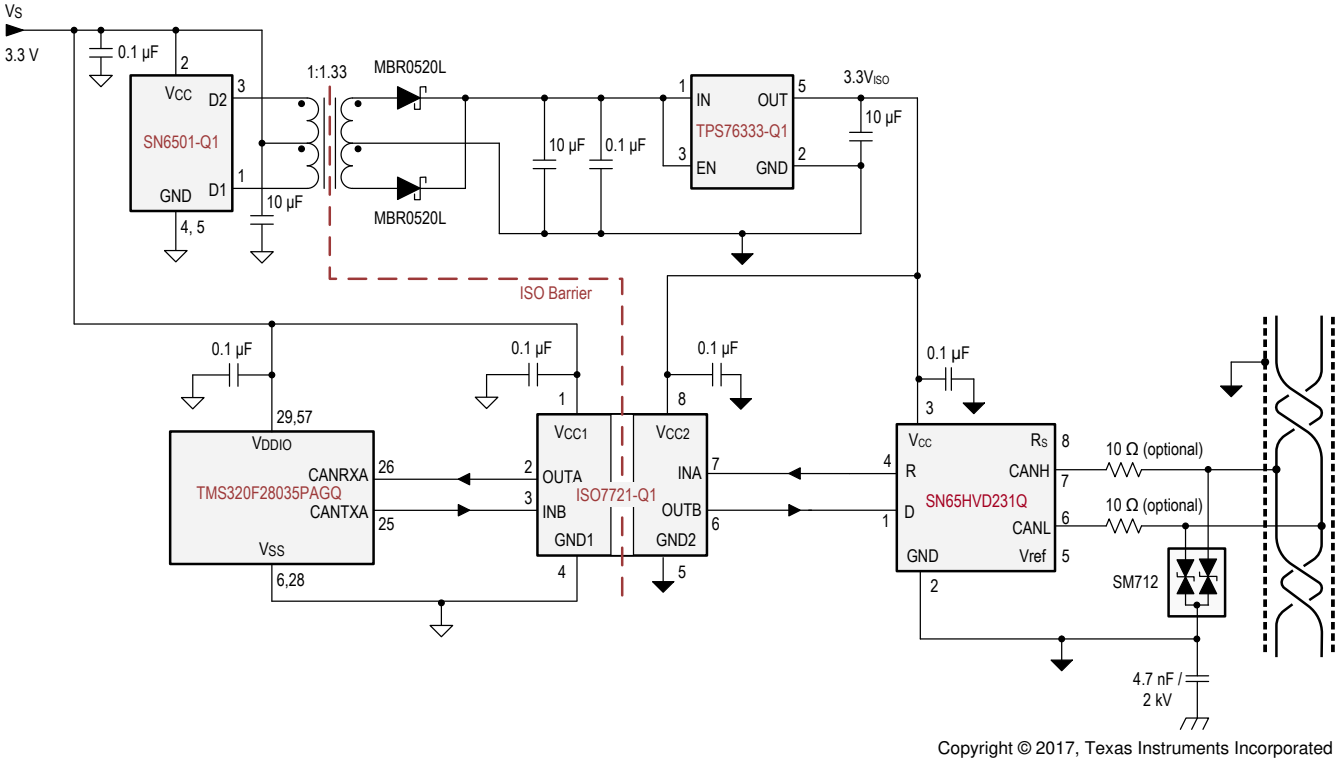

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Figure 9-1. Isolated 4-mA to 20-mA Current Loop

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9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO772x-Q1 devices only require two external bypass capacitors to operate.

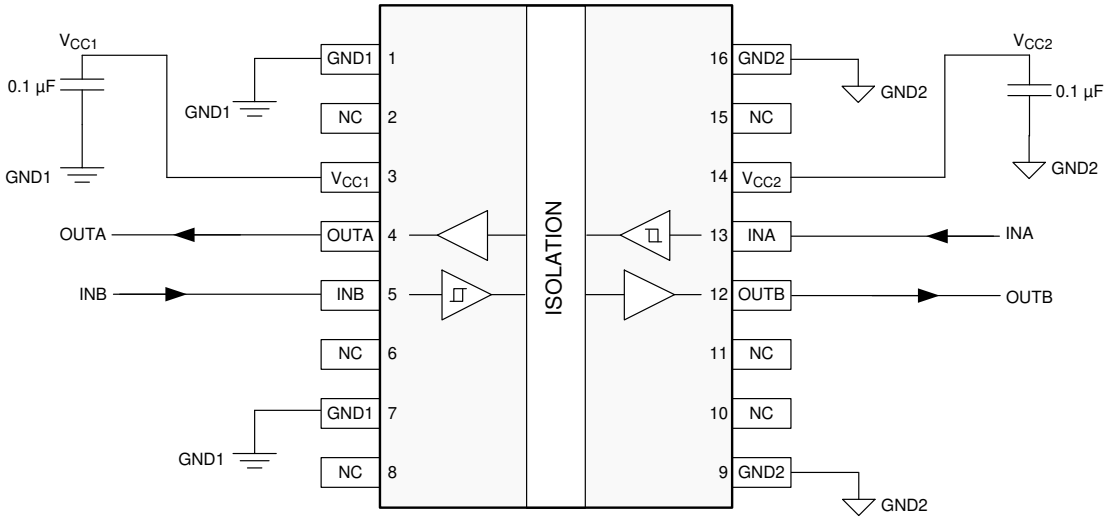

Figure 9-2. Typical ISO7721-Q1 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO772x-Q1 family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

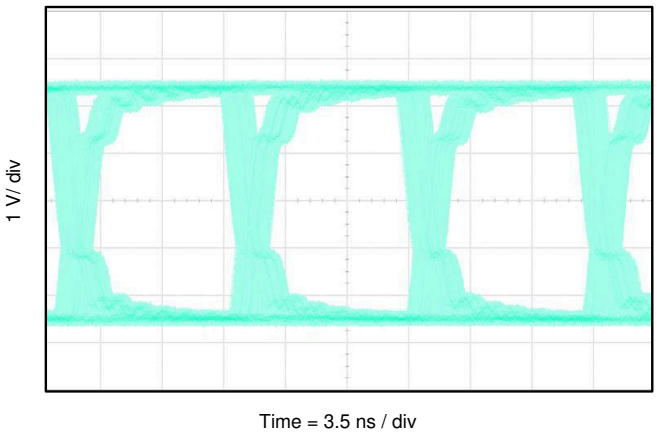

Figure 9-3. ISO7720-Q1 Eye Diagram at 100 Mbps PRBS, 5-V Supplies and 25°C

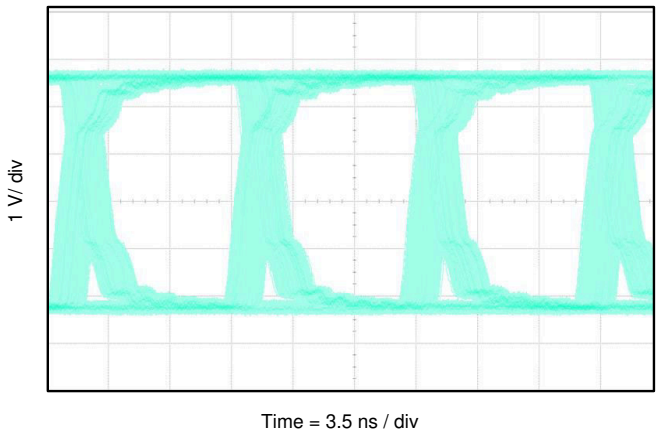

Figure 9-4. ISO7721-Q1 Eye Diagram at 100 Mbps PRBS, 5-V Supplies and 25°C

9.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Test Setup for Insulation Lifetime Measurement for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Insulation Lifetime Projection Data shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 and DWV-8 packages is specified up to 1500 V_{RMS} and D-8 package up to 450 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.

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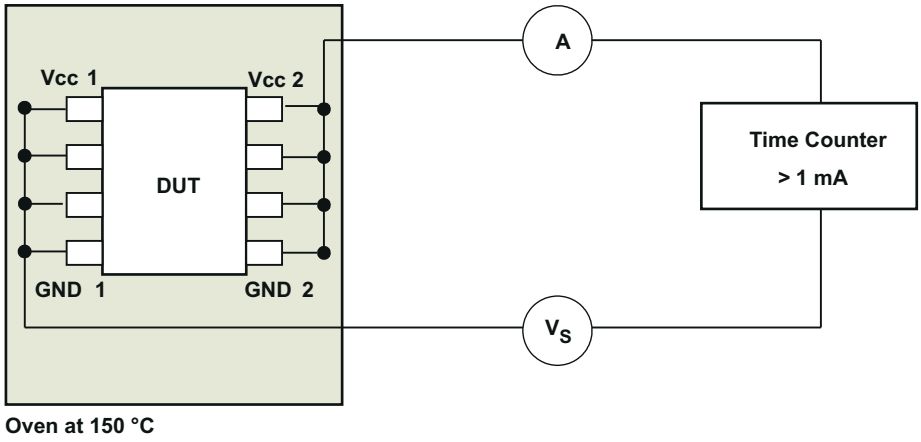

Figure 9-5. Test Setup for Insulation Lifetime Measurement

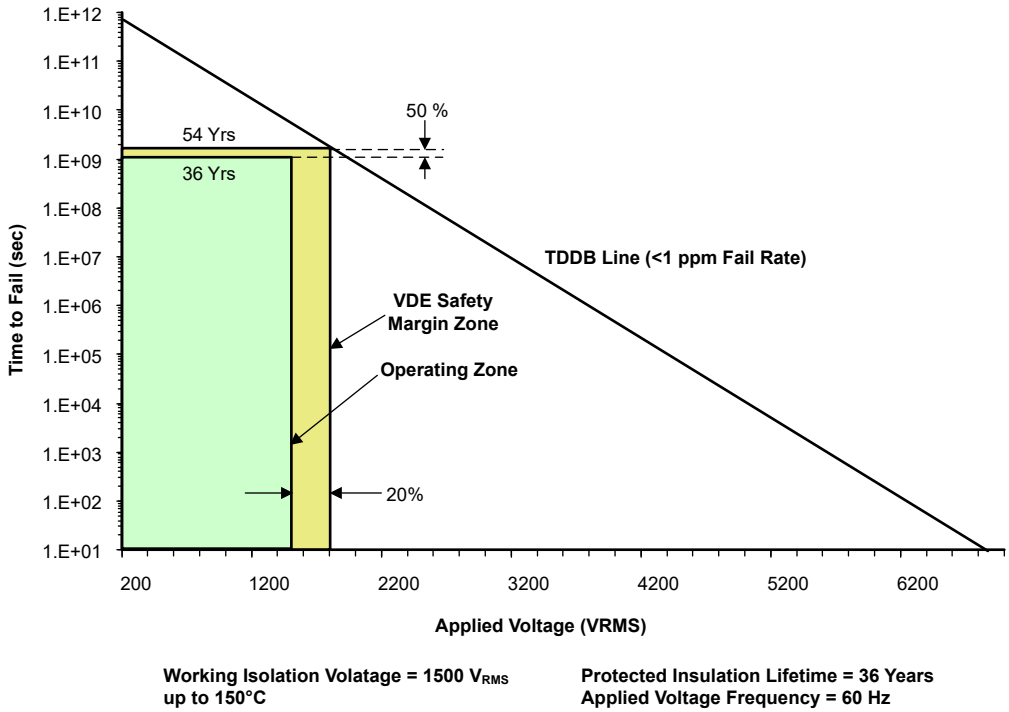

Figure 9-6. Insulation Lifetime Projection Data

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10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies*.

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11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 11-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

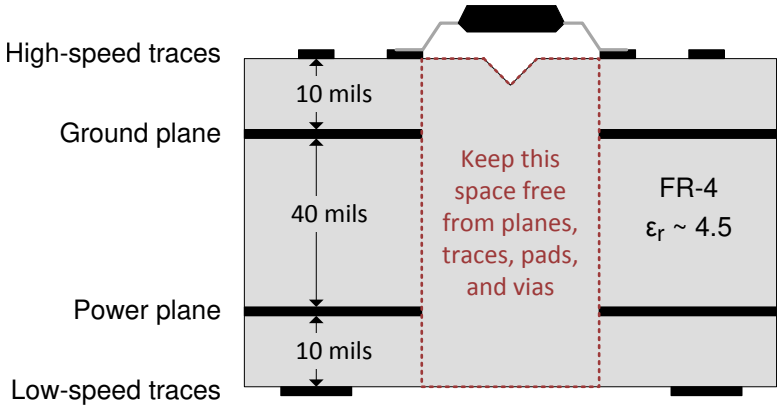

Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For development support, refer to:

- Isolated CAN Flexible Data (FD) Rate Repeater Reference Design
- Isolated 16-Channel AC Analog Input Module Reference Design Using Dual Simultaneously Sampled ADCs
- Polyphase Shunt Metrology with Isolated AFE Reference Design
- Reference Design for Power-Isolated Ultra-Compact Analog Output Module

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *How to use isolation to improve ESD, EFT and Surge immunity in industrial systems* application report
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, SN65HVD231Q *3.3-V CAN Transceivers* data sheet
- Texas Instruments, *TPS763xx-Q1 Low-Power, 150-mA, Low-Dropout Linear Regulators* data sheet
- Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers* data sheet

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7720-Q1	Click here	Click here	Click here	Click here	Click here
ISO7721-Q1	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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12.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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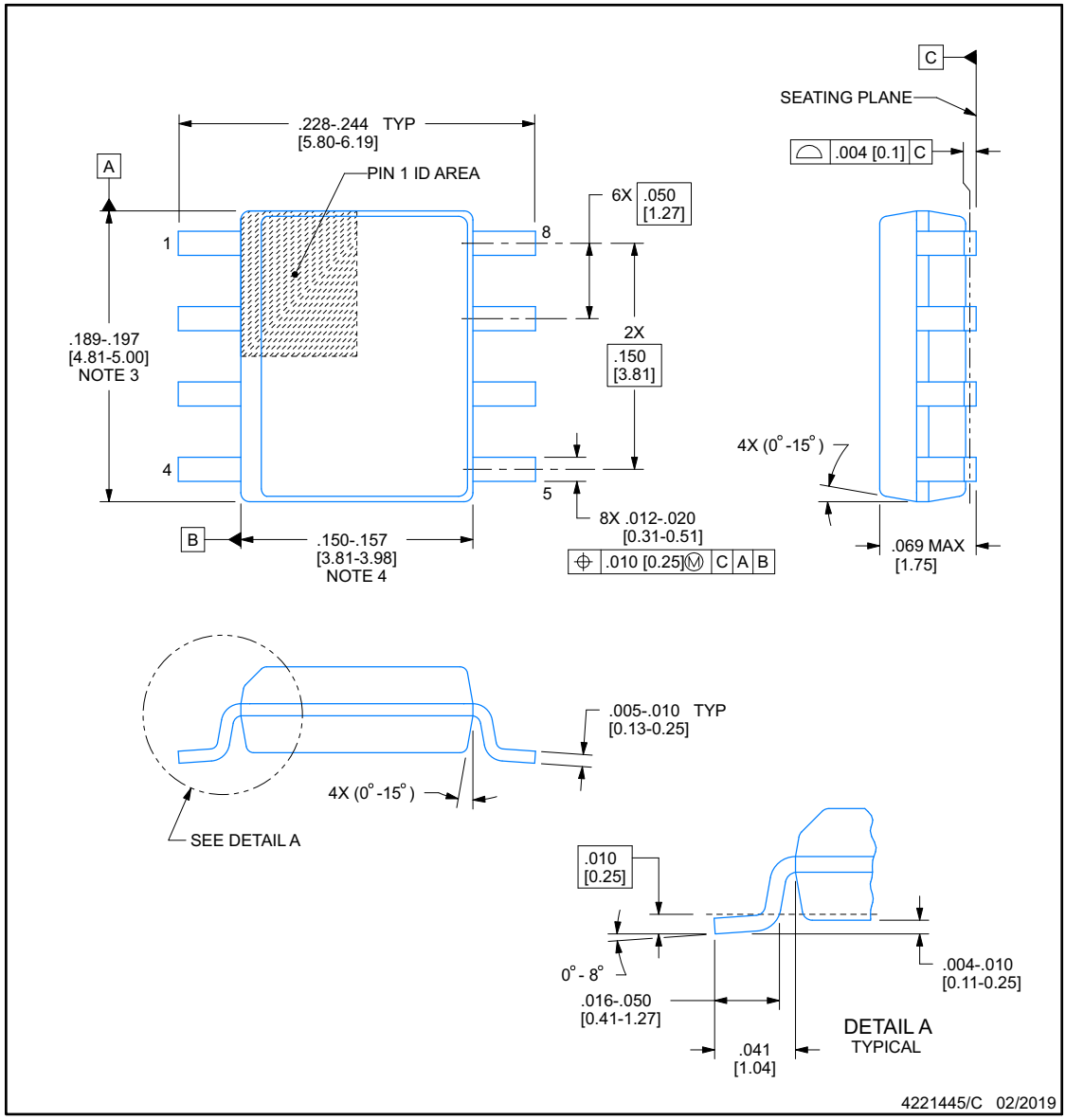
PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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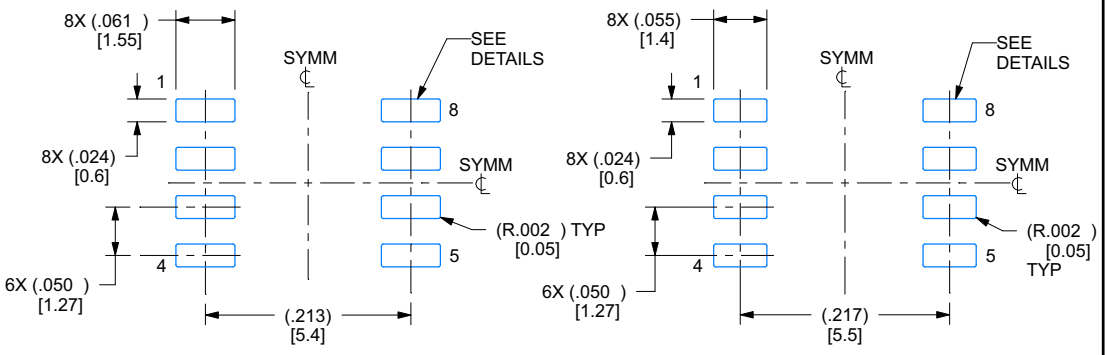
EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

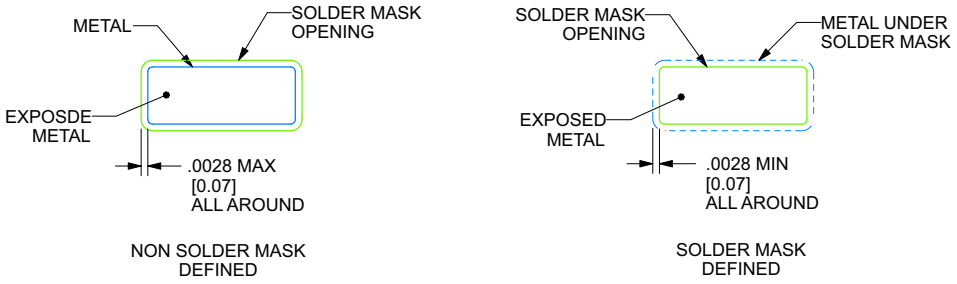
SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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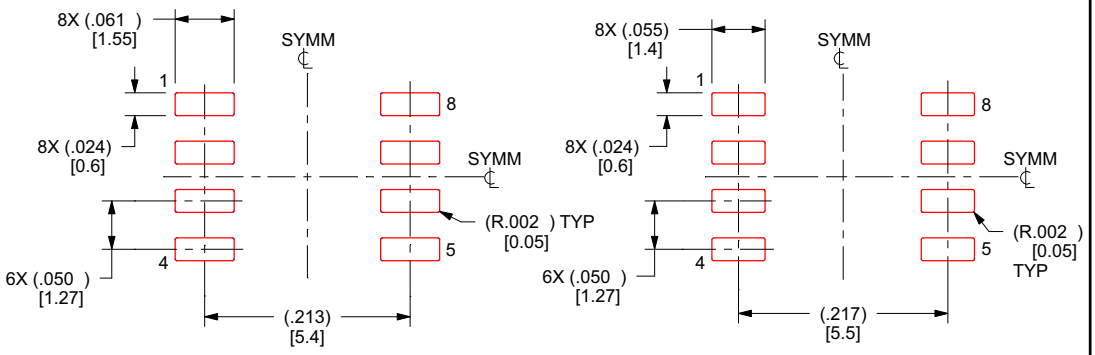
EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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13.1 Package Option Addendum

Packaging Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
ISO7720FQDWVRQ1	PREVIEW	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7720F
ISO7721FQDWVRQ1	PREVIEW	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7721F
ISO7720FQDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7720FQ
ISO7720FQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7720FQ
ISO7720FQDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	ISO7720FQ
ISO7720FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	ISO7720FQ
ISO7720QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7720Q
ISO7720QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7720Q
ISO7720QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	ISO7720Q
ISO7720QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	ISO7720Q
ISO7721FQDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7721FQ
ISO7721FQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7721FQ
ISO7721FQDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	ISO7721FQ
ISO7721FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	ISO7721FQ
ISO7721QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7721Q
ISO7721QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	7721Q
ISO7721QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	ISO7721Q

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Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
ISO7721QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C -1 YEAR	-40 to 125	ISO7721Q

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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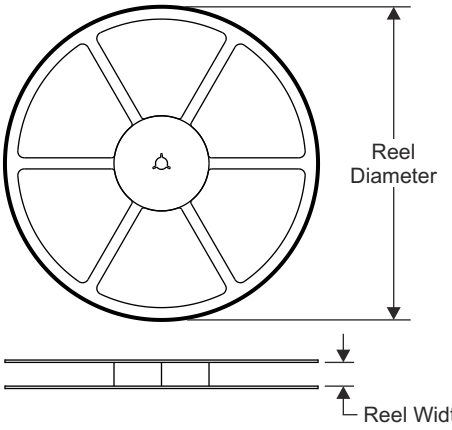
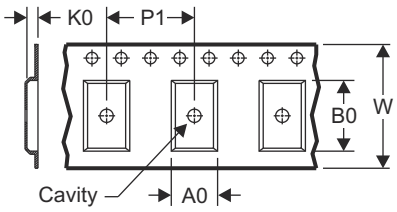
13.2 Tape and Reel Information

REEL DIMENSIONS

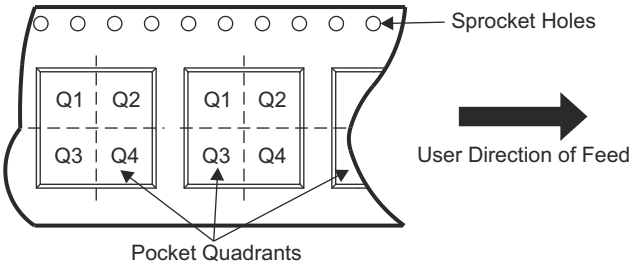


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7720FQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO7721FQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO7720FQDRQ1	SOIC	D	8	2500	330	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720FQDWRQ1	SOIC	DW	16	2000	330	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7720QDRQ1	SOIC	D	8	2500	330	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720QDWRQ1	SOIC	DW	16	2000	330	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721FQDRQ1	SOIC	D	8	2500	330	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721FQDWRQ1	SOIC	DW	16	2000	330	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721QDRQ1	SOIC	D	8	2500	330	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721QDWRQ1	SOIC	DW	16	2000	330	16.4	10.75	10.7	2.7	12.0	16.0	Q1

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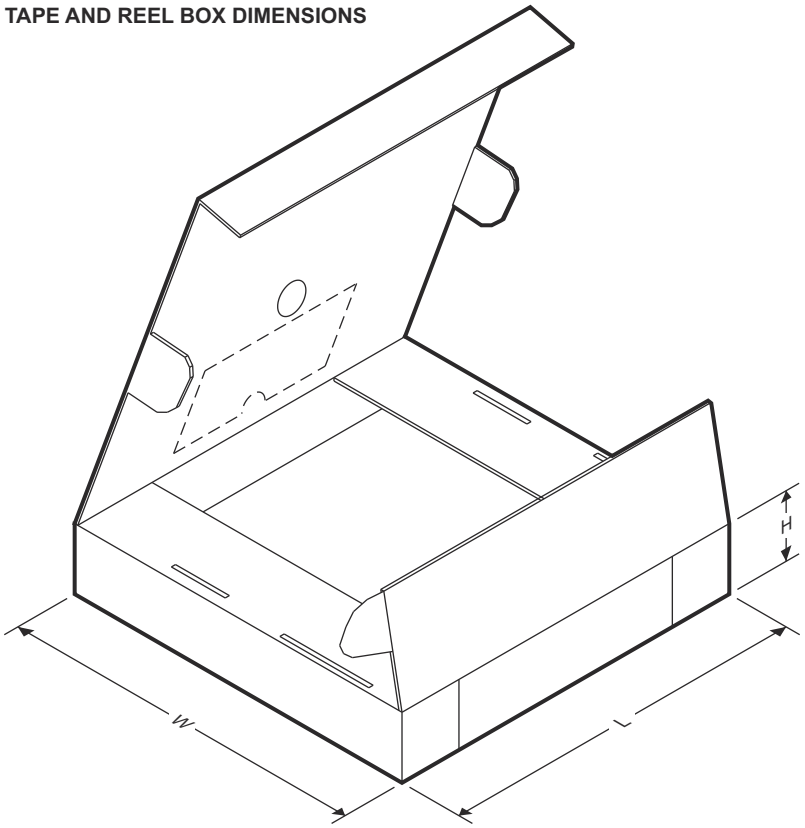
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7720FQDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0
ISO7721FQDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0
ISO7720FQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7720FQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7720QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7720QDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7721FQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7721FQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7721QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7721QDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0

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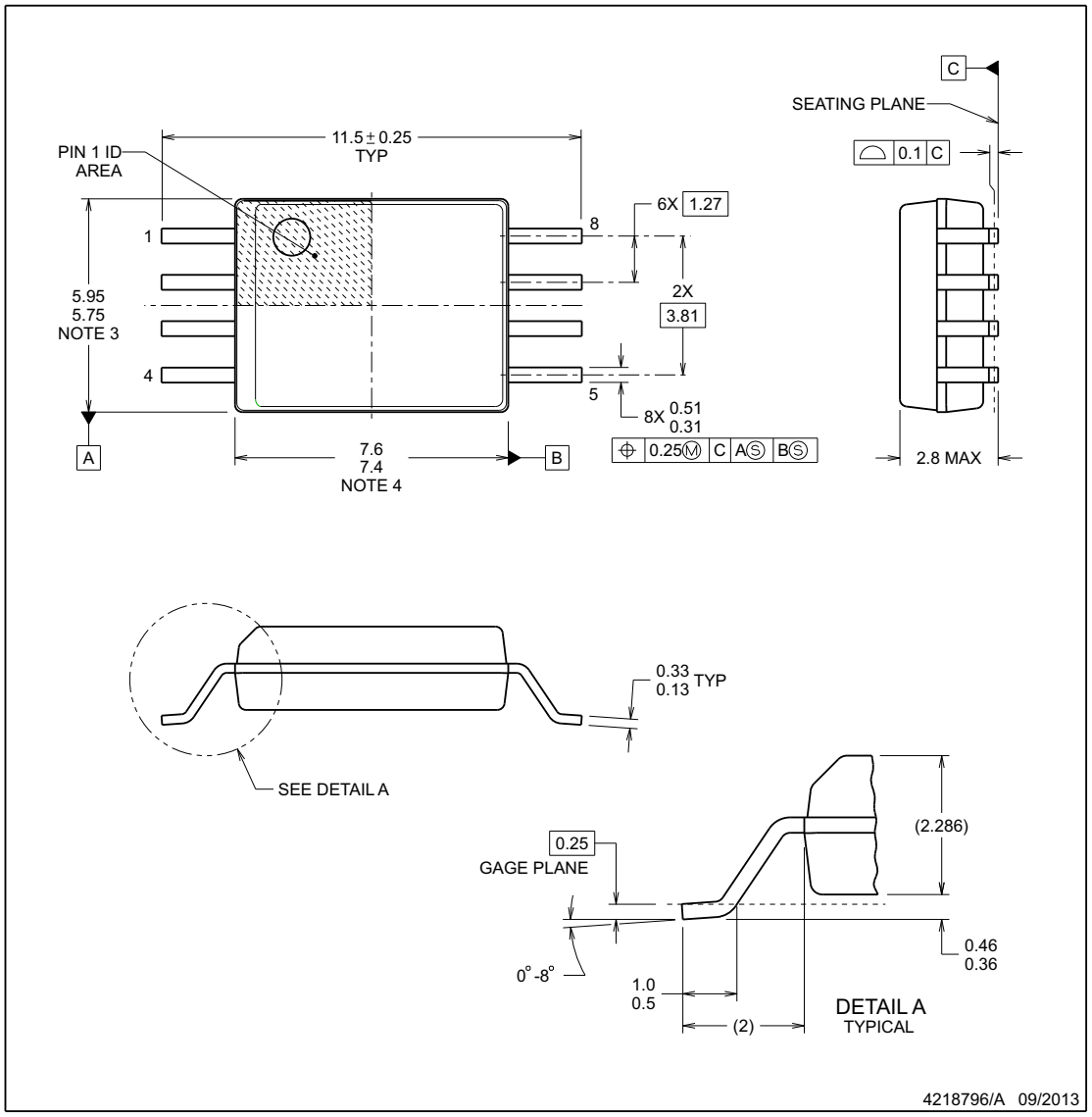
PACKAGE OUTLINE



DWV0008A

SOIC - 2.8 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

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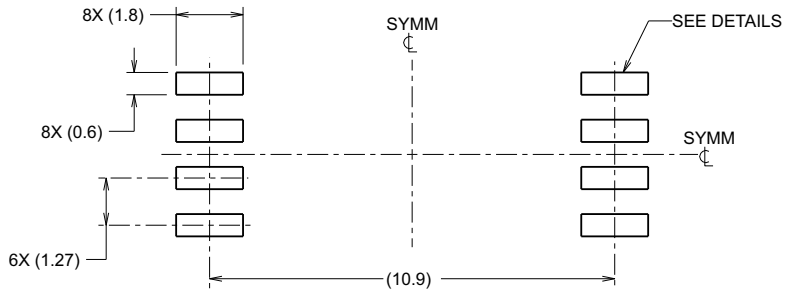
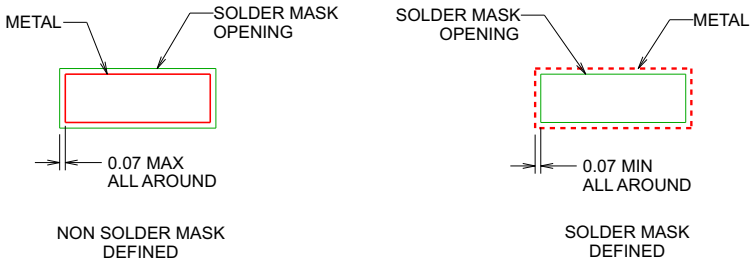
EXAMPLE BOARD LAYOUT

DWV0008A — SOIC - 2.8 mm max height

SOIC



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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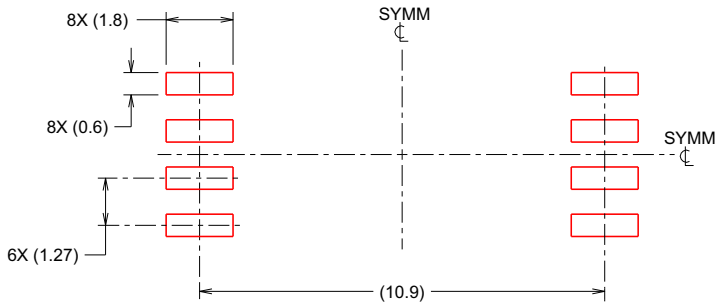
EXAMPLE STENCIL DESIGN

DWV0008A — SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7720FQDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7720FQ	Samples
ISO7720FQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7720FQ	Samples
ISO7720FQDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7720FQ	Samples
ISO7720FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7720F, ISO7720 FQ)	Samples
ISO7720QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7720Q	Samples
ISO7720QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7720Q	Samples
ISO7720QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7720Q	Samples
ISO7720QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7720, ISO7720Q)	Samples
ISO7721FQDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7721FQ	Samples
ISO7721FQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7721FQ	Samples
ISO7721FQDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7721FQ	Samples
ISO7721FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7721FQ	Samples
ISO7721QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7721Q	Samples
ISO7721QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7721Q	Samples
ISO7721QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7721Q	Samples
ISO7721QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7721Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ISO7720-Q1, ISO7721-Q1 :

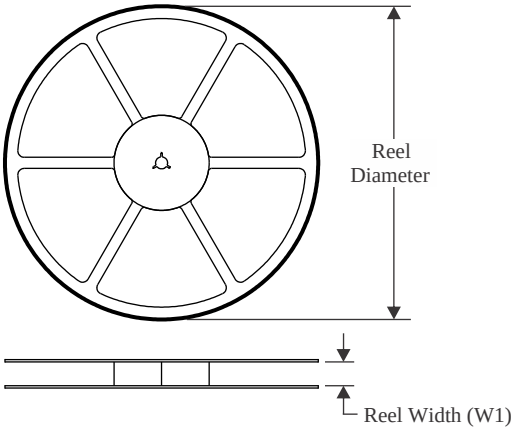
- Catalog : ISO7720, ISO7721

NOTE: Qualified Version Definitions:

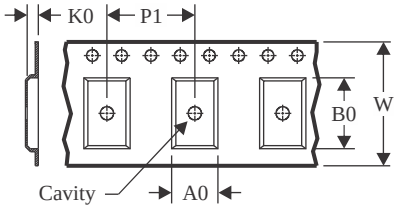
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

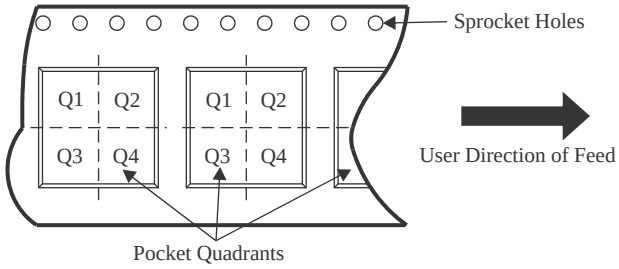


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

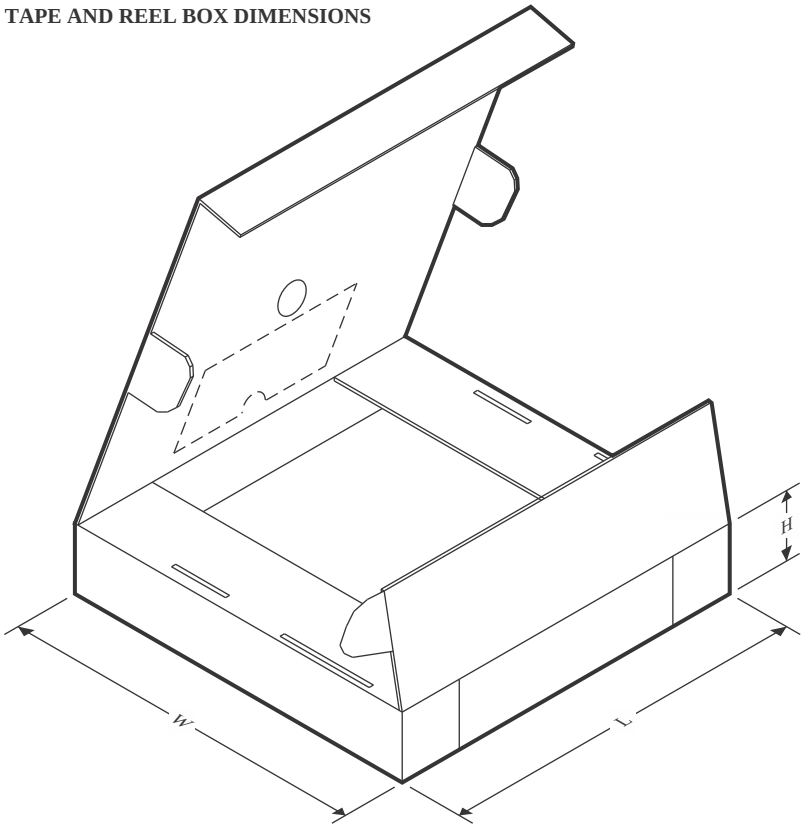
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7720FQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720FQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7720QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721FQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721FQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

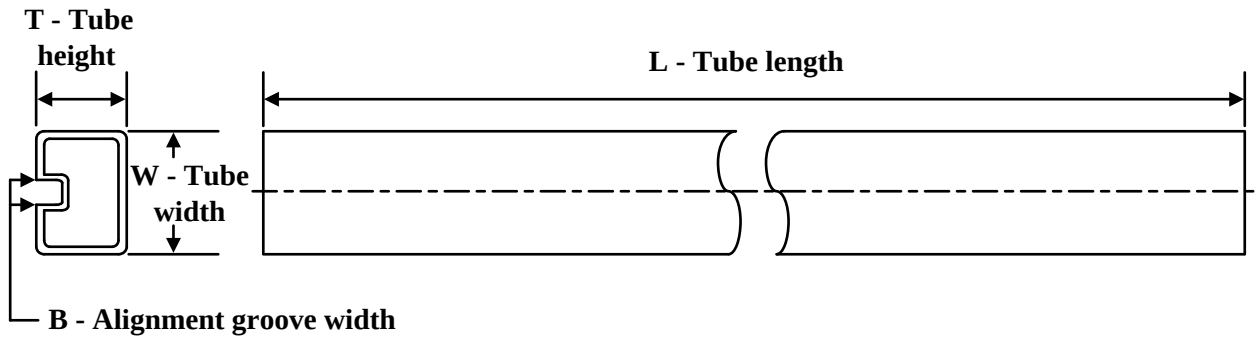
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7720FQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7720FQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7720FQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7720QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7720QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7720QDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7721FQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7721FQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7721FQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7721QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7721QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7721QDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7720FQDQ1	D	SOIC	8	75	505.46	6.76	3810	4
ISO7720FQDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7720QDQ1	D	SOIC	8	75	505.46	6.76	3810	4
ISO7720QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7721FQDQ1	D	SOIC	8	75	505.46	6.76	3810	4
ISO7721FQDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7721QDQ1	D	SOIC	8	75	505.46	6.76	3810	4
ISO7721QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

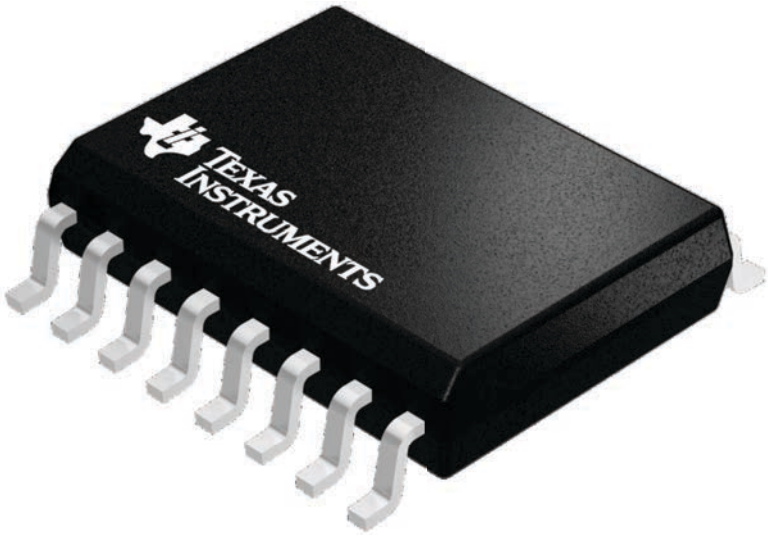
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

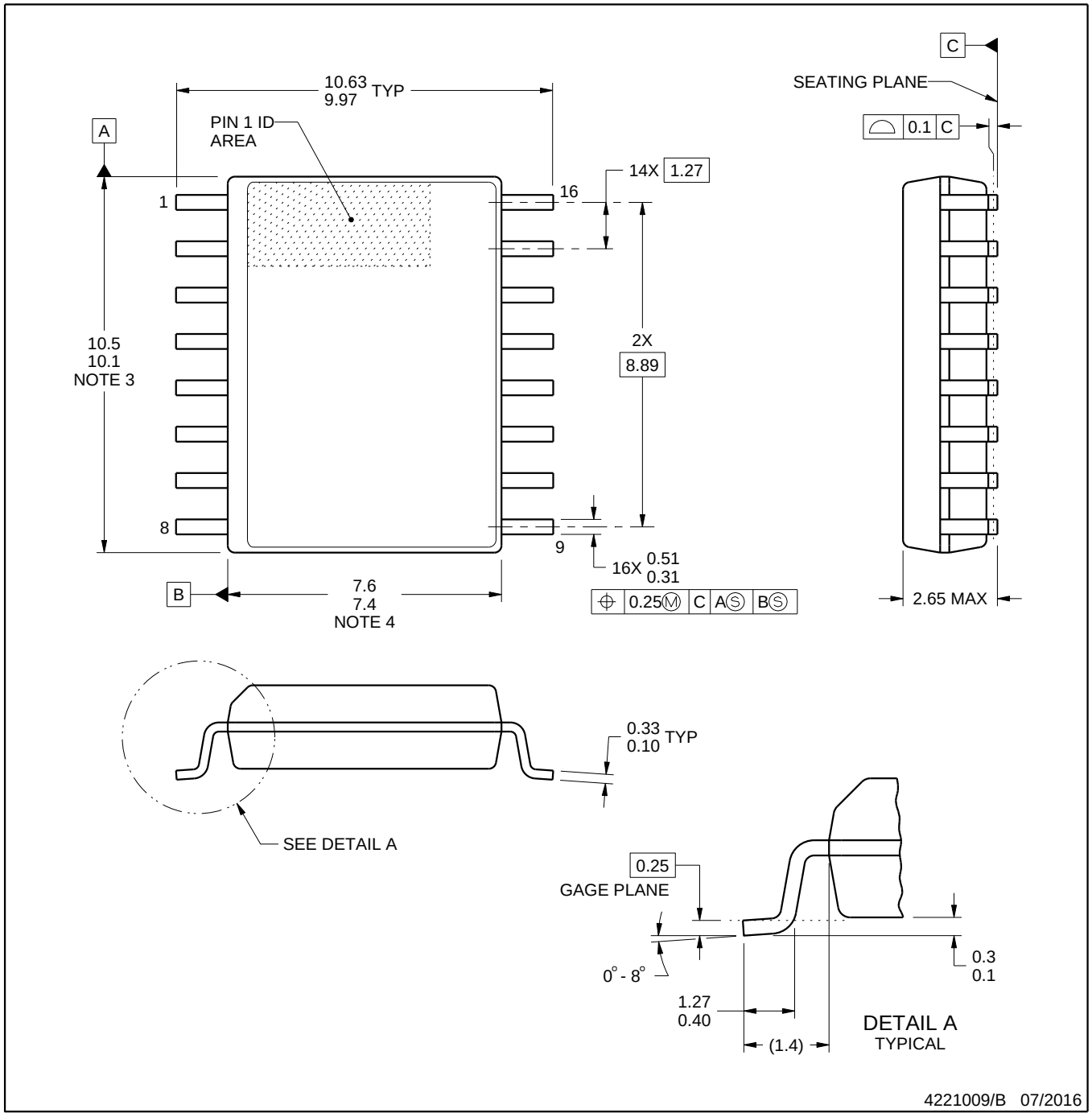
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



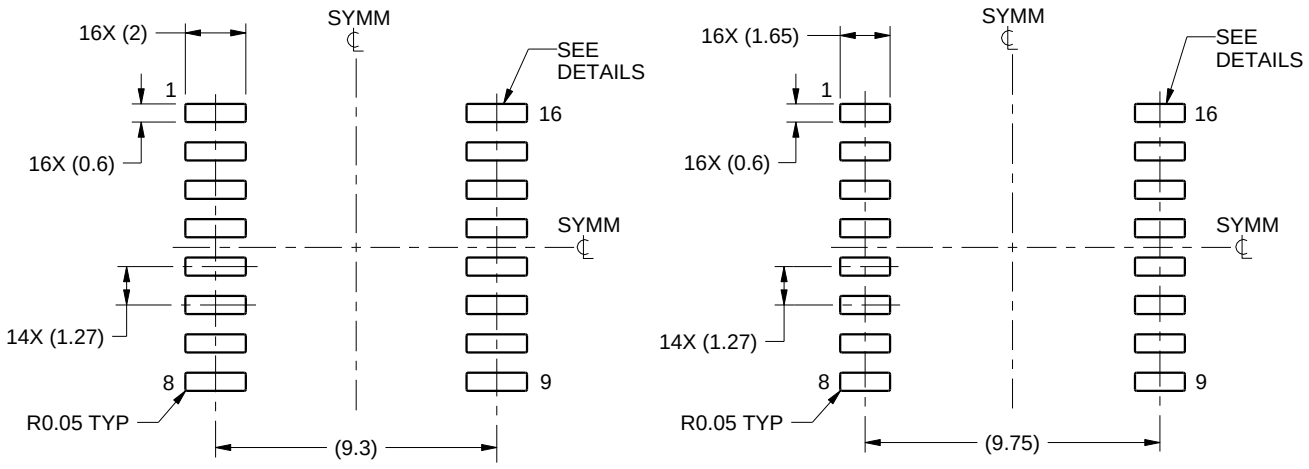
4224780/A

SOIC



NOTES:

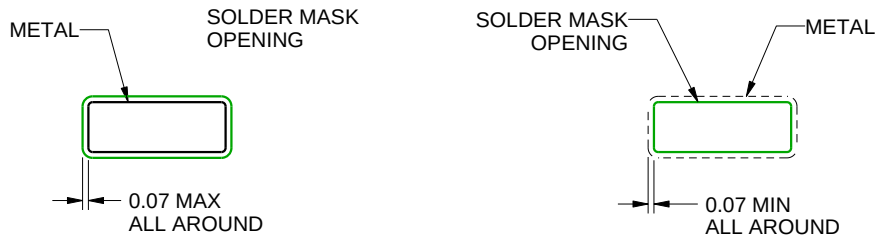
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

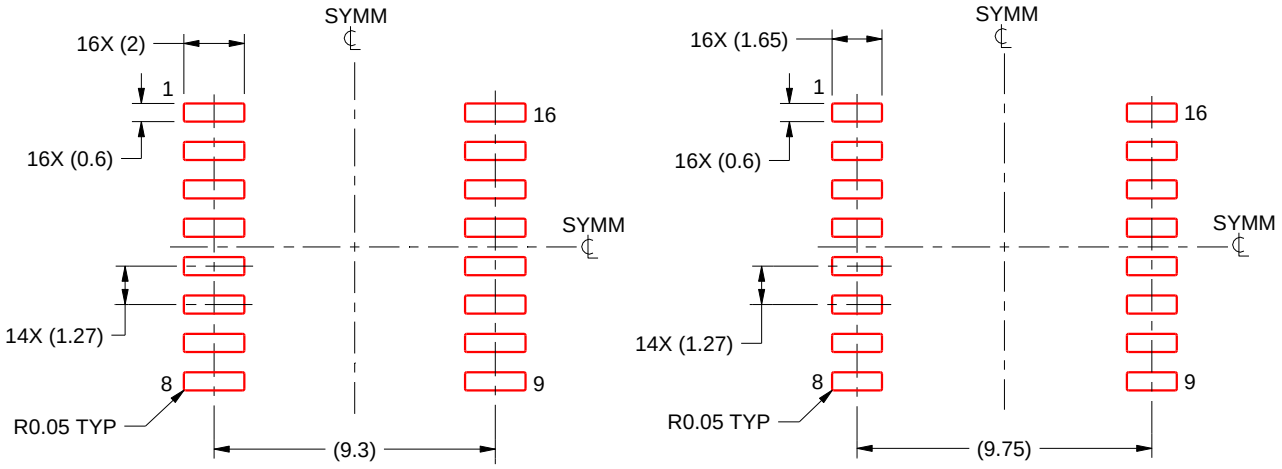
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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