TEXAS INSTRUMENTS

ISO1410, ISO1412, ISO1430, ISO1432
ISO1450, ISO1452

SLLSF22G – APRIL 2018 – REVISED JUNE 2020

ISO14xx 5-kV$_{RMS}$ Isolated RS-485/RS-422 Transceiver with Robust EMC

1 Features

- Compatible with TIA/EIA-485-A
- PROFIBUS compatible at 5-V bus-side supply
- Bus I/O protection
  - ± 30 kV HBM
  - ±16 kV IEC 61000-4-2 Contact discharge
  - ± 4 kV IEC 61000-4-4 Electrical fast transient
- Low-EMI 500-kbps, 12 Mbps and 50 Mbps Data Rates
- 1.71-V to 5.5-V logic-side supply (V_{CC1}), 3-V to 5.5-V bus-side supply (V_{CC2})
- Failsafe receiver for bus open, short, and idle
- 1/8 Unit load up to 256 nodes on bus
- 100-kV/µs (typical) high common-mode transient immunity
- Extended temperature range from –40°C to +125°C
- Glitch-free power-up and power-down for hot plug-in
- Wide-body SOIC-16 package
- Pin compatible to most isolated RS-485 transceivers
- Safety-related certifications:
  - 7071-V_{PK} V_{IOTM} and 1500-V_{PK} V_{IORM} (reinforced and basic options) per DIN VDE V 0884-11:2017-01
  - 5000-V_{RMS} isolation for 1 minute per UL 1577
  - IEC 60950-1, IEC 62368-1, IEC 60601-1 and IEC 61010-1 certifications
  - CQC, TUV, and CSA approvals

2 Applications

- Grid infrastructure
- Solar inverter
- Factory automation & control
- Motor drives
- HVAC systems and building automation

3 Description

The ISO14xx devices are galvanically-isolated differential line transceivers for TIA/EIA RS-485 and RS-422 applications. These noise-immune transceivers are designed to operate in harsh industrial environments. The bus pins of these devices can endure high levels of IEC electrostatic discharge (ESD) and IEC electrical fast transient (EFT) events which eliminates the need for additional components on bus for system-level protection. The devices are available for both basic and reinforced isolation (see *Reinforced and Basic Isolation Options*).

Device Information[1]

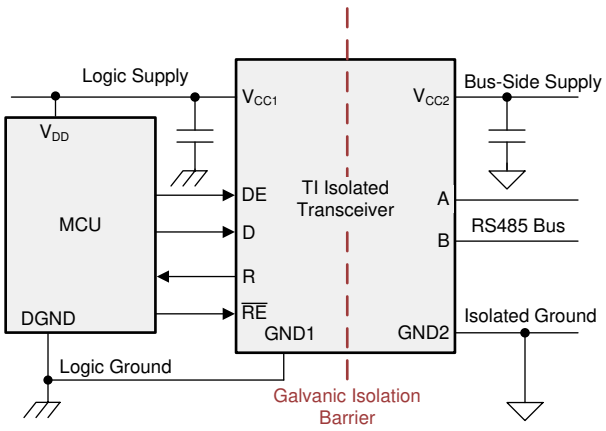
PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO1410, ISO1410B	SOIC (16)	10.30 mm × 7.50 mm
ISO1412, ISO1412B		
ISO1430, ISO1430B		
ISO1432, ISO1432B		
ISO1450, ISO1450B		
ISO1452, ISO1452B		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Reinforced and Basic Isolation Options

Feature	ISO14xx	ISO14xxB
Protection level	Reinforced	Basic
Surge test voltage per VDE	10000 V_{PK}	6000 V_{PK}
Isolation rating per UL	5000 V_{RMS}	5000V_{RMS}
Working voltage per VDE	1060 V_{RMS} / 1500 V_{PK}	1060 V_{RMS} / 1500 V_{PK}

Simplified Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (February 2020) to Revision G — **Page**

- Added minimum driver rise/fall time specification of 240 ns to 8.13 Switching characteristics: Driver (500kbps devices).. 15

Changes from Revision E (October 2019) to Revision F — **Page**

- Added updated certification information in Safety-Related Certifications ... 10

Changes from Revision D (May 2019) to Revision E — **Page**

- Added footnote to Pin functions table for NC pins ... 5

Changes from Revision C (April 2019) to Revision D — **Page**

- Added B part numbers throughout datasheet ... 1

Changes from Revision B (November 2018) to Revision C — **Page**

- Added ISO1430, ISO1432, ISO1450, ISO1452 in Device Information table ... 1
- Changed the position of Device Features tabels ... 4
- Added footnote to Pin Functions: Full-Duplex Device ... 5
- Added footnote to Pin Functions: Half-Duplex Device ... 6
- Added Typical curves for ISO143x and ISO145x in *Typical Characteristics* ... 17

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- Added Section 11.2.3 Application Curves and Section 11.2.3.1 Insulation Lifetime 33

Changes from Revision A (August 2018) to Revision B **Page**

- Changed status to production data 1

Changes from Original (July 2018) to Revision A **Page**

- Changed the designator of common mode voltage in Recommended operating condition to V_I 7
- Added test condition for CMTI in Electrical characteristics: Driver 11
- Added test condition for CMTI in Electrical characteristics: Receiver 12
- Changed V_{TEST} to V_{CM} in the *Common Mode Transient Immunity (CMTI)—Full Duplex* and *Common Mode Transient Immunity (CMTI)—Half Duplex* figures in the *Parameter Measurement Information* section 23
- Changed t_{PLH} to t_{PZH} and t_{PLZ} to t_{PHZ} in the first *Driver Enable and Disable Times* timing diagram in the *Parameter Measurement Information* section 24
- Added t_{PHZ} to the first *Receiver Enable and Disable Times* timing diagram in the *Parameter Measurement Information* section 25

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5 Description Continued

These devices are used for long distance communications. Isolation breaks the ground loop between the communicating nodes, allowing for a much larger common mode voltage range. The symmetrical isolation barrier of each device is tested to provide 5000 V_{RMS} of isolation for 1 minute per UL 1577 between the bus-line transceiver and the logic-level interface.

The ISO14xx devices can operate from 1.71 V to 5.5 V on side 1 which lets the devices be interfaced with low voltage FPGAs and ASICs. The wide supply voltage on side 2 from 3 V to 5.5 V eliminates the need for a regulated supply voltage on the isolated side. These devices support a wide operating ambient temperature range from –40°C to +125°C.

6 Device Options

Table 1 shows an overview of the options available for this family of devices.

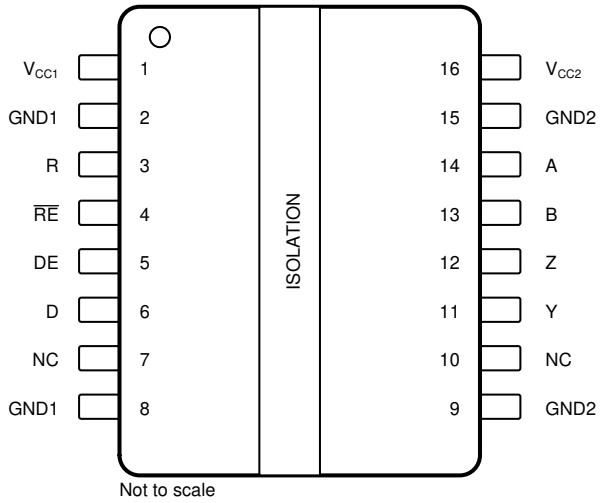
Table 1. Device Features

PART NUMBER	ISOLATION	DUPLEX	DATA RATE	PACKAGE
ISO1410, ISO1410B	Reinforced, Basic	Half	500 Kbps	16-pin DW
ISO1412, ISO1412B		Full	500 Kbps	16-pin DW
ISO1430, ISO1430B		Half	12 Mbps	16-pin DW
ISO1432, ISO1432B		Full	12 Mbps	16-pin DW
ISO1450, ISO1450B		Half	50 Mbps	16-pin DW
ISO1452, ISO1452B		Full	50 Mbps	16-pin DW

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7 Pin Configuration and Functions

DW Package
16-Pin SOIC
Full-Duplex Device Top View



Not to scale

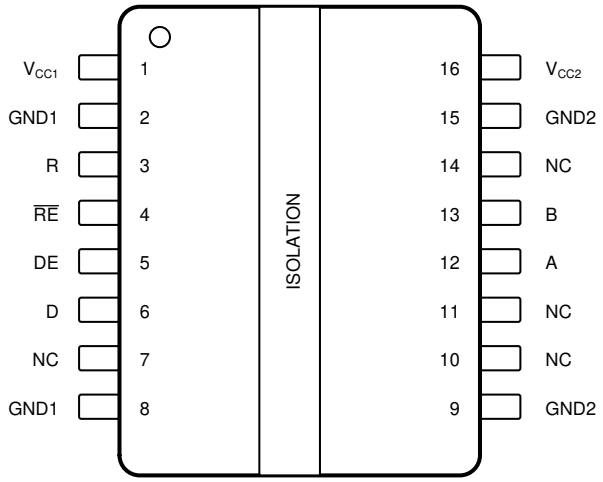
Pin Functions: Full-Duplex Device

PIN		I/O	DESCRIPTION
NAME	NO.		
A	14	I	Receiver non-inverting input on the bus side
B	13	I	Receiver inverting input on the bus side
D	6	I	Driver input
DE	5	I	Driver enable. This pin enables the driver output when high and disables the driver output when low or open.
GND1 (1)	2	—	Ground connection for V_{CC1}
GND1 (1)	8	—	Ground connection for V_{CC1}
GND2 (1)	9	—	Ground connection for V_{CC2}
GND2 (1)	15	—	Ground connection for V_{CC2}
NC (2)	7	—	No internal connection
NC (2)	10	—	No internal connection
R	3	O	Receiver output
$\overline{RE}$	4	I	Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low.
V_{CC1}	1	—	Logic-side power supply
V_{CC2}	16	—	Transceiver-side power supply
Y	11	O	Driver non-inverting output
Z	12	O	Driver inverting output

(1) For Logic side, both Pin 2 and Pin 8 must be connected to GND1. For Bus side, both Pin 9 and Pin 15 must be connected to GND2.
(2) Device functionality is not affected if NC pins are connected to supply or ground on PCB

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DW Package
16-Pin SOIC
Half-Duplex Device Top View



Not to scale

Pin Functions: Half-Duplex Device

PIN		I/O	DESCRIPTION
NAME	NO.		
A	12	I/O	Transceiver non-inverting input or output (I/O) on the bus side
B	13	I/O	Transceiver inverting input or output (I/O) on the bus side
D	6	I	Driver input
DE	5	I	Driver enable. This pin enables the driver output when high and disables the driver output when low or open.
GND1 (1)	2	—	Ground connection for V_{CC1}
GND1 (1)	8	—	Ground connection for V_{CC1}
GND2 (1)	9	—	Ground connection for V_{CC2}
GND2 (1)	15	—	Ground connection for V_{CC2}
NC (2)	7	—	No internal connection
NC (2)	10	—	No internal connection
NC (2)	11	—	No internal connection
NC (2)	14	—	No internal connection
R	3	O	Receiver output
$\overline{RE}$	4	I	Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low.
V_{CC1}	1	—	Logic-side power supply
V_{CC2}	16	—	Transceiver-side power supply

(1) For Logic side, both Pin 2 and Pin 8 must be connected to GND1. For Bus side, both Pin 9 and Pin 15 must be connected to GND2.
(2) Device functionality is not affected if NC pins are connected to supply or ground on PCB

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8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{CC1}	Supply voltage, side 1	-0.5	6	V
V_{CC2}	Supply voltage, side 2	-0.5	6	V
V_{IO}	Logic voltage level (D, DE, $\overline{RE}$, R)	-0.5	V_{CC1}+0.5(3)	V
I_O	Output current on R pin	-15	15	mA
V_{BUS}	Voltage on bus pins (A, B, Y, Z w.r.t GND2)	-18	18	V
T_J	Junction temperature	-40	150	℃
T_{STG}	Storage temperature	-65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Contact Discharge, per IEC 61000-4-2	Pins Bus terminals and GND2	±16000	V
$V_{(ESD)}$	Contact Discharge, per IEC 61000-4-2	ISO141x, Pins Bus terminals and GND1 (across isolation barrier)	±8000	V
$V_{(ESD)}$	Contact Discharge, per IEC 61000-4-2	ISO143x, Pins Bus terminals and GND1 (across isolation barrier)	±8000	V
$V_{(ESD)}$	Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except bus pins(1)	±6000	V
		Bus terminals to GND2(1)	±30000	V
	Electrostatic discharge Charged device model (CDM), per JEDEC specification JESD22-C101	All pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC1}	Supply Voltage, Side 1, 1.8-V operation	1.71	1.89	V
	Supply Voltage, Side 1, 2.5-V, 3.3-V and 5.5-V operation	2.25	5.5	V
V_{CC2}	Supply Voltage, Side 2	3	5.5	V
V_I	Common Mode voltage at any bus terminal: A or B	-7	12	V
V_{IH}	High-level input voltage (D, DE, $\overline{RE}$ inputs)	0.7*Vcc1	Vcc1	V
V_{IL}	Low-level input voltage (D, DE, $\overline{RE}$ inputs)	0	0.3*Vcc1	V
V_{ID}	Differential input voltage, A with respect to B	-15	15	V
I_O	Output current, Driver	-60	60	mA
I_{OR}	Output current, Receiver	-4	4	mA
R_L	Differential load resistance	54		Ω
$1/t_{UI}$	Signaling rate ISO141x		500	kbps
$1/t_{UI}$	Signaling Rate ISO143x		12	Mbps
$1/t_{UI}$	Signaling rate ISO145x		50	Mbps
T_A	Operating ambient temperature	-40	125	°C

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8.4 Thermal Information

THERMAL METRIC(1)		ISO14xx DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO1410_ISO1412						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, A-B load = 54 Ω ||50pF, Load on R=15pF Input a 250kHz 50% duty cycle square wave to D pin with V_{DE}=V_{CC1}, $V_{\overline{RE}}$=GND1			556	mW
P_{D1}	Maximum power dissipation (side-1)				28	mW
P_{D2}	Maximum power dissipation (side-2)				528	mW
ISO1430_ISO1432						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, A-B load = 54 Ω ||50pF, Load on R=15pF Input a 6MHz 50% duty cycle square wave to D pin with V_{DE}=V_{CC1}, $V_{\overline{RE}}$=GND1			352	mW
P_{D1}	Maximum power dissipation (side-1)				33	mW
P_{D2}	Maximum power dissipation (side-2)				319	mW
ISO1450_ISO1452						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, A-B load = 54 Ω ||50pF, Load on R=15pF Input a 25MHz 50% duty cycle square wave to D pin with V_{DE}=V_{CC1}, $V_{\overline{RE}}$=GND1			588	mW
P_{D1}	Maximum power dissipation (side-1)				49	mW
P_{D2}	Maximum power dissipation (side-2)				539	mW

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8.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
			DW-16	
IEC 60664-1				
CLR	External clearance (1)	Side 1 to side 2 distance through air	>8	mm
CPG	External creepage (1)	Side 1 to side 2 distance across package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01 (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 56	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISO141x (3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)	6250	V_{PK}
	Maximum surge isolation voltage ISO141xB (3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 6000\ V_{PK}$ (qualification)	4615	V_{PK}
q_{pd}	Apparent charge (4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; ISO14xx: $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s ISO14xxB: $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; ISO14xx: $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s ISO14xxB: $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	1	pF
R_{IO}	Insulation resistance, input to output (5)	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 150°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) ISO14xx is suitable for *safe electrical insulation* and ISO14xxB is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

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8.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017- 01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010/A1:2019, EN 60950-1:2006/A2:2013 and EN 62368-1:2014
Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1500 V_{PK}; Maximum surge isolation voltage, ISO141x, ISO143x, ISO145x: 6250 V_{PK} (Reinforced) ISO141xB, ISO143xB, ISO145xB: 4600 V_{PK} (Basic)	CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14, and IEC 62368-1 2nd Ed., for pollution degree 2, material group I ISO141x, ISO143x, ISO145x: 800 V_{RMS} reinforced isolation ISO141xB, ISO143xB, ISO145xB: 800 V_{RMS} basic isolation ---------- CSA 60601- 1:14 and IEC 60601-1 Ed. 3.1, ISO141x, ISO143x, ISO145x: 2 MOPP (Means of Patient Protection) 250 V_{RMS} (354 V_{PK}) maximum working voltage	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage	EN 61010-1:2010 /A1:2019 ISO141x, ISO143x, ISO145x: 600 V_{RMS} reinforced isolation ISO141xB, ISO143xB, ISO145xB: 1000 V_{RMS} basic isolation ---------- EN 60950-1:2006/A2:2013 and EN 62368-1:2014 ISO141x, ISO143x, ISO145x: 800 V_{RMS} reinforced isolation ISO141xB, ISO143xB, ISO145xB: 1060 V_{RMS} basic isolation
Reinforced certificate:40040142 Basic certificate: 40047657	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

8.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 67.9°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			334	mA
		$R_{\theta JA}$ = 67.9°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 1			511	
		$R_{\theta JA}$ = 67.9°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 1			669	
		$R_{\theta JA}$ = 67.9°C/W, V_I = 1.89 V, T_J = 150°C, T_A = 25°C, see Figure 1			974	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 67.9°C/W, T_J = 150°C, T_A = 25°C, see Figure 2			1837	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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8.9 Electrical Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential-output voltage magnitude	Open circuit voltage, unloaded bus, 3 V ≤ V_{CC2} ≤ 5.5 V	1.5	5	V_{CC2}	V
		R_L = 60 Ω, –7 V ≤ V_{TEST} ≤ 12 V (see Figure 35), 3 V ≤ V_{CC2} ≤ 3.6 V, T_A<100C	1.5	2.3		V
		R_L = 60 Ω, –7 V ≤ V_{TEST} ≤ 12 V (see Figure 35), 3.1 V ≤ V_{CC2} ≤ 3.6 V, T_A>100C	1.5	2.3		
		R_L = 60 Ω, –7 V ≤ V_{TEST} ≤ 12 V, 4.5 V < V_{CC2} < 5.5 V (see Figure 35)	2.1	3.7		V
		R_L = 100 Ω (see Figure 36), RS-422 load	2	4.2		V
		R_L = 54 Ω (see Figure 36), RS-485 load, V_{CC2} = 3 V to 3.6 V	1.5	2.3		V
		R_L = 54 Ω (see Figure 36), RS-485 load, 4.5 V < V_{CC2} < 5.5 V	2.1	3.7		V
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states	R_L = 54 Ω or R_L = 100 Ω, see Figure 36	–200		200	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or R_L = 100 Ω, see Figure 36	1	0.5 × V_{CC2}	3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states	R_L = 54 Ω or R_L = 100 Ω, see Figure 36	–200		200	mV
I_{OS}	Short-circuit output current	V_D = V_{CC1} or V_D = V_{GND1}, V_{DE} = V_{CC1}, V_{CC2}=3.3V ± 10% –7 V ≤ V ≤ 12 V, see Figure 45	–250		250	mA
		V_D = V_{CC1} or V_D = V_{GND1}, V_{DE} = V_{CC1}, V_{CC2}=5V ± 10% –7 V ≤ V ≤ 12 V, see Figure 45		250		mA
I_i	Input current	V_D and V_{DE} = 0 V or V_D and V_{DE} = V_{CC1}	–10		10	µA
CMTI	Common-mode transient immunity	V_D=V_{CC1} or GND1, V_{CC1} = 1.71 V to 5.5 V, V_{CM} = 1200 V, ISO141x, See Figure 38	85	100		kV/µs
CMTI	Common-mode transient immunity	V_D=V_{CC1} or GND1, V_{CC1} = 1.71 V to 5.5 V, V_{CM} = 1200 V, ISO143x, See Figure 38	85	100		kV/µs
CMTI	Common-mode transient immunity	V_D=V_{CC1} or GND1, V_{CC1} = 2.25 V to 5.5 V, V_{CM} = 1200 V, ISO145x, See Figure 38	85	100		kV/µs

8.10 Electrical Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{i1}	Bus input current	V_{DE} = 0 V, V_{CC2} = 0 V or V_{CC2} = 5.5 V, 500-kbps devices, V_I = –7 V or V_I = 12 V, other input at 0 V	–100		125	µA
I_{i1}	Bus input current	V_{DE} = 0 V, V_{CC2} = 0 V or V_{CC2} = 5.5 V, 12-Mbps and 50-Mbps devices, V_I = –7 V or V_I = 12 V, other input at 0 V	–100		125	µA
I_{i1}	Bus input current	V_{DE} = 0 V, V_{CC2} = 0 V or V_{CC2} = 5.5 V, 500-kbps devices, V_I = –15 V or V_I = 15 V, other input at 0 V	-200		125	µA
I_{i1}	Bus input current	V_{DE} = 0 V, V_{CC2} = 0 V or V_{CC2} = 5.5 V, 12-Mbps and 50-Mbps devices, V_I = –15 V or V_I = 15 V, other input at 0 V	-200		125	µA
V_{TH+}	Positive-going input threshold voltage	–15 V ≤ V_{CM} ≤ 15 V	See (1)	-100	–10	mV
		–7 V ≤ V_{CM} ≤ 12 V	See (1)	-100	–20	mV
$V_{TH–}$	Negative-going input threshold voltage	–15 V ≤ V_{CM} ≤ 15 V	–200	–130	See (1)	mV
V_{hys}	Input hysteresis (V_{TH+} – $V_{TH–}$)	–15 V ≤ V_{CM} ≤ 15 V		30		mV
V_{OH}	Output high voltage on the R pin	V_{CC1}=5V ± 10%, I_{OH} = –4 mA, V_{ID} = 200 mV	V_{CC1} – 0.4			V
		V_{CC1}=3.3V ± 10%, I_{OH} = –2 mA, V_{ID} = 200 mV	V_{CC1} – 0.3			V
		V_{CC1}=2.5V ± 10%, 1.8V+/-5%, I_{OH} = –1 mA, V_{ID} = 200 mV	V_{CC1} – 0.2			V

(1) Under any specific conditions, V_{TH+} is ensured to be at least V_{hys} higher than $V_{TH–}$.

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Electrical Characteristics: Receiver (continued)

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage on the R pin	V_{CC1}=5V ± 10%, I_{OL} = 4 mA, V_{ID} = –200 mV			0.4	V
		V_{CC1}=3.3V ± 10%, I_{OL} = 2 mA, V_{ID} = –200 mV			0.3	V
		V_{CC1}=2.5V ± 10%, 1.8V ± 5%, I_{OL} = 1 mA, V_{ID} = –200 mV			0.2	V
I_{OZ}	Output high-impedance current on the R pin	V_R = 0 V or V_R = V_{CC1}, $V_{\overline{RE}}$ = V_{CC1}	–1		1	µA
I_i	Input current on the $\overline{RE}$ pin	$V_{\overline{RE}}$ = 0 V or $V_{\overline{RE}}$ = V_{CC1}	–10		10	µA
CMTI	Common-mode transient immunity	V_{CC1}=1.71 V to 5.5 V, V_{ID} = 1.5 V or -1.5 V, V_{CM} = 1200 V, ISO141x, See Figure 38	85	100		kV/µs
CMTI	Common-mode transient immunity	V_{CC1}=1.71 V to 5.5 V, V_{ID} = 1.5 V or -1.5 V, V_{CM} = 1200 V, ISO143x, See Figure 38	85	100		kV/µs
CMTI	Common-mode transient immunity	V_{CC1}=2.25 V to 5.5 V, V_{ID} = 1.5 V or -1.5 V, V_{CM} = 1200 V, ISO145x, See Figure 38	85	100		kV/µs

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8.11 Supply Current Characteristics: Side 1 (I_{CC1})

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, RECEIVER DISABLED					
Logic-side supply current	$V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%		2.6	4.4	mA
Logic-side supply current	$V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%		2.6	4.4	mA
Logic-side supply current	ISO141x, D = 500-kbps square wave with 50% duty cycle, V_{CC1} = 5 V ± 10%		3.2	5.1	mA
Logic-side supply current	ISO141x, D = 500-kbps square wave with 50% duty cycle, V_{CC1} = 3.3 V ± 10%		3.2	5.1	mA
Logic-side supply current	ISO143x, D = 12-Mbps square wave with 50% duty cycle, V_{CC1} = 5 V ± 10%		3.2	5.1	mA
Logic-side supply current	ISO143x, D = 12-Mbps square wave with 50% duty cycle, V_{CC1} = 3.3 V ± 10%		3.2	5.1	mA
Logic-side supply current	ISO145x, D = 50-Mbps square wave with 50% duty cycle, V_{CC1} = 5 V ± 10%		3.6	5.3	mA
Logic-side supply current	ISO145x, D = 50-Mbps square wave with 50% duty cycle, V_{CC1} = 3.3 V ± 10%		3.4	5.2	mA
DRIVER ENABLED, RECEIVER ENABLED					
Logic-side supply current	$V_{\overline{RE}} = V_{GND1}$, loopback if full-duplex device, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%		2.6	4.4	mA
Logic-side supply current	$V_{\overline{RE}} = V_{GND1}$, loopback if full-duplex device, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%		2.6	4.4	mA
Logic-side supply current	ISO141x, $V_{\overline{RE}} = V_{GND1}$, loopback if full-duplex device, D = 500-kbps square wave with 50% duty cycle, V_{CC1} = 5 V ± 10%, $C_{L(R)}$ (1) = 15 pF		3.3	5.1	mA
Logic-side supply current	ISO141x, $V_{\overline{RE}} = V_{GND1}$, loopback if full-duplex device, D = 500-kbps square wave with 50% duty cycle, V_{CC1} = 3.3 V ± 10%, $C_{L(R)}$ (1) = 15 pF		3.2	5.1	mA
Logic-side supply current	ISO143x, $V_{\overline{RE}} = V_{GND1}$, loopback if full-duplex device, D = 12-Mbps square wave with 50% duty cycle, V_{CC1} = 5 V ± 10%, $C_{L(R)}$ (1) = 15 pF		4.1	6	mA
Logic-side supply current	ISO143x, $V_{\overline{RE}} = V_{GND1}$, loopback if full-duplex device, D= 12-Mbps square wave with 50% duty cycle, V_{CC1} = 3.3 V ± 10%, $C_{L(R)}$ (1) = 15 pF		3.8	5.7	mA
Logic-side supply current	ISO145x, $V_{\overline{RE}} = V_{GND1}$, loopback if full-duplex device, D = 50-Mbps square wave with 50% duty cycle, V_{CC1} = 5 V ± 10%, $C_{L(R)}$ (1) = 15 pF		6.3	8.9	mA
Logic-side supply current	ISO145x, $V_{\overline{RE}} = V_{GND1}$, loopback if full-duplex device, D= 50-Mbps square wave with 50% duty cycle, V_{CC1} = 3.3 V ± 10%, $C_{L(R)}$ (1) = 15 pF		5.3	7.8	mA
DRIVER DISABLED, RECEIVER ENABLED					
Logic-side supply current	$V_{(A-B)} \geq 200$ mV, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%		1.6	3.1	mA
Logic-side supply current	$V_{(A-B)} \geq 200$ mV, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%		1.6	3.1	mA
Logic-side supply current	ISO141x, (A-B) = 500-kbps square wave with 50% duty cycle, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%, $C_{L(R)}$ (1) = 15 pF		1.7	3.1	mA
Logic-side supply current	ISO141x, (A-B) = 500-kbps square wave with 50% duty cycle, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%, $C_{L(R)}$ (1) = 15 pF		1.6	3.1	mA
Logic-side supply current	ISO143x, (A-B) = 12-Mbps square wave with 50% duty cycle, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%, $C_{L(R)}$ (1) = 15 pF		2.6	4	mA
Logic-side supply current	ISO143x, (A-B) = 12-Mbps square wave with 50% duty cycle, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%, $C_{L(R)}$ (1) = 15 pF		2.2	3.7	mA
Logic-side supply current	ISO145x, (A-B) = 50-Mbps square wave with 50% duty cycle, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%, $C_{L(R)}$ (1) = 15 pF		4.7	6.7	mA
Logic-side supply current	ISO145x, (A-B) = 50-Mbps square wave with 50% duty cycle, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%, $C_{L(R)}$ (1) = 15 pF		3.7	5.7	mA
DRIVER DISABLED, RECEIVER DISABLED					
Logic-side supply current	$V_{DE} = V_{GND1}$, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%		1.6	3.1	mA
Logic-side supply current	$V_{DE} = V_{GND1}$, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%		1.6	3.1	mA

(1) $C_{L(R)}$ is the load capacitance on the R pin.

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8.12 Supply Current Characteristics: Side 2 (I_{CC2})

$V_{\overline{RE}} = V_{GND1}$ or $V_{\overline{RE}} = V_{CC1}$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, BUS UNLOADED					
Bus-side supply current	$V_D = V_{CC1}$, V_{CC2} = 3.3 V ± 10%		4	6.1	mA
Bus-side supply current	$V_D = V_{CC1}$, V_{CC2} = 5 V ± 10%		4.5	6.6	mA
DRIVER ENABLED, BUS LOADED					
Bus-side supply current	$V_D = V_{CC1}$, R_L = 54 Ω, V_{CC2} = 3.3 V ± 10%		48	58	mA
Bus-side supply current	$V_D = V_{CC1}$, R_L = 54 Ω, V_{CC2} = 5 V ± 10%		74	88	mA
Bus-side supply current	ISO141x, D = 500-kbps square wave with 50% duty cycle, R_L = 54 Ω, C_L = 50 pF, V_{CC2} = 3.3 V ± 10%		63	95	mA
Bus-side supply current	ISO141x, D = 500-kbps square wave with 50% duty cycle, R_L = 54 Ω, C_L = 50 pF, V_{CC2} = 5 V ± 10%		113	160	mA
Bus-side supply current	ISO143x, D = 12-Mbps square wave with 50% duty cycle, R_L = 54 Ω, C_L = 50 pF, V_{CC2} = 3.3 V ± 10%		56	75	mA
Bus-side supply current	ISO143x, D = 12-Mbps square wave with 50% duty cycle, R_L = 54 Ω, C_L = 50 pF, V_{CC2} = 5 V ± 10%		97	122	mA
Bus-side supply current	ISO145x, D = 50-Mbps square wave with 50% duty cycle, R_L = 54 Ω, C_L = 50 pF, V_{CC2} = 3.3 V ± 10%		84	103	mA
Bus-side supply current	ISO145x, D = 50-Mbps square wave with 50% duty cycle, R_L = 54 Ω, C_L = 50 pF, V_{CC2} = 5 V ± 10%		134	162	mA
DRIVER DISABLED, BUS LOADED OR UNLOADED					
Bus-side supply current	$V_D = V_{CC1}$, V_{CC2} = 3.3 V ± 10%		2.6	4.3	mA
Bus-side supply current	$V_D = V_{CC1}$, V_{CC2} = 5 V ± 10%		2.8	4.5	mA

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8.13 Switching Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
500-kbps DEVICES						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 37	240	460	680	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see Figure 37		310	570	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see Figure 37		4	50	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 40, and Figure 41		125	200	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 40, and Figure 41		160	600	ns
12-Mbps DEVICES						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, V_{CC2}= 4.5 V to 5.5 V, see Figure 37		10	25	ns
		R_L = 54 Ω, C_L = 50 pF, V_{CC2}= 3 V to 3.6 V, see Figure 37			27.8	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see Figure 37		68	125	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see Figure 37		2	10	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 40, and Figure 41		75	125	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 40, and Figure 41		75	160	ns
50-Mbps DEVICES						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, V_{CC2}= 4.5 V to 5.5 V, see Figure 37		4.7	6	ns
		R_L = 54 Ω, C_L = 50 pF, V_{CC2}= 3 V to 3.6 V, see Figure 37			7.8	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see Figure 37		19	41	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see Figure 37		1	6	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 40, and Figure 41		25	46	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 40, and Figure 41		32	78	ns

(1) Also known as pulse skew.

8.14 Switching Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
500-kbps DEVICES						
t_r, t_f	Differential output rise time and fall time	C_L = 15 pF, see Figure 42		1	4	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see Figure 42		92	135	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see Figure 42		4.5	12.5	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 43 and Figure 44		9	30	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 43 and Figure 44		5	20	ns
12-Mbps DEVICES						
t_r, t_f	Differential output rise time and fall time	C_L = 15 pF, see Figure 42		1	4	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see Figure 42		75	120	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see Figure 42		1	10	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 43 and Figure 44		9	30	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 43 and Figure 44		5	20	ns
50-Mbps DEVICES						
t_r, t_f	Differential output rise time and fall time	C_L = 15 pF, see Figure 42		1	4	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see Figure 42		36	60	ns

(1) Also known as pulse skew.

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Switching Characteristics: Receiver (continued)

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, Measured with 50kHz, 50% Duty Clock, see Figure 42		2	6	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 43 and Figure 44		9	30	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 43 and Figure 44		5	20	ns

8.15 Insulation Characteristics Curves

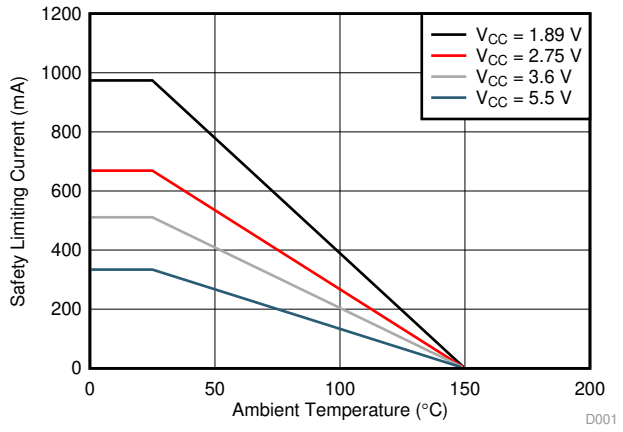


Figure 1. Thermal Derating Curve for Limiting Current per VDE

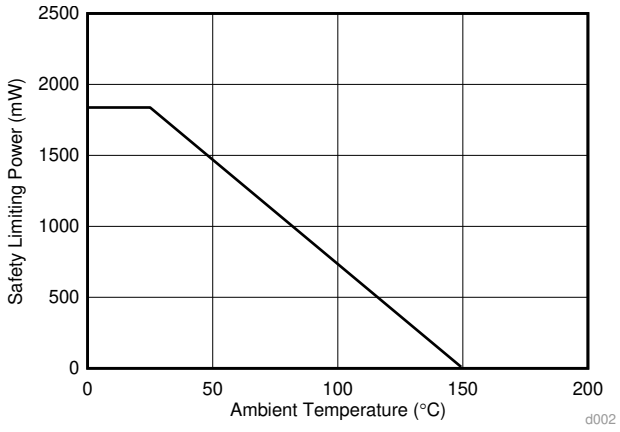
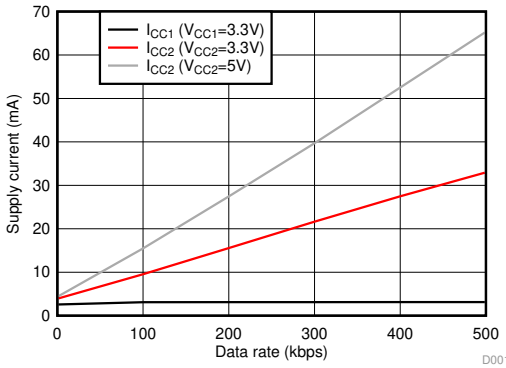


Figure 2. Thermal Derating Curve for Limiting Power per VDE

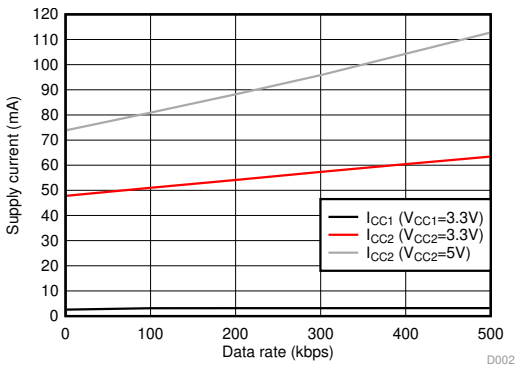
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8.16 Typical Characteristics



DE = V_{CC1} $\overline{RE}$ = GND1 T_A = 25°C

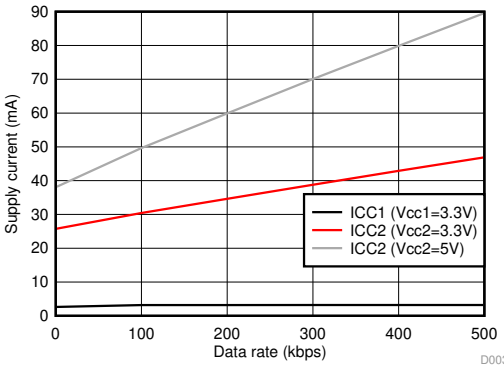
Figure 3. ISO141x Supply Current Vs Data Rate- No Load



DE = V_{CC1} $\overline{RE}$ = GND1 Driver Load = 54 Ω || 50pF

T_A = 25°C Load On R = 15 pF

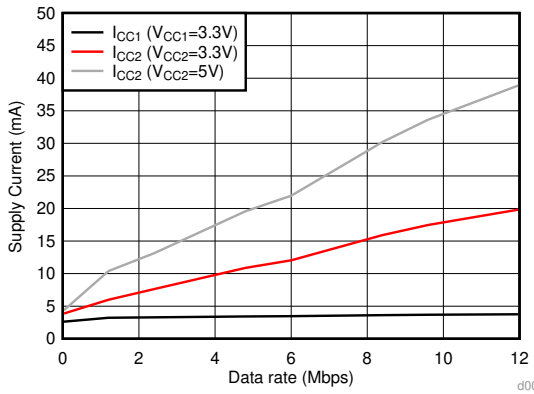
Figure 4. ISO141x Supply Current Vs Data Rate- With 54Ω||50pf Load



DE = V_{CC1} $\overline{RE}$ = GND1 Driver Load = 120 Ω || 50pF

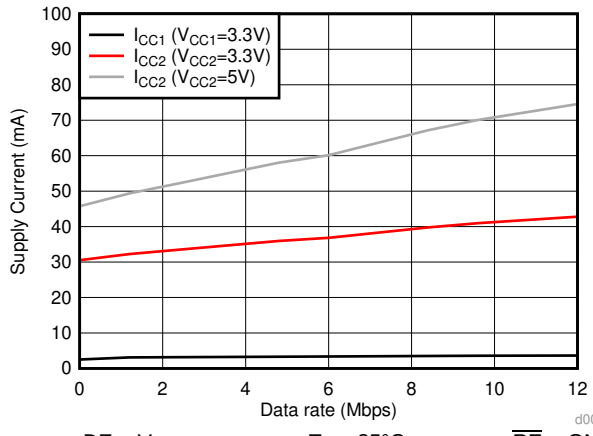
T_A = 25°C Load On R = 15 pF

Figure 5. ISO141x Supply Current Vs Data Rate- With 120Ω||50pf Load



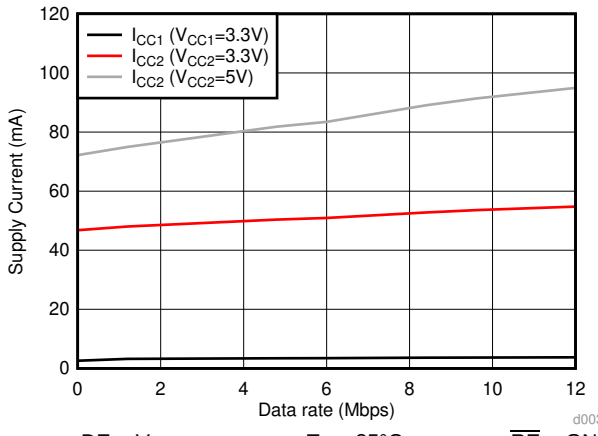
DE = V_{CC1} T_A = 25°C $\overline{RE}$ = GND1

Figure 6. ISO143x Supply Current Vs. Data Rate - No Load



DE = V_{CC1} T_A = 25°C $\overline{RE}$ = GND1
Driver Load = 120 Ω || 50pF 50pF, Load On R = 15pf

Figure 7. ISO143x Supply Current Vs. Data Rate - 120Ω||50pF Load

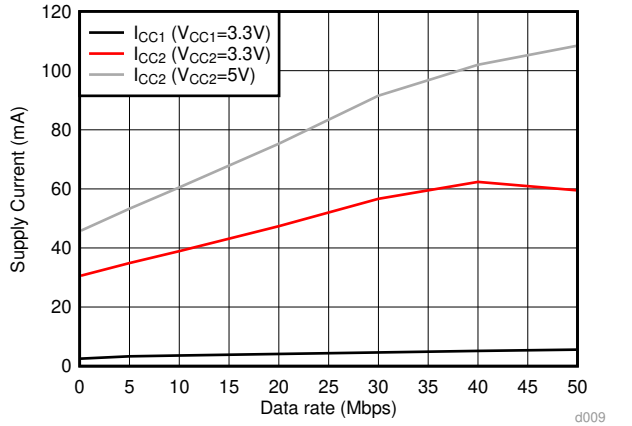


DE = V_{CC1} T_A = 25°C $\overline{RE}$ = GND1
Driver Load = 54 Ω || 50pF 50pF, Load On R = 15pf

Figure 8. ISO143x Supply Current Vs Data Rate- 54Ω||50pF Load

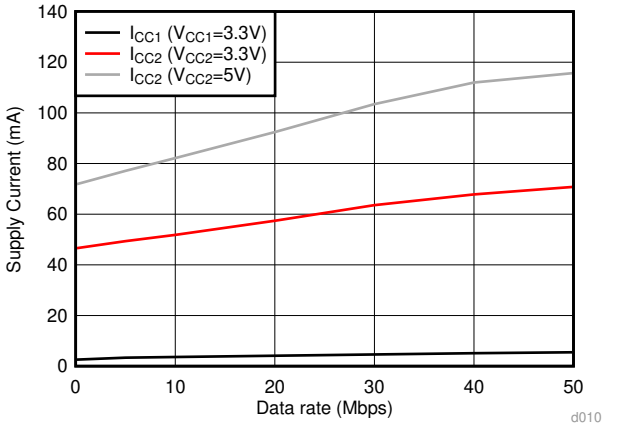
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Typical Characteristics (continued)



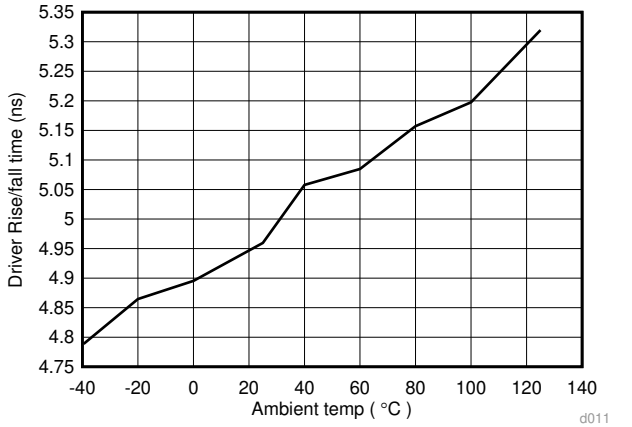
DE = V_{CC1} T_A = 25°C $\overline{RE}$ = GND1

Figure 9. ISO145x Supply Current Vs Data Rate- No Load



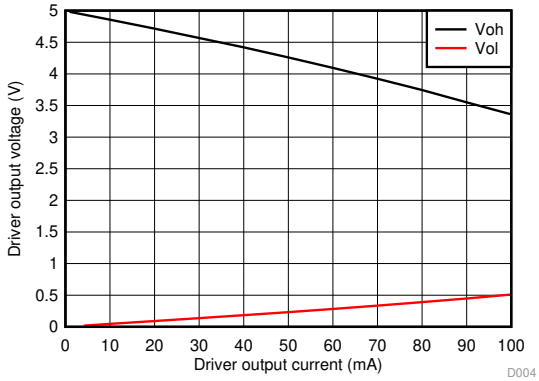
DE = V_{CC1} T_A = 25°C $\overline{RE}$ = GND1
Driver Load = 120 Ω || 50pF 50pF, Load On R = 15pf

Figure 10. ISO145x Supply Current Vs Data Rate- 120Ω||50pF Load



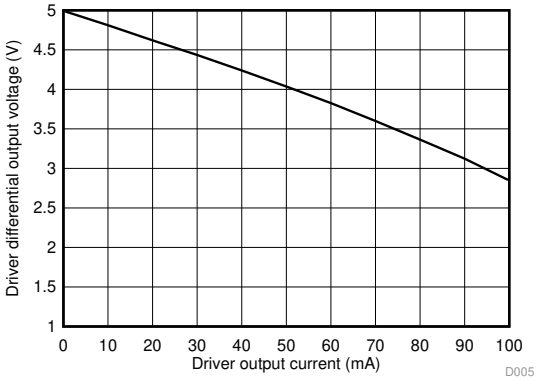
DE = V_{CC1} T_A = 25°C $\overline{RE}$ = GND1
Driver Load = 54 Ω || 50pF 50pF, Load On R = 15pf

Figure 11. ISO145x Supply Current Vs Data Rate- 54Ω||50pF Load



DE = V_{CC1} D = GND1 V_{CC1} = 3.3 V
T_A = 25°C V_{CC2} = 5 V

Figure 12. Driver Output Voltage Vs Driver Output Current



DE = V_{CC1} D = GND1 V_{CC1} = 3.3 V
T_A = 25°C V_{CC2} = 5 V

Figure 13. Driver Differential Output Voltage Vs Driver Output Current

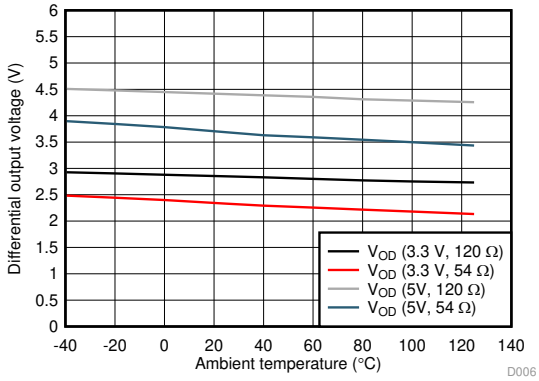


Figure 14. Driver Differential Output Voltage Vs Temperature

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Typical Characteristics (continued)

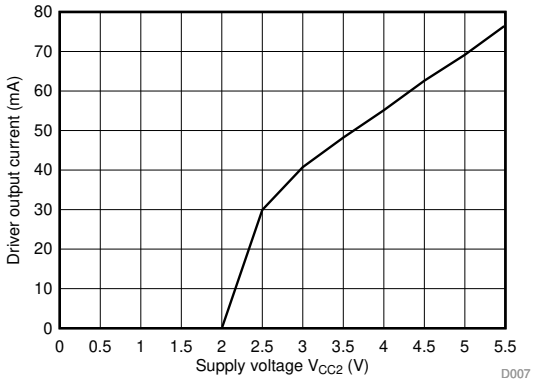


Figure 15. Driver Output Current Vs Supply Voltage (V_{CC2})

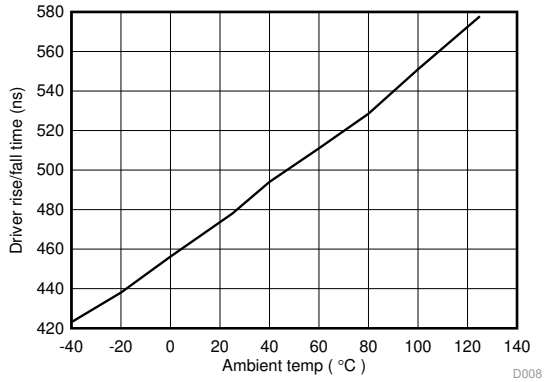


Figure 16. ISO141x Driver Rise/fall Time (ns) Vs Temperature (c)

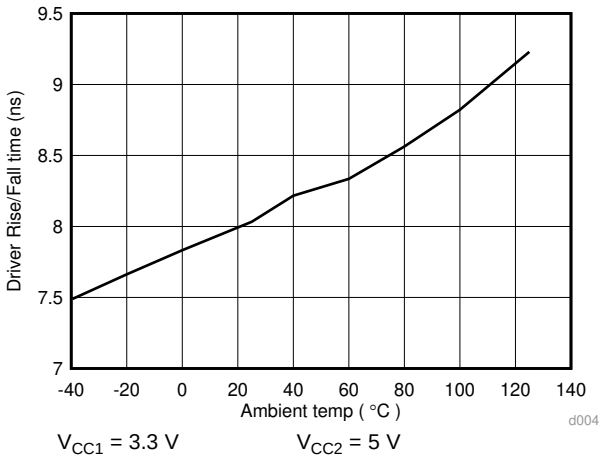


Figure 17. ISO143x Driver Rise/Fall Time (ns) Vs Temperature (C)

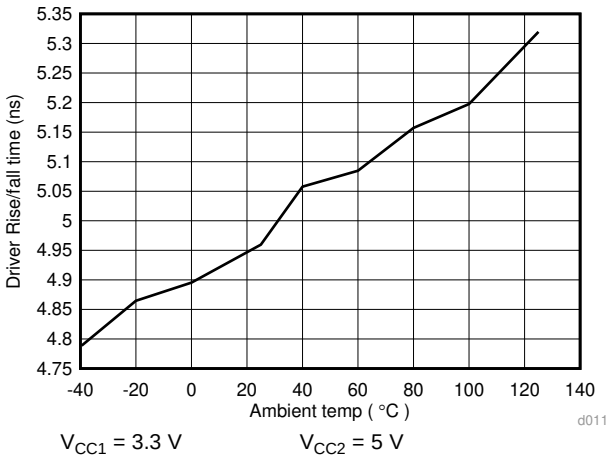


Figure 18. ISO145x Driver Rise/Fall Time (ns) Vs Temperature (C)

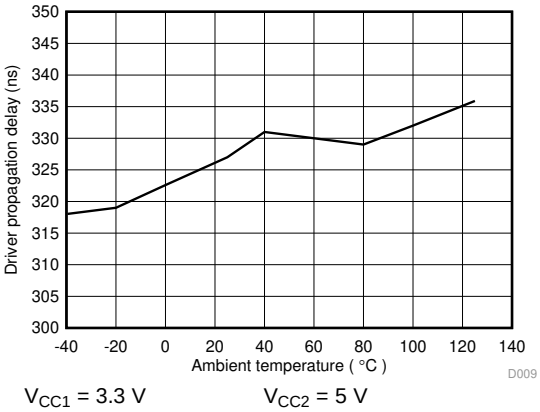


Figure 19. ISO141x Driver Propagation Delay (ns) Vs Temperature (c)

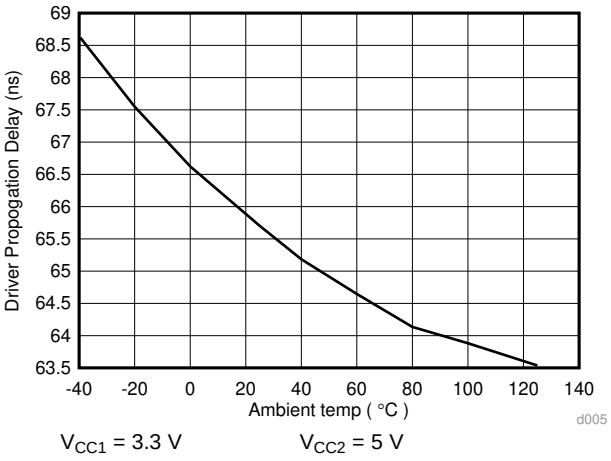


Figure 20. ISO143x Driver Propagation Delay (ns) Vs Temperature (C)

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Typical Characteristics (continued)

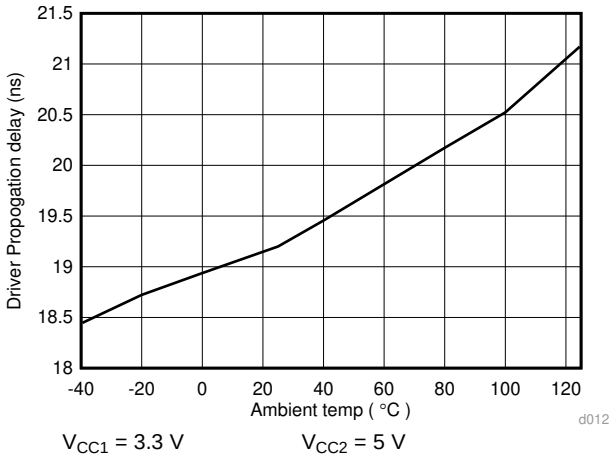


Figure 21. ISO145x Driver Propagation Delay (ns) Vs Temperature (C)

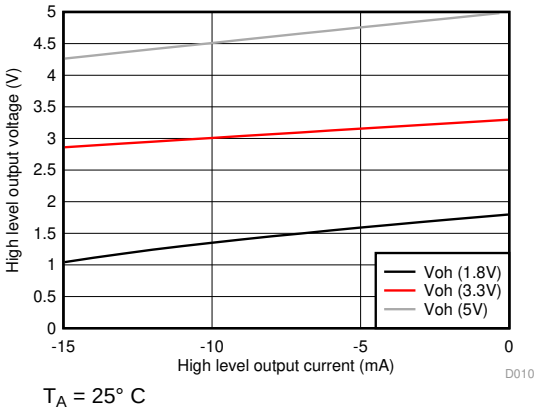


Figure 22. Receiver Buffer High Level Output Voltage Vs High Level Output Current

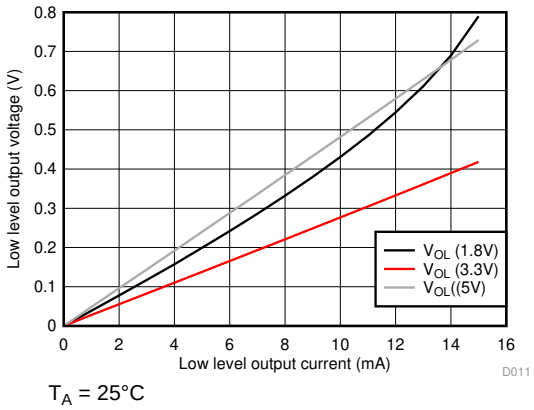


Figure 23. Receiver Buffer Low Level Output Voltage Vs Low Level Output Current

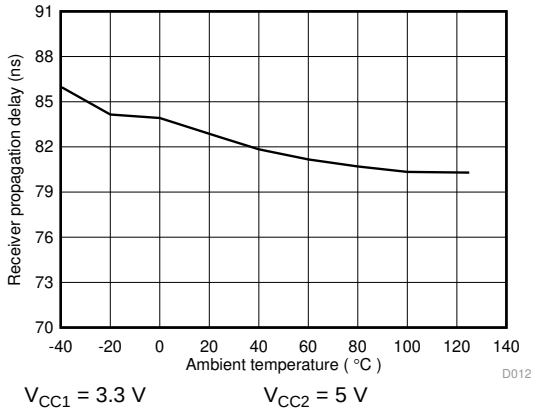


Figure 24. ISO141x Receiver Propagation Delay (ns) Vs Temperature (c)

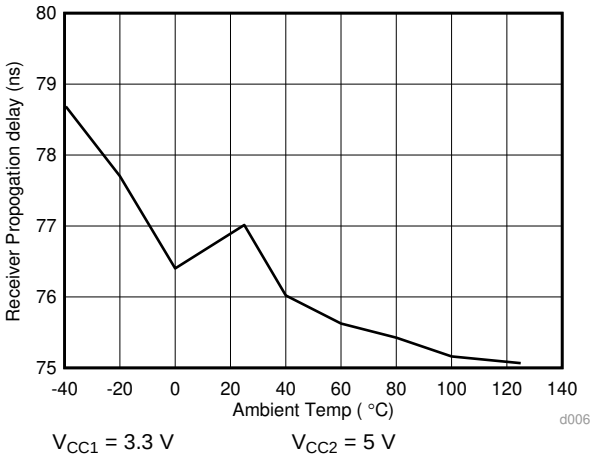


Figure 25. ISO143x Receiver Propagation Delay (ns) Vs. Temperature (C)

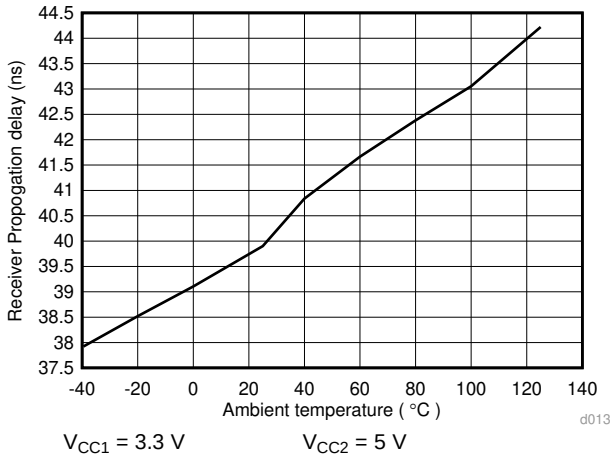
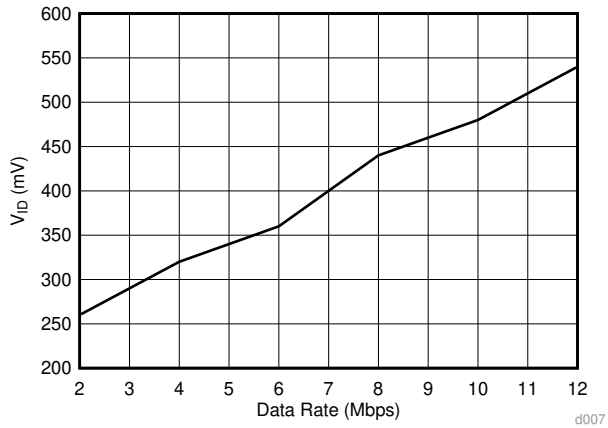


Figure 26. ISO145x Receiver Propagation Delay (ns) Vs. Temperature (C)

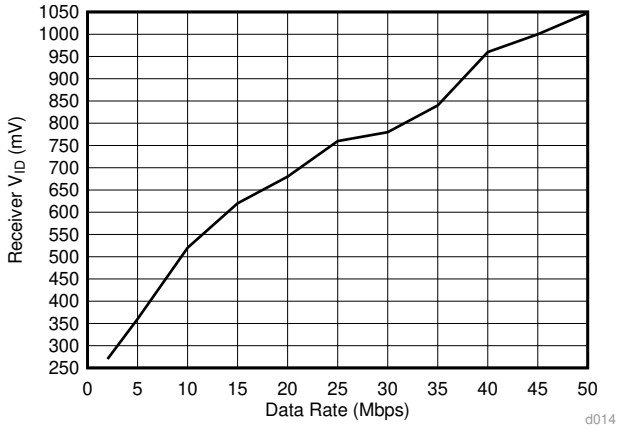
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Typical Characteristics (continued)



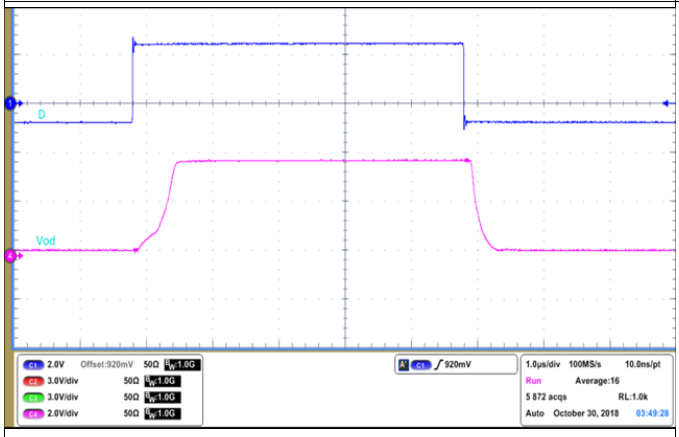
For PWD ≤±5%

Figure 27. ISO143x Receiver V_{ID} vs Signaling Rate



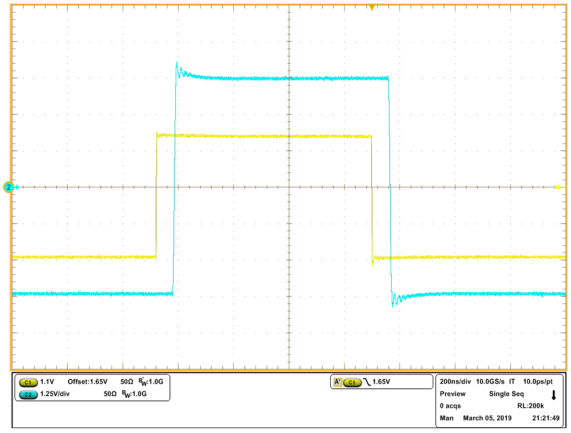
For PWD ≤±5%

Figure 28. ISO145x Receiver V_{ID} vs Signaling Rate



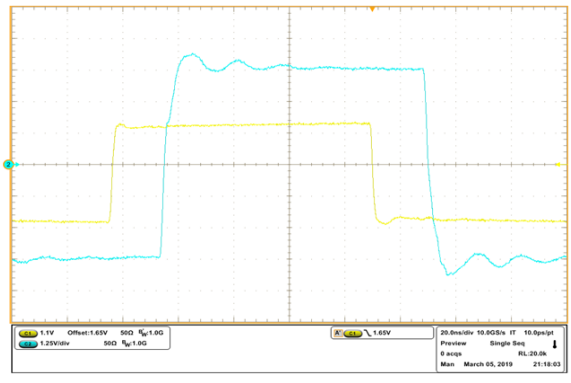
V_{CC1} = 3.3 V V_{CC2} = 5 V T_A = 25° C
DE = V_{CC1}

Figure 29. ISO141x Driver Propagation Delay



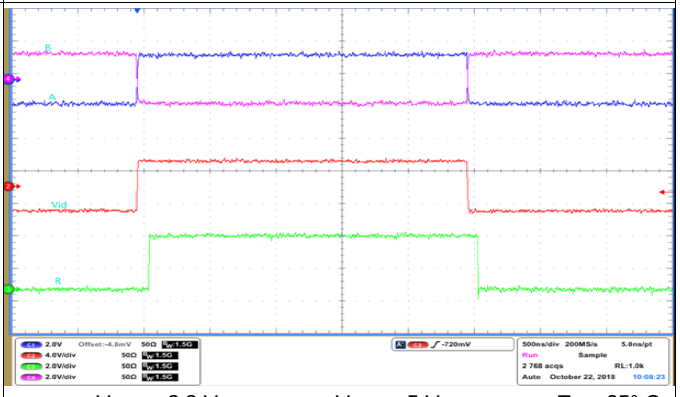
V_{CC1} = 3.3 V V_{CC2} = 5 V T_A = 25° C
DE = V_{CC1}

Figure 30. ISO143x Driver Propagation Delay



V_{CC1} = 3.3 V V_{CC2} = 5 V T_A = 25° C
DE = V_{CC1}

Figure 31. ISO145x Driver Propagation Delay



V_{CC1} = 3.3 V V_{CC2} = 5 V T_A = 25° C
DE = GND1 $\overline{RE}$ = GND1

Figure 32. ISO141x Receiver Propagation Delay

Typical Characteristics (continued)

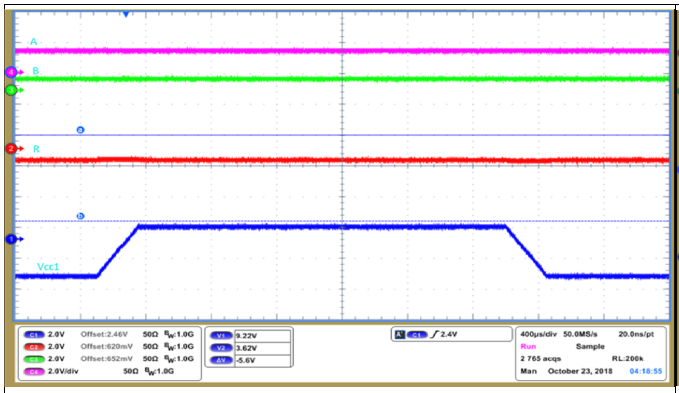


Figure 33. V_{CC1} Power Up/Power Down - Glitch Free Behavior

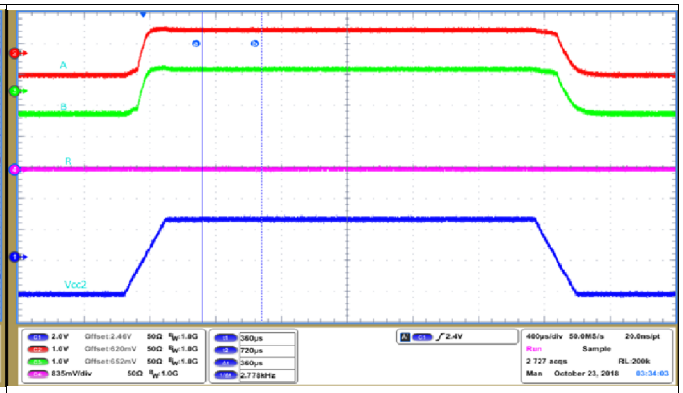


Figure 34. V_{CC2} Power Up/Power Down - Glitch Free Behavior

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9 Parameter Measurement Information

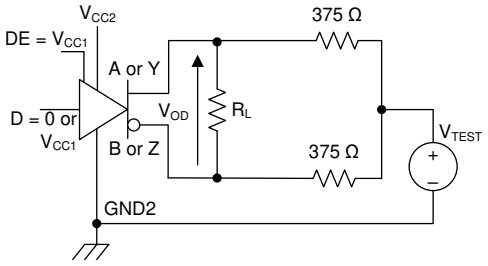
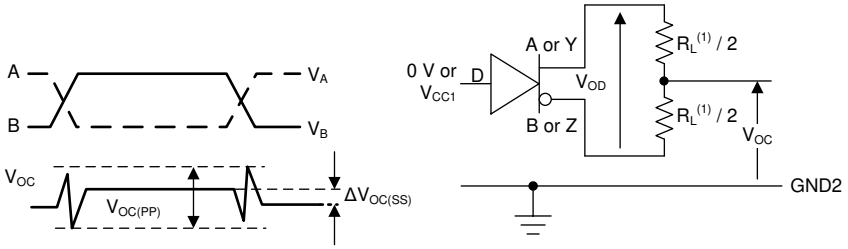
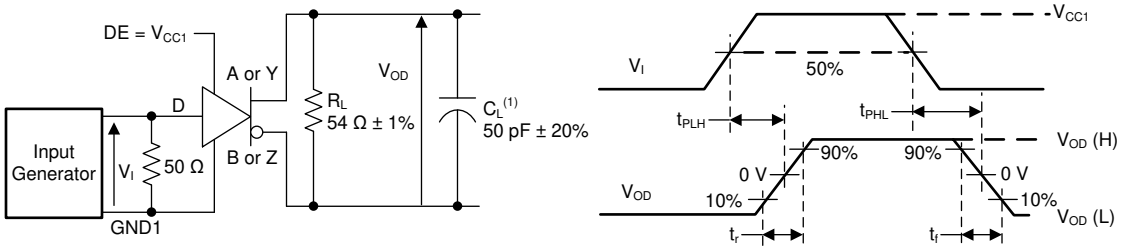


Figure 35. Driver Voltages



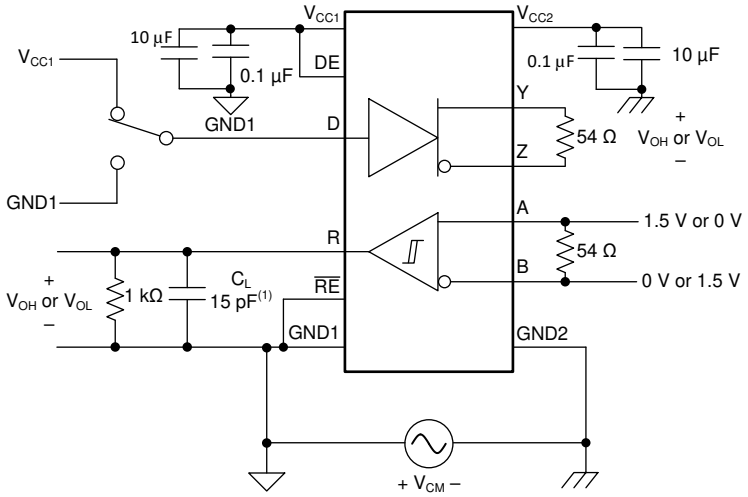
(1) R_L = 100 Ω for RS422, R_L = 54 Ω for RS-485

Figure 36. Driver Voltages



(1) C_L includes fixture and instrumentation capacitance.

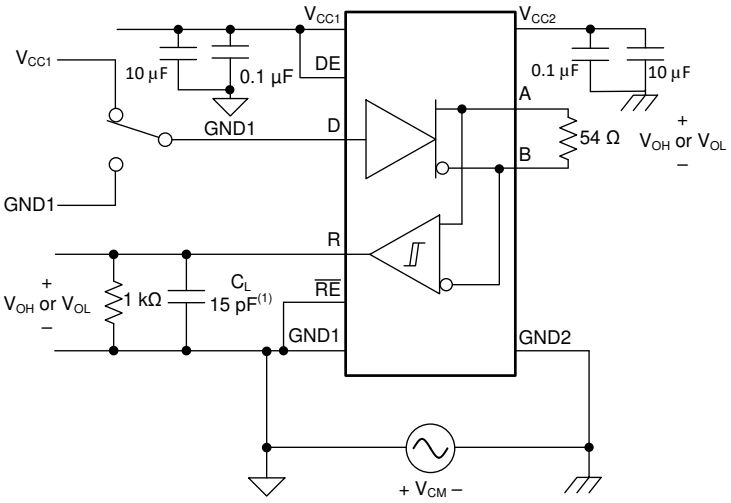
Figure 37. Driver Switching Specifications



(1) Includes probe and fixture capacitance.

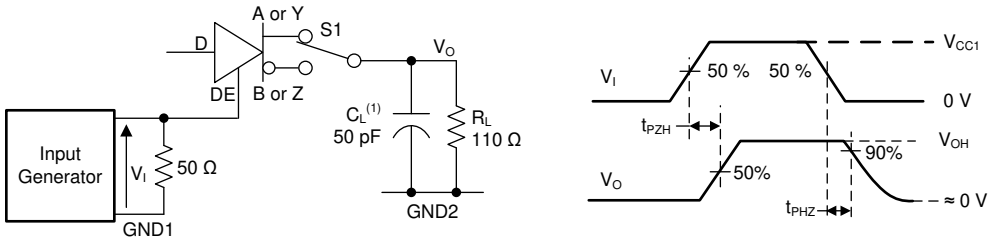
Figure 38. Common Mode Transient Immunity (CMTI)—Full Duplex

Parameter Measurement Information (continued)



(1) Includes probe and fixture capacitance.

Figure 39. Common Mode Transient Immunity (CMTI)—Half Duplex



(1) C_L includes fixture and instrumentation capacitance

Figure 40. Driver Enable and Disable Times

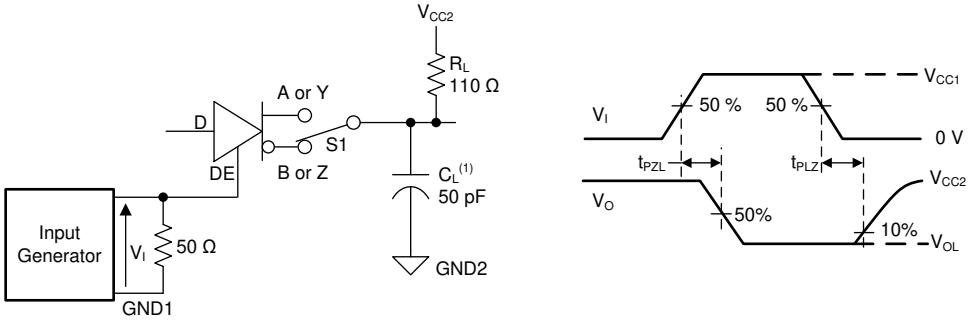
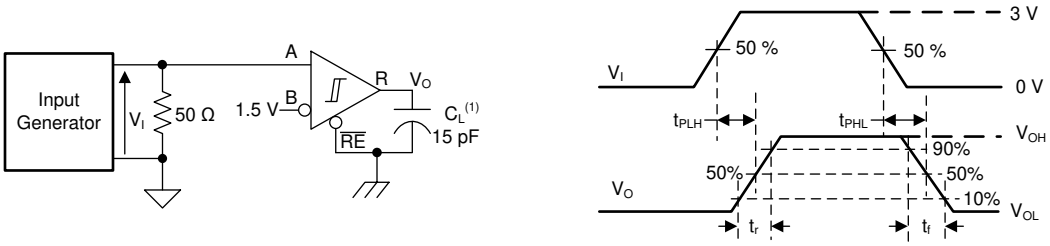


Figure 41. Driver Enable and Disable Times

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Parameter Measurement Information (continued)



(1) C_L includes fixture and instrumentation capacitance.

Figure 42. Receiver Switching Specifications

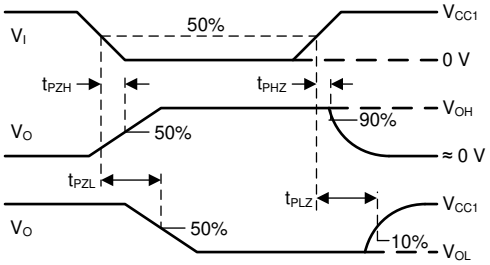


Figure 43. Receiver Enable and Disable Times

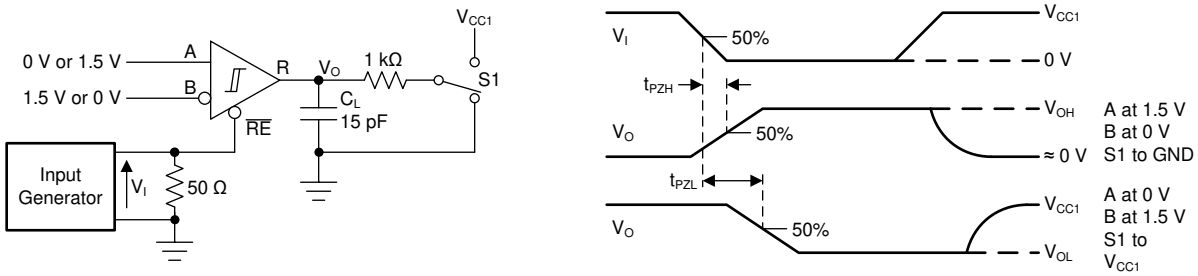
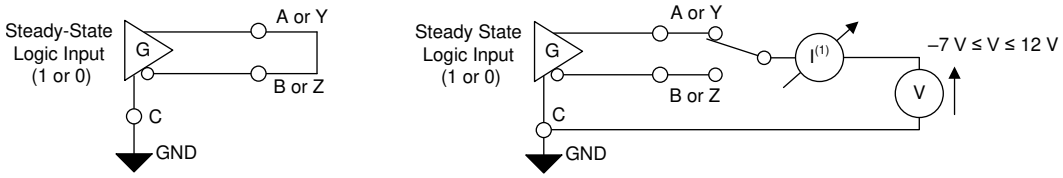


Figure 44. Receiver Enable and Disable Times



(1) The driver should not sustain any damage with this configuration.

Figure 45. Short-Circuit Current Limiting

10 Detailed Description

10.1 Overview

The ISO14xx devices are isolated RS-485/RS-422 transceivers designed to operate in harsh industrial environments. ISO141x, ISO143x and ISO145x devices support up to 500 kbps, 12 Mbps and 50 Mbps signaling rates respectively. This family of devices has a 3-channel digital isolator and an RS-485 transceiver in a 16-pin wide-body SOIC package. The silicon-dioxide based capacitive isolation barrier supports an isolation withstand voltage of 5 kV_{RMS} and an isolation working voltage of 1500 V_{PK}. Isolation breaks the ground loop between the communicating nodes and allows for data transfer in the presence of large ground potential differences. These devices have a higher typical differential output voltage (V_{OD}) than traditional transceivers for better noise immunity. A minimum differential output voltage of 2.1 V is specified at a V_{CC2} voltage of 5 V ±10% which meets the requirements for Profibus applications. The wide logic supply of the device (V_{CC1}) supports interfacing with 1.8-V, 2.5-V, 3.3-V, and 5-V control logic. The 3-V to 5.5-V bus side supply (V_{CC2}) removes the need of a well-regulated isolated supply in end systems. Figure 46 shows the functional block diagram of the full-duplex devices and Figure 47 shows the functional block diagram of a half-duplex devices.

10.2 Functional Block Diagram

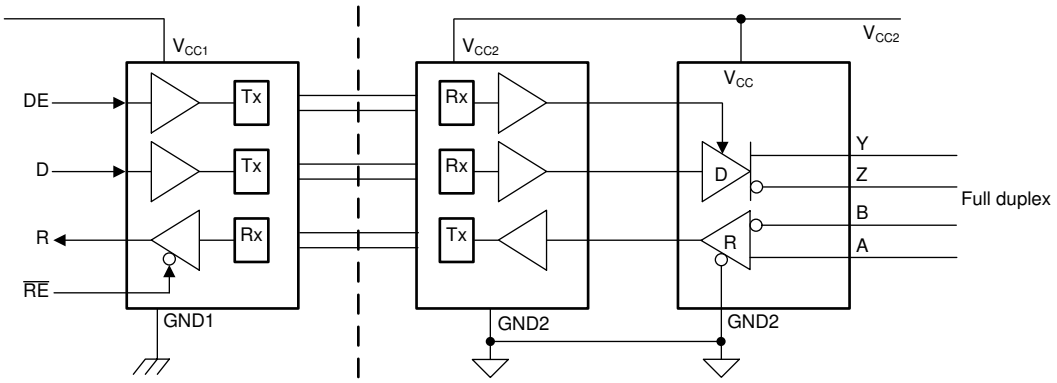


Figure 46. Full-Duplex Block Diagram

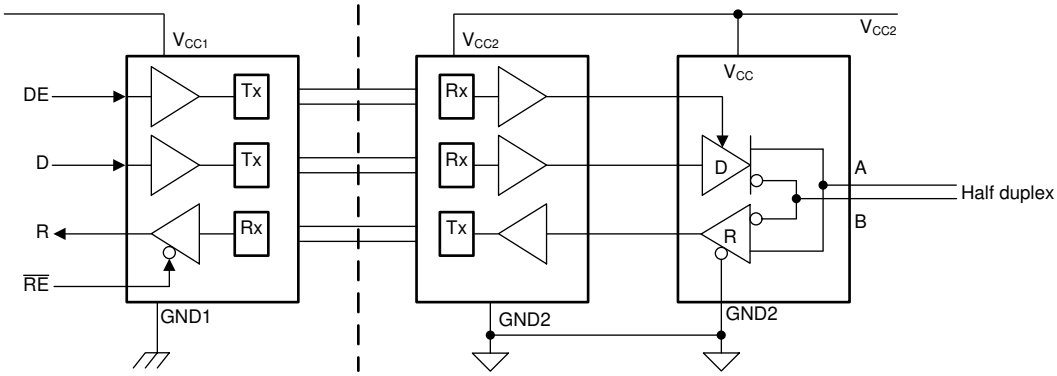


Figure 47. Half-Duplex Block Diagram

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10.3 Feature Description

10.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO14xx devices incorporate dedicated circuitry to protect the transceiver from ±16 kV ESD per IEC61000-4-2 and ±4 kV EFT per IEC 61000-4-4. System designers can achieve the ±4-kV EFT Criterion A with careful system design (data communication between nodes in the presence of transient noise with minimum to no data loss).

10.3.2 Failsafe Receiver

The differential receiver of the ISO14xx devices has failsafe protection from invalid bus states caused by:

- Open bus conditions such as a broken cable or a disconnected connector
- Shorted bus conditions such as insulation breakdown of a cable that shorts the twisted-pair
- Idle bus conditions that occur when no driver on the bus is actively driving

The differential input of the RS-485 receiver is 0 in any of these conditions for a terminated transmission line. The receiver outputs a failsafe logic-high state so that the output of the receiver is not indeterminate.

The receiver thresholds are offset in the receiver failsafe protection so that the indeterminate range of the does not include a 0 V differential. The receiver output must generate a logic high when the differential input (V_{ID}) is greater than 200 mV to comply with the RS-485 standard. The receiver output must also generate a output a logic low when V_{ID} is less than –200 mV to comply with the RS-485 standard. The receiver parameters that determine the failsafe performance are V_{TH+}, $V_{TH–}$, and V_{HYS}. Differential signals less than –200 mV always cause a low receiver output as shown in the *Electrical Characteristics* table. Differential signals greater than 200 mV always cause a high receiver output. A differential input signal that is near zero is still greater than the V_{TH+} threshold which makes the receiver output logic high. The receiver output goes to a low state only when the differential input decreases by V_{HYS} to less than V_{TH+}.

The internal failsafe biasing feature removes the need for the two external resistors that are typically required with traditional isolated RS-485 transceivers as shown in Figure 48.

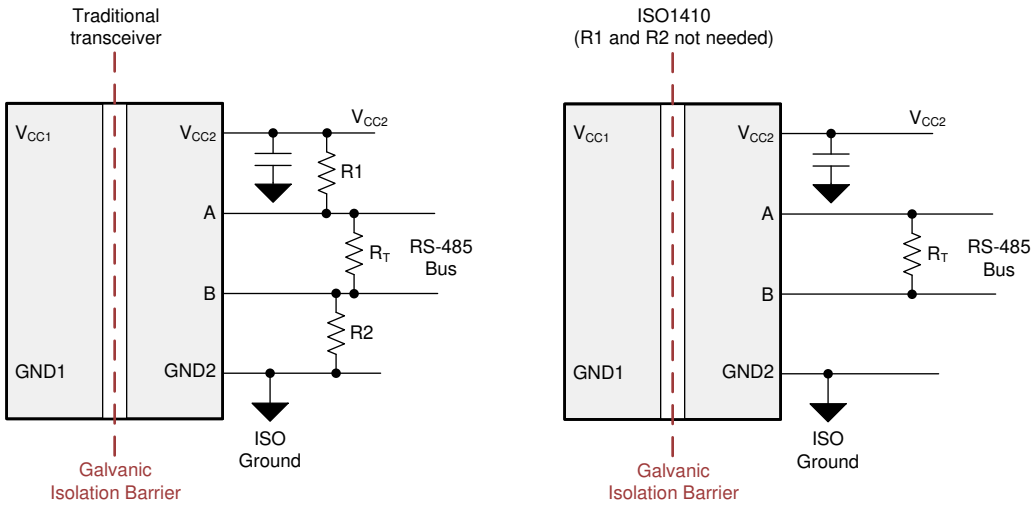


Figure 48. Failsafe Transceiver

10.3.3 Thermal Shutdown

The ISO14xx devices have a thermal shutdown circuit to protect against damage when a fault condition occurs. A driver output short circuit or bus contention condition can cause the driver current to increase significantly which increases the power dissipation inside the device. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes 170℃ (typical) which lets the device decrease the temperature. The device is enabled when the junction temperature becomes 165℃ (typical).

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Feature Description (continued)

Bus short circuit for an extended duration and/or beyond voltage levels specified in recommended operating condition should be avoided. Repeated or prolonged exposure to bus shorts can result in high junction temperatures and affect device reliability.

10.3.4 Glitch-Free Power Up and Power Down

Communication on the bus that already exist between a master node and slave node in an RS485 network must not be disturbed when a new node is swapped in or out of the network. No glitches on the bus occur when the device is:

- Hot plugged into the network in an unpowered state
- Hot plugged into the network in a powered state and disabled state
- Powered up or powered down in a disabled state when already connected to the bus

The ISO14xx devices do not cause any false data toggling on the bus when powered up or powered down in a disabled state with supply ramp rates from 100 µs to 10 ms.

10.4 Device Functional Modes

Table 2 shows the driver functional modes.

Table 2. Driver Functional table(1)

V_{CC1}	V_{CC2}	INPUT D	DRIVER ENABLE DE	OUTPUTS(2)	
				Y, A	Z, B
PU	PU	H	H	H	L
		L	H	L	H
		X	L	Hi-Z	Hi-Z
		X	Open	Hi-Z	Hi-Z
		Open	H	H	L
PD(3)	PU	X	X	Hi-Z	Hi-Z
X	PD	X	X	Hi-Z	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = High Level; L = Low level; X = Irrelevant, Hi-Z = High impedance state
(2) The driver outputs are Y and Z for a full-duplex device. The driver outputs are A and B for a half-duplex device.
(3) A strongly driven input signal can weakly power the floating V_{CC1} through an internal protection diode and cause an undetermined output.

The description that follows is specific to half-duplex device but the same logic applies to full-duplex device with the outputs being Y and Z.

When the driver enable pin, DE, is logic high, the differential outputs, A and B, follow the logic states at data input, D. A logic high at the D input causes the A output to go high and the B output to go low. Therefore the differential output voltage defined by Equation 1 is positive.

$$V_{OD} = V_A - V_B \quad (1)$$

A logic low at the D input causes the B output to go high and the A output to go low. Therefore the differential output voltage defined by Equation 1 is negative. A logic low at the DE input causes both outputs to go to the high-impedance (Hi-Z) state. The logic state at the D pin is irrelevant when the DE input is logic low. The DE pin has an internal pulldown resistor to ground. The driver is disabled (bus outputs are in the Hi-Z) by default when the DE pin is left open. The D pin has an internal pullup resistor. The A output goes high and the B output goes low when the D pin is left open while the driver enabled.

Table 3 shows the receiver functional modes.

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Table 3. Receiver Functional Table(1)

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT	RECEIVER ENABLE $\overline{RE}$	OUTPUT R
		$V_{ID} = V_A - V_B$		
PU	PU	$-0.02\ V \le V_{ID}$	L	H
		$-0.2\ V < V_{ID} < 0.02\ V$	L	Indeterminate
		$V_{ID} \le -0.2\ V$	L	L
		X	H	Hi-Z
		X	Open	Hi-Z
		Open, Short, Idle	L	H
PD(2)	PU	X	X	Hi-Z
PU	PD	X	L	H
PD(2)	PD	X	X	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (OFF) state
(2) A strongly driven input signal can weakly power the floating V_{CC1} through an internal protection diode and cause an undetermined output.

The receiver is enabled when the receiver enable pin, $\overline{RE}$, is logic low. The receiver output, R, goes high when the differential input voltage defined by Equation 2 is greater than the positive input threshold, V_{TH+}.

$$V_{ID} = V_A - V_B \quad (2)$$

The receiver output, R, goes low when the differential input voltage defined by Equation 2 is less than the negative input threshold, V_{TH-}. If the V_{ID} voltage is between the V_{TH+} and V_{TH-} thresholds, the output is indeterminate. The receiver output is in the Hi-Z state and the magnitude and polarity of V_{ID} are irrelevant when the $\overline{RE}$ pin is logic high or left open. The internal biasing of the receiver inputs causes the output to go to a failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

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10.4.1 Device I/O Schematics

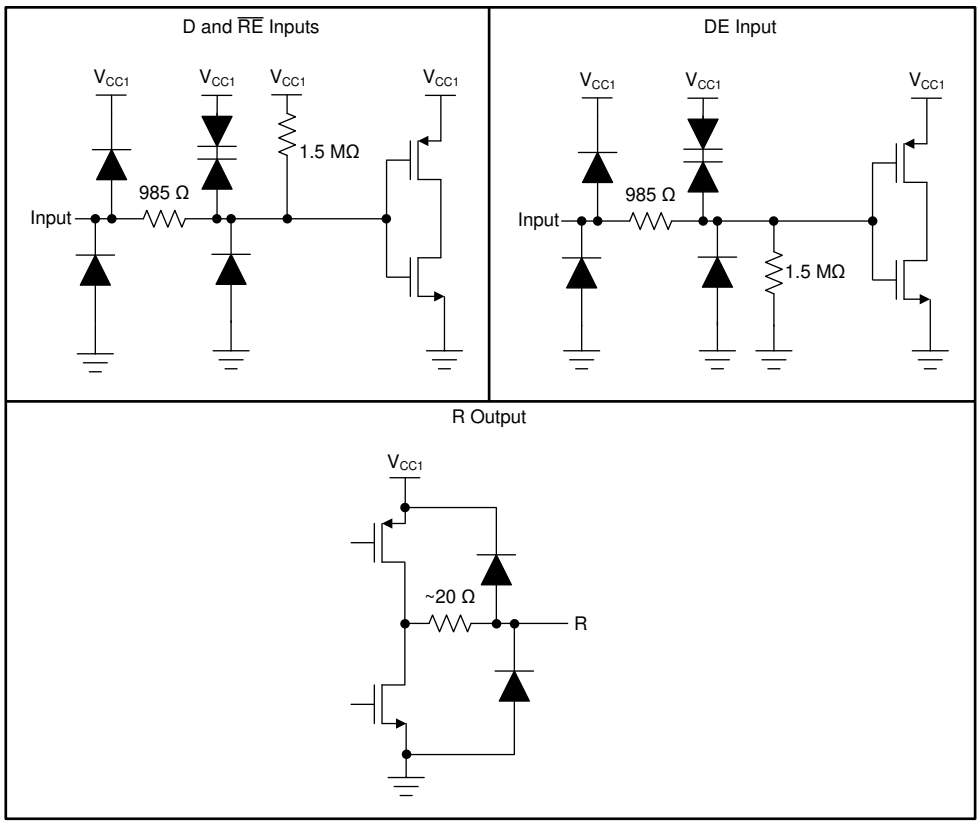


Figure 49. Device I/O Schematics

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11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The ISO14xx devices are designed for bidirectional data transfer on multipoint RS-485 networks. The design of each RS-485 node in the network requires an ISO14xx device and an isolated power supply as shown in Figure 52.

An RS-485 bus has multiple transceivers that connect in parallel to a bus cable. Both cable ends are terminated with a termination resistor, R_T, to remove line reflections. The value of R_T matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, lets higher data rates be used over a longer cable length.

Full-duplex implementation, as shown in Figure 50, requires two signal pairs (four wires). Full-duplex implementation lets each node to transmit data on one pair while simultaneously receiving data on the other pair. In half-duplex implementation, as shown in Figure 51, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements.

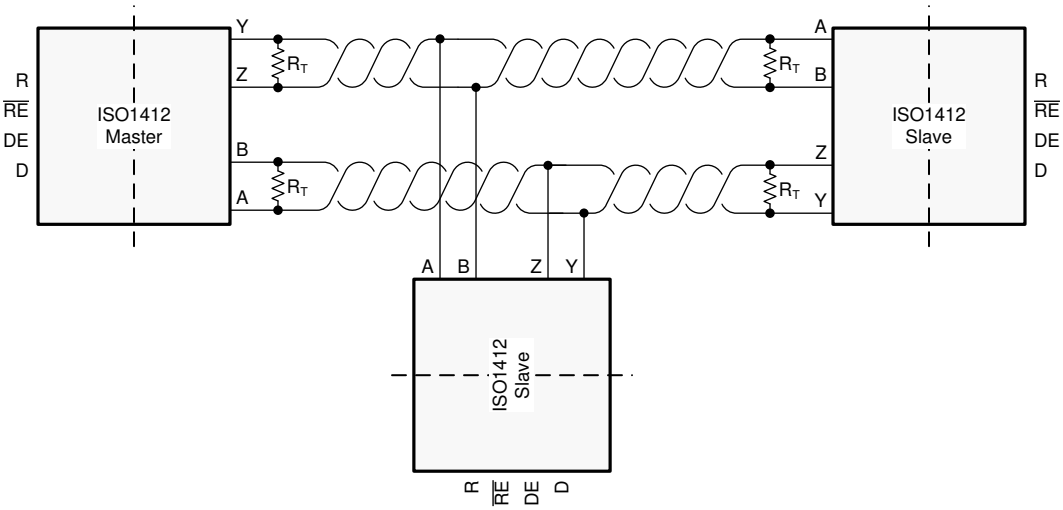


Figure 50. Typical RS-485 Network With Full-Duplex Isolated Transceivers

Application Information (continued)

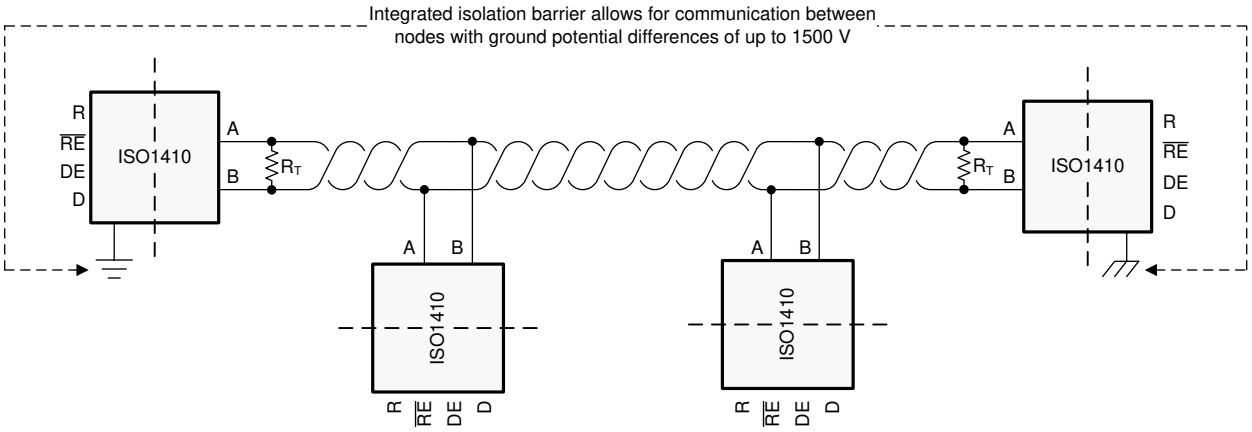


Figure 51. Typical RS-485 Network With Half-Duplex Isolated Transceivers

11.2 Typical Application

Figure 52 shows the application circuit of the ISO1410 device.

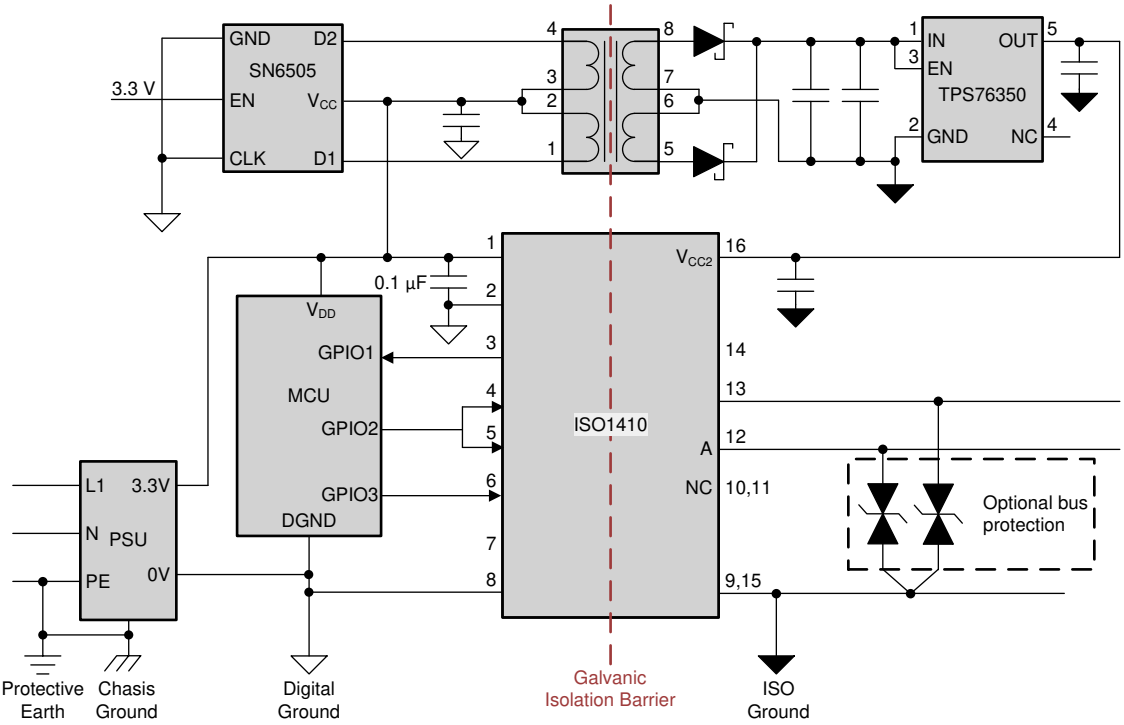


Figure 52. Application Circuit of ISO1410

11.2.1 Design Requirements

Unlike an optocoupler-based solution, which requires several external components to improve performance, provide bias, or limit current, the ISO14xx devices only require external bypass capacitors to operate.

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Typical Application (continued)

11.2.2 Detailed Design Procedure

The RS-485 bus is a robust electrical interface suitable for long-distance communications. The RS-485 interface can be used in a wide range of applications with varying requirements of distance of communication, data rate, and number of nodes.

11.2.2.1 Data Rate and Bus Length

The RS-485 standard has typical curves similar to those shown in Figure 53. These curves show the inverse relationship between signaling rate and cable length. If the data rate of the payload between two nodes is lower, the cable length between the nodes can be longer.

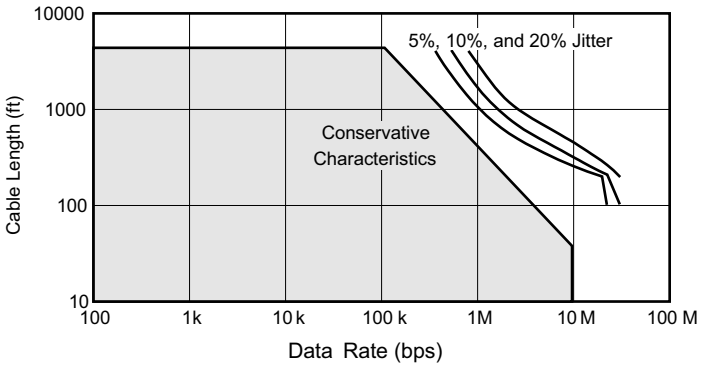


Figure 53. Cable Length vs Data Rate Characteristics

Use Figure 53 as a guideline for cable selection, data rate, cable length and subsequent jitter budgeting.

11.2.2.2 Stub Length

In an RS-485 network, the distance between the transceiver inputs and the cable trunk is known as the *stub*. The stub should be as short as possible when a node is connected to the bus. Stubs are a non-terminated piece of bus line that can introduce reflections of varying phase as the length of the stub increases. The electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver as a general guideline. Therefore, the maximum physical stub length ($L_{(STUB)}$) is calculated as shown in Equation 3.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (3)$$

where

- t_r is the 10/90 rise time of the driver.
- c is the speed of light (3×10^8 m/s).
- v is the signal velocity of the cable or trace as a factor of c.

11.2.2.3 Bus Loading

The current supplied by the driver must supply into a load because the output of the driver depends on this current. Add transceivers to the bus to increase the total bus loading. The RS-485 standard specifies a hypothetical term of a unit load (UL) to estimate the maximum number of possible bus loads. The UL represents a load impedance of approximately 12 kΩ. Standard-compliant drivers must be able to drive 32 of these ULs.

The ISO14xx devices have 1/8 UL impedance transceiver and can connect up to 256 nodes to the bus.

11.2.3 Application Curves

Below eye diagram of ISO145x device indicates low jitter and wide open eye at maximum data rate of 50 Mbps.

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Typical Application (continued)

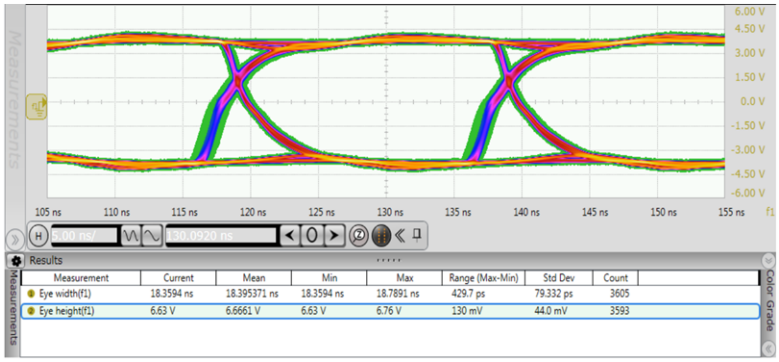


Figure 54. Eye Diagram at 50 Mbps Clock, V_{CC2} = 5 V, 25°C

11.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 55 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 56 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1060 V_{RMS} with a lifetime of 220 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 is specified up to 1060 V_{RMS} . At the lower working voltages, the corresponding insulation lifetime is much longer than 220 years.

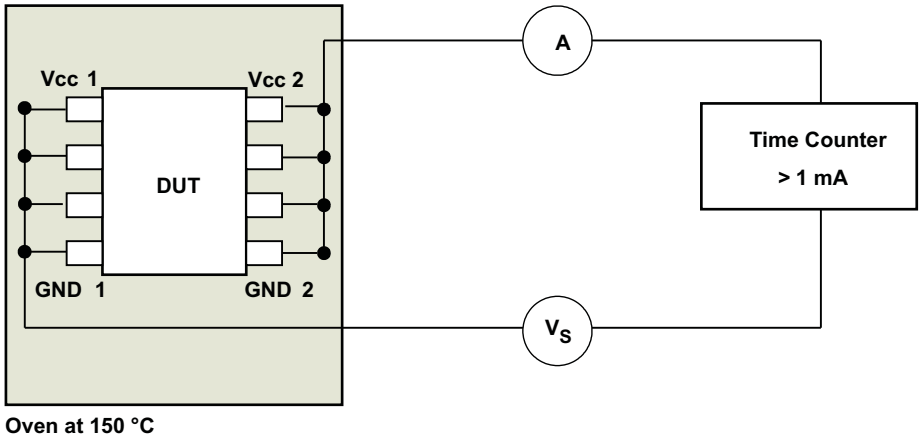
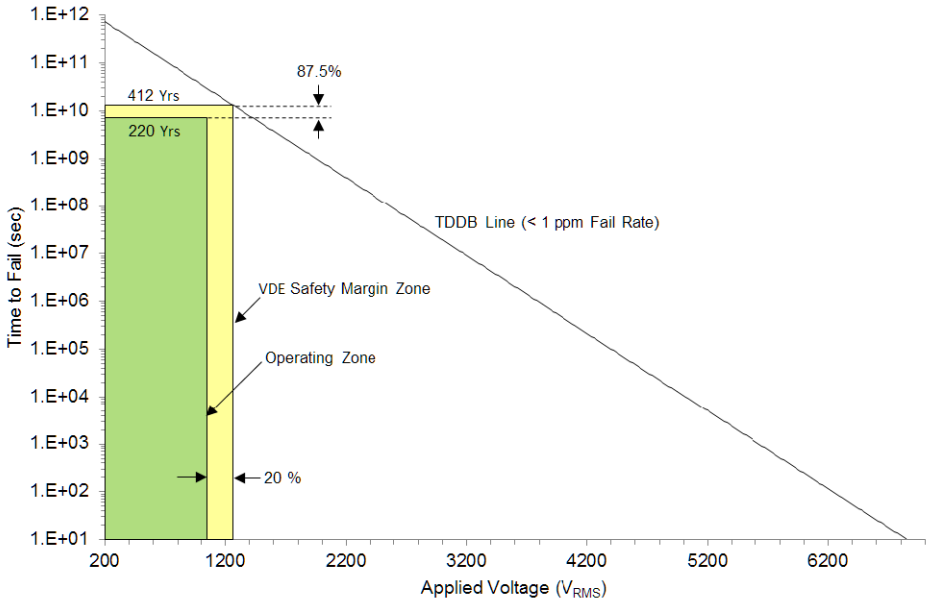


Figure 55. Test Setup for Insulation Lifetime Measurement

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Typical Application (continued)



Working Isolation Voltage = 1060 V_{RMS} Projected Insulation Lifetime = 220 Years

T_A up to 150°C Applied Voltage Frequency = 60 Hz

Figure 56. Insulation Lifetime Projection Data

12 Power Supply Recommendations

To make sure device operation is reliable at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the logic and transceiver supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as near to the supply pins as possible. Additionally, a 10 µF bulk capacitor on V_{CC2} improves transceiver performance during bus transitions in transmit mode. If only one primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6505B device. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

13 Layout

13.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 57). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

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Layout Guidelines (continued)

Figure 58 shows the recommended placement and routing of the device bypass capacitors and optional TVS diodes. Put the V_{CC2} bypass capacitors on the top layer and as near to the device pins as possible. Do not use vias to complete the connection to the V_{CC2} and GND2 pins. If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the *Digital Isolator Design Guide* for detailed layout recommendations.

13.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

13.2 Layout Example

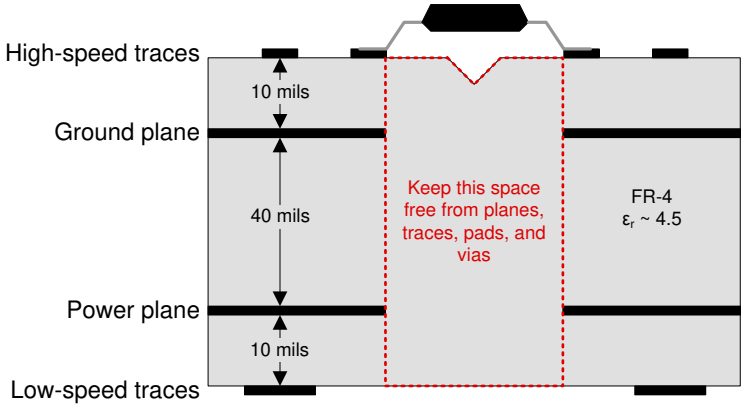


Figure 57. Recommended Layer Stack

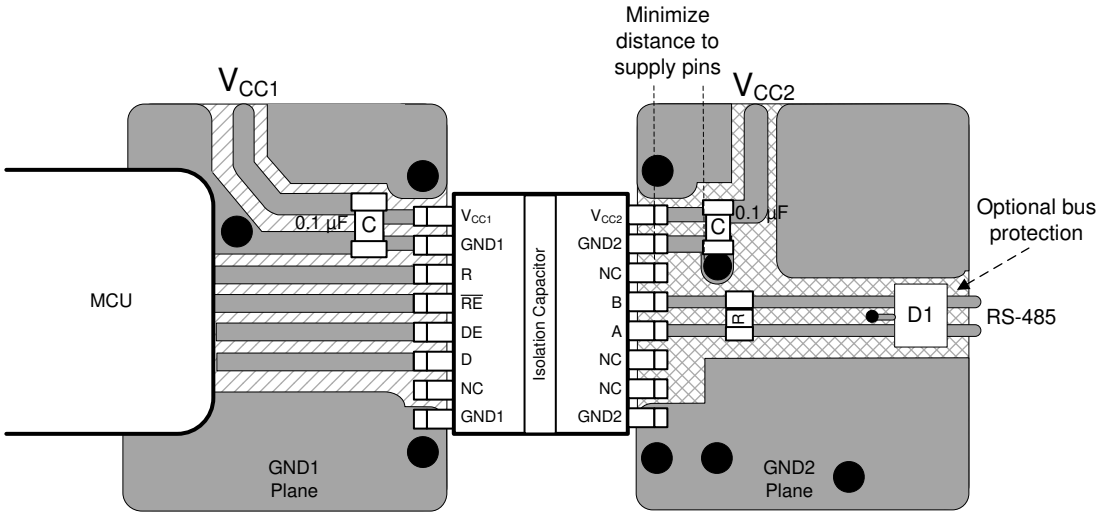


Figure 58. Layout Example

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14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *Isolated RS-485 Half-Duplex Evaluation Module* user's guide
- Texas Instruments, *How to isolate signal and power for an RS-485 system* TI TechNote
- Texas Instruments, *Robust Isolated RS-485 for industrial long-haul communications* TI TechNote

14.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO1410	Click here	Click here	Click here	Click here	Click here
ISO1412	Click here	Click here	Click here	Click here	Click here
ISO1430	Click here	Click here	Click here	Click here	Click here
ISO1432	Click here	Click here	Click here	Click here	Click here
ISO1450	Click here	Click here	Click here	Click here	Click here
ISO1452	Click here	Click here	Click here	Click here	Click here
ISO1410B	Click here	Click here	Click here	Click here	Click here
ISO1412B	Click here	Click here	Click here	Click here	Click here
ISO1430B	Click here	Click here	Click here	Click here	Click here
ISO1432B	Click here	Click here	Click here	Click here	Click here
ISO1450B	Click here	Click here	Click here	Click here	Click here
ISO1452B	Click here	Click here	Click here	Click here	Click here

14.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.4 Community Resource

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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14.5 Trademarks

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All other trademarks are the property of their respective owners.

14.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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14.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1410BDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1410B	Samples
ISO1410BDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1410B	Samples
ISO1410DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1410	Samples
ISO1410DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1410	Samples
ISO1412BDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1412B	Samples
ISO1412BDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1412B	Samples
ISO1412DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1412	Samples
ISO1412DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1412	Samples
ISO1430BDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1430B	Samples
ISO1430BDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1430B	Samples
ISO1430DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1430	Samples
ISO1430DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1430	Samples
ISO1432BDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1432B	Samples
ISO1432BDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1432B	Samples
ISO1432DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1432	Samples
ISO1432DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1432	Samples
ISO1450BDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1450B	Samples
ISO1450BDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1450B	Samples
ISO1450DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1450	Samples
ISO1450DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1450	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1452BDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1452B	Samples
ISO1452BDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1452B	Samples
ISO1452DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1452	Samples
ISO1452DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO1452	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

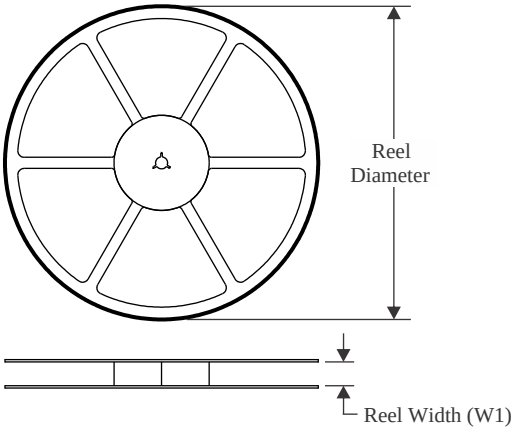
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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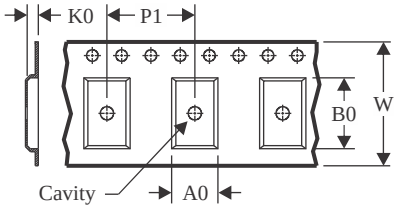
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

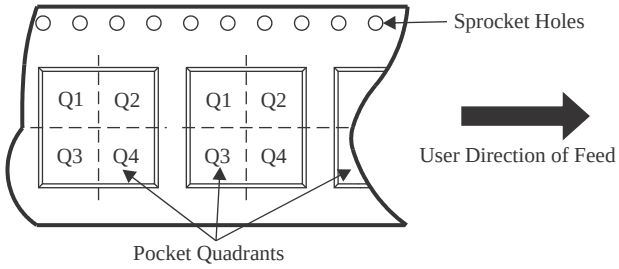


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

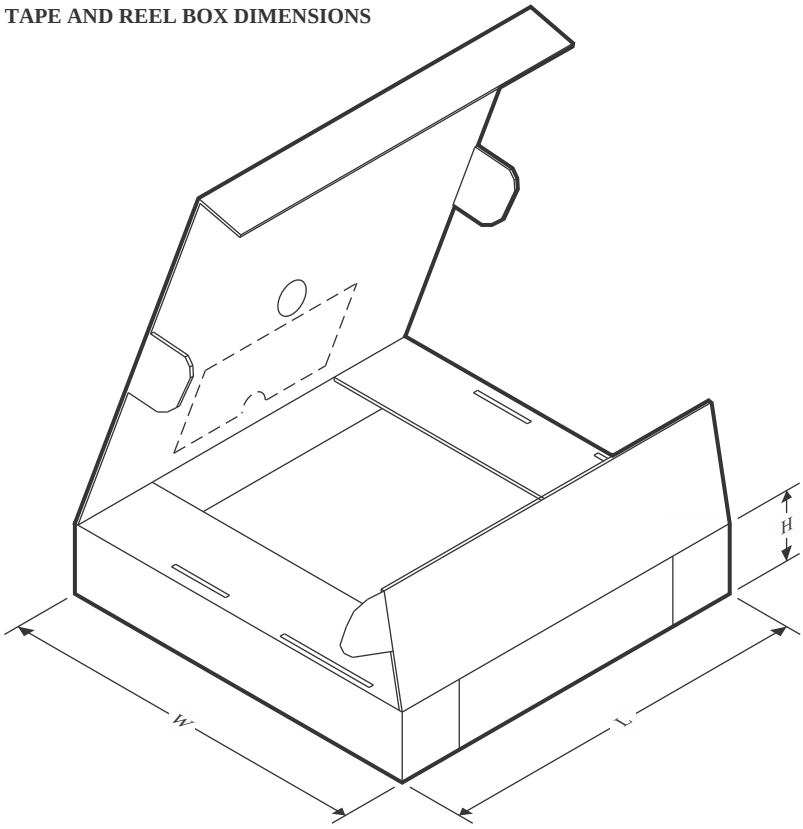


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1410BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1410BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1410DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1410DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1412BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1412BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1412DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1412DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1430BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1430BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1430DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1432BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1432BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1432DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1432DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1450BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1450DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1452BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1452DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

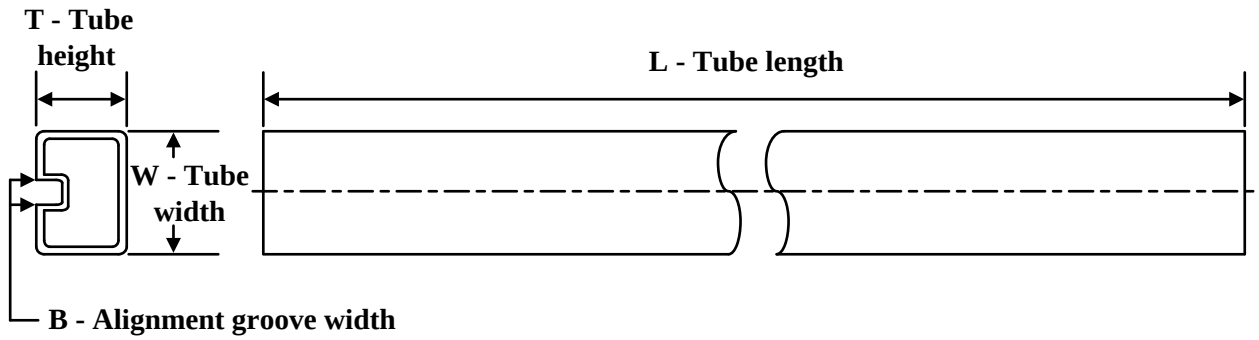


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1410BDWR	SOIC	DW	16	2000	356.0	356.0	35.0
ISO1410BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1410DWR	SOIC	DW	16	2000	356.0	356.0	35.0
ISO1410DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1412BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1412BDWR	SOIC	DW	16	2000	356.0	356.0	35.0
ISO1412DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1412DWR	SOIC	DW	16	2000	356.0	356.0	35.0
ISO1430BDWR	SOIC	DW	16	2000	356.0	356.0	35.0
ISO1430BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1430DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1432BDWR	SOIC	DW	16	2000	356.0	356.0	35.0
ISO1432BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1432DWR	SOIC	DW	16	2000	356.0	356.0	35.0
ISO1432DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1450BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1450DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1452BDWR	SOIC	DW	16	2000	350.0	350.0	43.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1452DWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO1410BDW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1410BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1410DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1410DW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1412BDW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1412BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1412DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1412DW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1430BDW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1430BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1430DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1430DW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1432BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1432BDW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1432DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1432DW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1450BDW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1450BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1450DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1450DW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1452BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1452BDW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1452DW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO1452DW	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

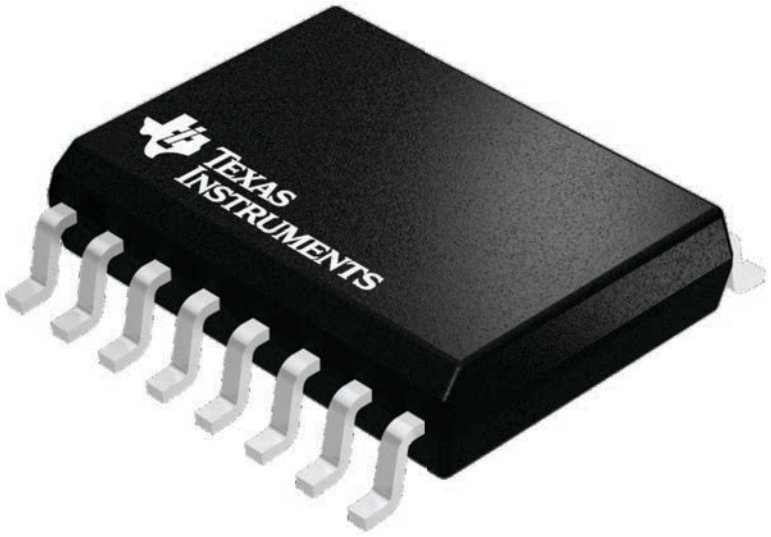
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

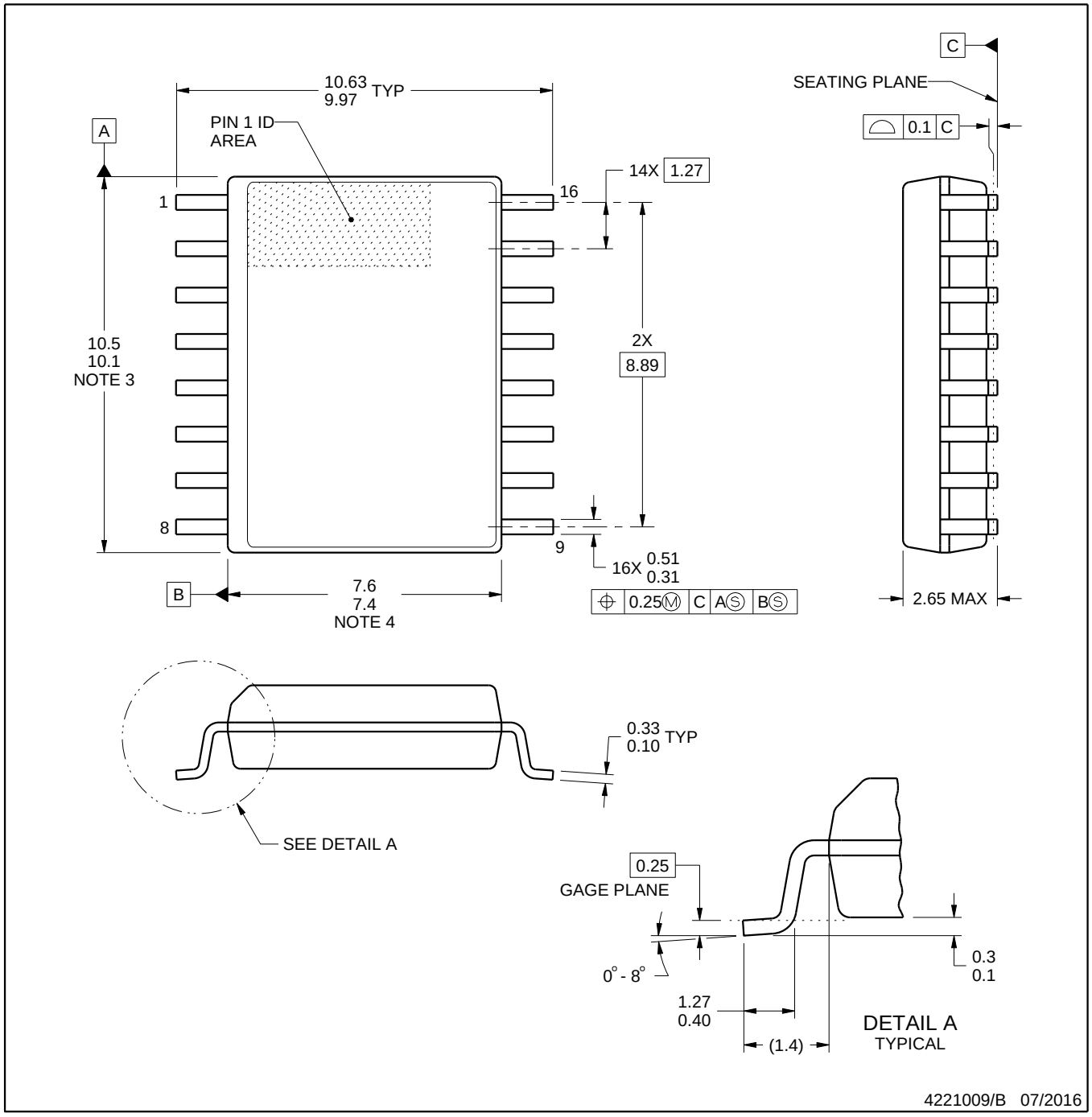
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



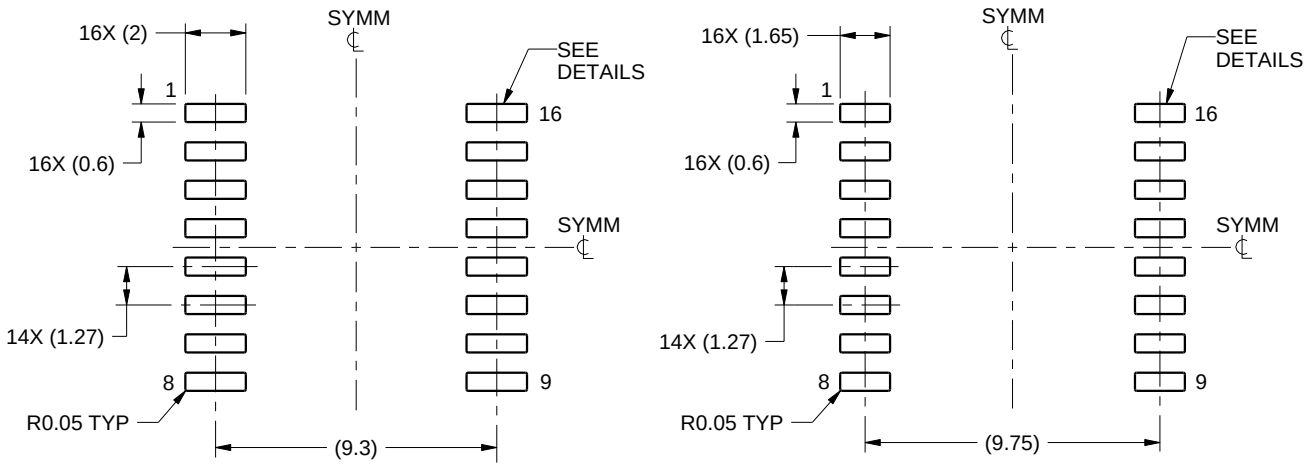
4224780/A

SOIC



NOTES:

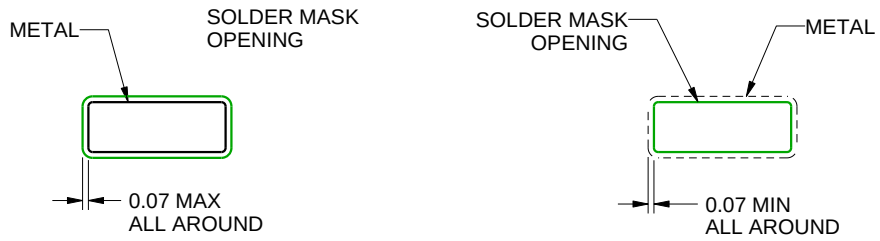
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

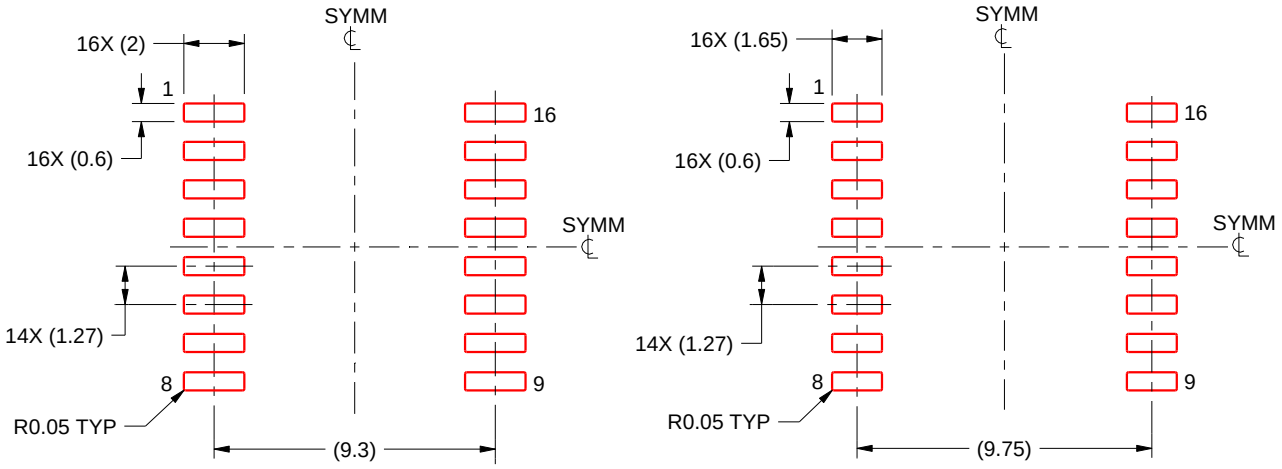
SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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