9QXL2000C

20-Output Enhanced DB2000Q

The 9QXL2000C is a 20-output very-low-additive phase jitter fanout buffer for PCIe Gen6. It offers integrated terminations for 85Ω transmission lines.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers
- Storage
- Networking
- SSDs

Output Features

20 Low-Power HCSL (LP-HCSL) 85Ω output pairs

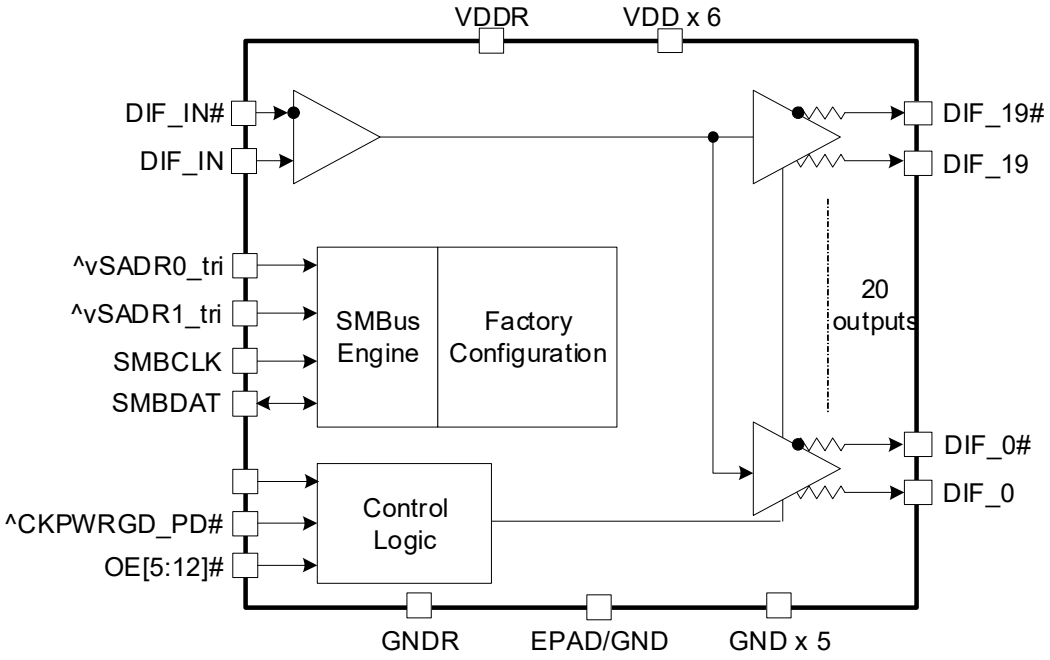
Features

- Low-Power HCSL (LP-HCSL) 85Ω outputs eliminate 80 resistors, saving 130mm^2 of area
- Low-Power HCSL (LP-HCSL) outputs reduce device power consumption by 50%
- 8 OE# pins configurable to control up to 20 outputs
- 9 selectable SMBus addresses
- Spread spectrum compatible
- 10 × 10 mm 72-VFQFPN package

Key Specifications

- Output-to-output skew: < 50ps
- Additive phase jitter: DB2000Q < 12fs RMS
- Additive Phase jitter: PCIe Gen5 <7fs RMS
- Additive Phase jitter: PCIe Gen6 < 5fs RMS
- DB2000Q v1.1 pinout

Block Diagram



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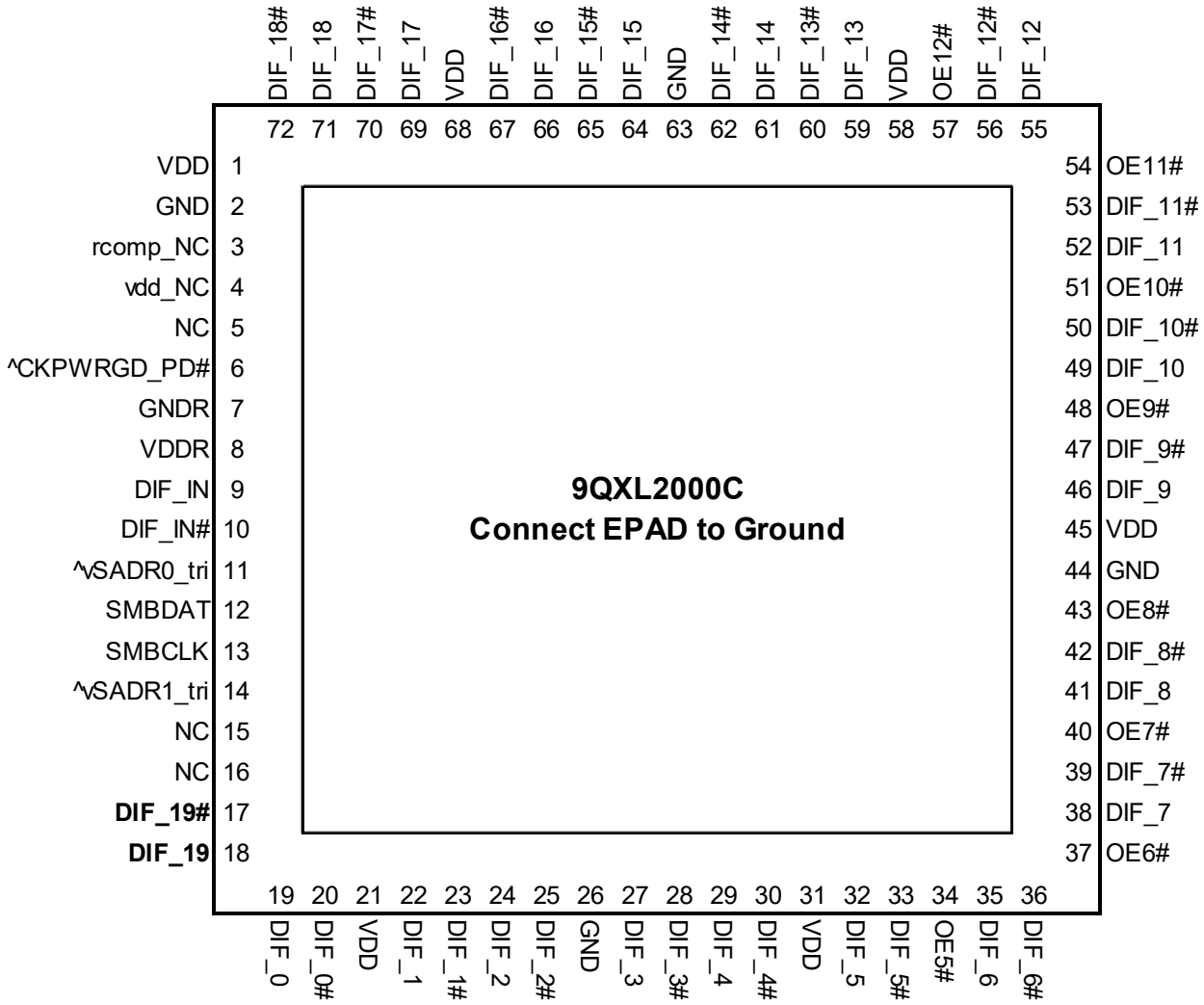
1. Pin Information

1.1 Signal Types

Term	Description
I	Input
O	Input
OD	Open Drain Output
I/O	Bi-Directional
PD	Pull-down
PU	Pull-up
Z	Tristate
D	Driven
X	Don’t care
SE	Single ended
DIF	Differential
PWR	3.3 V power
GND	Ground
PDT	Power Down Tolerant: These signals must tolerate being driven when the device is powered down.

Note that some pins have both internal pull-up and pull-down resistors which bias the pins to VDD/2.

1.2 Pin Assignments



72-VFQFPN (10 x 10 mm, 0.5mm pad pitch)

^ prefix indicates an internal pull-up resistor
v prefix indicates an internal pull-down resistor
^v prefix indicates an internal pull-up and pull-down resistor

1.2.1 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	VDD	PWR	Power supply, nominally 3.3V.
2	GND	GND	Ground pin.
3	rcomp_NC	-	The DB2000Q specification calls this pin RCOMP. This pin is a true No Connect on the 9QXL2000 device, since it is not needed. Any existing connections on the board may remain to support non-DB2000Q devices.
4	vdd_NC	-	The DB2000Q specification calls this pin VDD. This pin is a true No Connect on the 9QXL2000 device, since it is not needed. Any existing connections on the board may remain to support non-DB2000Q devices.
5	NC	-	No connection.

Pin Number	Pin Name	Type	Description
6	^CKPWRGD_PD#	I, SE, PU, PDT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
7	GNDR	GND	Analog ground pin for the differential input (receiver).
8	VDDR	PWR	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
9	DIF_IN	I, DIF, PDT	HCSL true input.
10	DIF_IN#	I, DIF, PDT	HCSL complementary input.
11	^vSADR0_tri	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has internal pull up/down resistors to bias to VDD/2. See the SMBus Addressing table.
12	SMBDAT	I/O, SE, OD, PDT	Data pin of SMBUS circuitry
13	SMBCLK	I, SE, PDT	Clock pin of SMBUS circuitry
14	^vSADR1_tri	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has internal pull up/down resistors to bias to VDD/2. See the SMBus Addressing table.
15	NC	-	No connection.
16	NC	-	No connection.
17	DIF_19#	O, DIF	HCSL complementary clock output.
18	DIF_19	O, DIF	HCSL true clock output.
19	DIF_0	O, DIF	HCSL true clock output.
20	DIF_0#	O, DIF	HCSL complementary clock output.
21	VDD	PWR	Power supply, nominally 3.3V.
22	DIF_1	O, DIF	HCSL true clock output.
23	DIF_1#	O, DIF	HCSL complementary clock output.
24	DIF_2	O, DIF	HCSL true clock output.
25	DIF_2#	O, DIF	HCSL complementary clock output.
26	GND	GND	Ground pin.
27	DIF_3	O, DIF	HCSL true clock output.
28	DIF_3#	O, DIF	HCSL complementary clock output.
29	DIF_4	O, DIF	HCSL true clock output.
30	DIF_4#	O, DIF	HCSL complementary clock output.
31	VDD	PWR	Power supply, nominally 3.3V.
32	DIF_5	O, DIF	HCSL true clock output.
33	DIF_5#	O, DIF	HCSL complementary clock output.
34	OE5#	I, SE, PU, PDT	Active low input for enabling output 5. 1 = disable output, 0 = enable output.

Pin Number	Pin Name	Type	Description
35	DIF_6	O, DIF	HCSL true clock output.
36	DIF_6#	O, DIF	HCSL complementary clock output.
37	OE6#	I, SE, PU, PDT	Active low input for enabling output 6. 1 = disable output, 0 = enable output.
38	DIF_7	O, DIF	HCSL true clock output.
39	DIF_7#	O, DIF	HCSL complementary clock output.
40	OE7#	I, SE, PU, PDT	Active low input for enabling output 7. 1 = disable output, 0 = enable output.
41	DIF_8	O, DIF	HCSL true clock output.
42	DIF_8#	O, DIF	HCSL complementary clock output.
43	OE8#	I, SE, PU, PDT	Active low input for enabling output 8. 1 = disable output, 0 = enable output.
44	GND	GND	Ground pin.
45	VDD	PWR	Power supply, nominally 3.3V.
46	DIF_9	O, DIF	HCSL true clock output.
47	DIF_9#	O, DIF	HCSL complementary clock output.
48	OE9#	I, SE, PU, PDT	Active low input for enabling output 9. 1 = disable output, 0 = enable output.
49	DIF_10	O, DIF	HCSL true clock output.
50	DIF_10#	O, DIF	HCSL complementary clock output.
51	OE10#	I, SE, PU, PDT	Active low input for enabling output 10. 1 = disable output, 0 = enable output.
52	DIF_11	O, DIF	HCSL true clock output.
53	DIF_11#	O, DIF	HCSL complementary clock output.
54	OE11#	I, SE, PU, PDT	Active low input for enabling output 11. 1 = disable output, 0 = enable output.
55	DIF_12	O, DIF	HCSL true clock output.
56	DIF_12#	O, DIF	HCSL complementary clock output.
57	OE12#	I, SE, PU, PDT	Active low input for enabling output 12. 1 = disable output, 0 = enable output.
58	VDD	PWR	Power supply, nominally 3.3V.
59	DIF_13	O, DIF	HCSL true clock output.
60	DIF_13#	O, DIF	HCSL complementary clock output.
61	DIF_14	O, DIF	HCSL true clock output.
62	DIF_14#	O, DIF	HCSL complementary clock output.
63	GND	GND	Ground pin.
64	DIF_15	O, DIF	HCSL true clock output.
65	DIF_15#	O, DIF	HCSL complementary clock output.
66	DIF_16	O, DIF	HCSL true clock output.

Pin Number	Pin Name	Type	Description
67	DIF_16#	O, DIF	HCSL complementary clock output.
68	VDD	PWR	Power supply, nominally 3.3V.
69	DIF_17	O, DIF	HCSL true clock output.
70	DIF_17#	O, DIF	HCSL complementary clock output.
71	DIF_18	O, DIF	HCSL true clock output.
72	DIF_18#	O, DIF	HCSL complementary clock output.
73	EPAD	GND	Connect EPAD to ground.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply Voltage [1][2]	V_{DDx}		-	-	3.9	V
Input Low Voltage [1]	V_{IL}		GND - 0.5	-	-	V
Input High Voltage [3]	V_{IH}	Except for SMBus interface.	-	-	V_{DD} + 0.5	V
Input High Voltage [1]	V_{IHSMB}	SMBus clock and data pins.	-	-	3.9	V
Storage Temperature [1]	Ts		-65	-	150	°C
Junction Temperature [1]	Tj	Maximum operating junction temperature.	-	-	125	°C

1. Confirmed by design and characterization, not 100% tested in production.
2. Operation under these conditions is neither implied nor guaranteed.
3. Not to exceed 3.9V.

2.2 ESD Ratings

ESD Model/Test	Symbol	Rating	Unit
Human Body Model (JESD22-A114 (JS-001) Classification)	ESD prot	2000	V
Charged Device Model (JESD22-C101 Classification)	ESD prot	500	V

2.3 Electrical Specifications

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 1. SMBus Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
SMBus Input Low Voltage	V_{ILSMB}		-	-	0.8	V
SMBus Input High Voltage	V_{IHSMB}		2.1	-	V_{DDSMB}	V
SMBus Output Low Voltage	V_{OLSMB}	At $I_{PULLUP.}$	-	-	0.4	V
SMBus Sink Current	I_{PULLUP}	At $V_{OL.}$	4	-	-	mA
Nominal Bus Voltage [1]	V_{DDSMB}		2.7	-	3.6	V
SMBCLK/SMBDAT Rise Time [1]	t_{RSMB}	(Max V_{IL} - 0.15V) to (Min V_{IH} + 0.15V).	-	-	1000	ns
SMBCLK/SMBDAT Fall Time [1]	t_{FSMB}	(Min V_{IH} + 0.15V) to (Max V_{IL} - 0.15V).	-	-	300	ns
SMBus Operating Frequency [2]	f_{SMBMAX}	Maximum SMBus operating frequency.	-	-	400	kHz

1. Confirmed by design and characterization, not 100% tested in production.
2. The device must be powered up with CKPWRGD_PD# = '1' for the SMBus to be active.

Table 2. DIF_IN Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Crossover Voltage – DIF_IN [1]	V_{CROSS}	Cross over voltage.	100	-	1400	mV
Input Swing – DIF_IN [1]	V_{SWING}	Differential value.	200	-	-	mV
Input Slew Rate – DIF_IN [1][2]	dv/dt	Measured differentially.	0.6	-	-	V/ns
Input Current	I_{IH}	DIF_IN, V_{IN} = 0.8V	-3	-	3	µA
		DIF_IN#, V_{IN} = 0.8V	5	-	15	µA
	I_{IL}	DIF_IN, V_{IN} = GND	-12	-	-6	µA
		DIF_IN#, V_{IN} = GND	-3	-	3	µA
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	45	-	55	%

1. See the Phase Jitter tables for values required for performance.
2. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero-crossing.

Table 3. Input/Supply/Common Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DDx}	Supply voltage for core and analog.	3.135	3.3	3.465	V
Ambient Operating Temperature	T_{AMB}	Extended Industrial range.	-40	25	105	°C
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, tri-level inputs.	2	-	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, tri-level inputs.	GND - 0.3	-	0.8	V

Table 3. Input/Supply/Common Parameters (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input High Voltage	V_{IH}	Tri-level inputs.	2.2	-	V_{DD} + 0.3	V
Input Mid Voltage	V_{IM}	Tri-level inputs.	1.2	V_{DD}/2	1.8	V
Input Low Voltage	V_{IL}	Tri-level inputs.	GND - 0.3	-	0.8	V
Input Current	I_{IH}	Single-ended inputs unless otherwise listed. Clock Inputs are listed in Table 2. V_{IN} = VDD.	25	-	35	µA
		CKPWRGD_PD#, V_{IN} = VDD.	-1	-	5	µA
		SADR[1:0]_tri, V_{IN} = VDD.	25	-	35	µA
Input Current	I_{IL}	Single-ended inputs unless otherwise listed. Clock Inputs are listed in Table 2. V_{IN} = GND.	-3	-	3	µA
		CKPWRGD_PD#, V_{IN} = GND.	-35	-	-20	µA
		SADR[1:0]_tri, V_{IN} = GND.	-35	-	-20	µA
Input Frequency	F_{IN}	-	1	-	400	MHz
Pin Inductance [1]	L_{pin}	-	-	-	7	nH
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5	-	5	pF
	C_{INDIF_IN}	DIF_IN differential clock inputs. [1][2]	1.5	-	2.7	pF
	C_{OUT}	Output pin capacitance.	-	-	6	pF
Clk Stabilization	T_{STAB}	Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. CKPWRGD_PD# tied to VDD in this case. [1][3]	-	1.2	3	ms
		VDD stable, measured from de-assertion of CKPWRGD_PD#. [1][3]	-	0.3	1.0	ms
OE# Latency [1][3][4]	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	4	5	10	clocks
Tfall [3]	t_F	Fall time of control inputs.	-	-	5	ns
Trise [3]	t_R	Rise time of control inputs.	-	-	5	ns

1. Confirmed by design and characterization, not 100% tested in production.
2. DIF_IN input.
3. Control input must be monotonic from 20% to 80% of input swing.
4. Time from deassertion until outputs are > 200mV.

Table 4. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current [1]	I_{DD}	V_{DD}, All outputs 100MHz, C_L = 2pF; Zo = 85Ω.	-	224	246	mA
	I_{DDR}	V_{DDR}. All outputs 100MHz, C_L = 2pF; Zo = 85Ω.	-	0.6	1.3	mA
Power Down Current [1]	I_{DDPD}	All differential pairs low-low.	-	3.5	5	mA
	I_{DDRRP}	All differential pairs low-low.	-	0.6	1.3	mA

1. This is the sum of VDD and VDDA on the 9QXL2000C.

Table 5. Skew and Differential Jitter Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
CLK_IN, DIF[x:0]	t_{PD}	Input-to-output skew. [1][2][3][4][5][6]	1.2	1.4	1.6	ns
CLK_IN, DIF[x:0]	$t_{PDVARIATION}$	Input-to-output skew variation for a given device at a given voltage.[1][2][3][5][7]	1.1	1.2	1.4	ps/°C
DIF[x:0]	t_{SKEW_ALL}	Output-to-output skew across all outputs. [1][2][3][6]	26	38	50	ps

1. Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input. Slew rate set to fast.
2. Measured from differential cross-point to differential cross-point.
3. All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.
4. Measured with scope averaging on to find mean value.
5. Confirmed by design and characterization, not 100% tested in production.
6. Measured from differential waveform.
7. This is the amount of input-to-output delay variation with respect to temperature. 2 ps/°C is equivalent to 250ps over the -40°C to +85°C temperature range.
8. Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.

Table 6. LP-HCSL Outputs Driving High-Impedance Receiver at 100MHz [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits [2]	Unit
Maximum Voltage [3][4]	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).	-	-	1092	1150	mV
Minimum Voltage [3][5]	Vmin		-112	-	-	-300	
Voltage High [3]	Vhigh	Vhigh set to default (800mV).	741	866	994	N/A	mV
Voltage Low [3]	Vlow		-101	-17	67		
Crossing Voltage (abs) [3][6]	Vcross_abs	Scope averaging off.	318	414	490	250 – 550	mV
Crossing Voltage (var) [3][6][7][8]	Δ-Vcross	Scope averaging off.	-	1	77	140	
Slew Rate [9][10]	dV/dt	Scope averaging on, fast slew rate.	2.1	3.0	4.0	1 – 4	V/ns
		Scope averaging on, slow slew rate.	1.6	2.4	3.3	1.5 – 3.5	

Table 6. LP-HCSL Outputs Driving High-Impedance Receiver at 100MHz (Cont.) [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits [2]	Unit
Rise/Fall Matching [3][11]	ΔtR/tF	Single-ended measurement fast slew rate.	-	4.1	19.4	20	%
		Single-ended measurement slow slew rate.	-	3.6	15.5	20	
Output Duty Cycle [9]	t_{DC}	VT = 0V, Differential. 50% duty cycle input	49.4	49.9	50.4	45 – 55	%

1. Standard high impedance load with CL = 2pF. See Test Loads
2. The specification limits are taken from either the PCIe Base Specification Revision 6.0, Version 1.0 or from relevant processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 7. PCIe Refclk Additive Phase Jitter - Normal Conditions

Parameter	Symbol	Conditions [1]	Typical	Maximum	Industry Limits	Unit
PCIe Gen1 (2.5 GT/s) [2][3][4][5]	$t_{jphPCIeG1-CC}$	Additive Phase Jitter, Common Clocked Architecture	528	623	86,000	fs pk-pk
PCIe Gen2 Hi-Band (5.0 GT/s) [2][3][4][5]	$t_{jphPCIeG2-CC}$		32	37	3,000	fs RMS
PCIe Gen2 Lo-Band (5.0 GT/s) [2][3][4][5]			9	11	3,100	
PCIe Gen3 (8.0 GT/s) [2][3][4][5]	$t_{jphPCIeG3-CC}$		15	18	1,000	
PCIe Gen4 (16.0 GT/s) [2][3][4][5][6]	$t_{jphPCIeG4-CC}$		15	18	500	
PCIe Gen5 (32.0 GT/s) [2][3][4][5][7]	$t_{jphPCIeG5-CC}$		6	7	150	
PCIe Gen6 (64.0 GT/s) [2][3][4][5][8]	$t_{jphPCIeG6-CC}$		3.5	4.1	100	
PCIe Gen2 IR (5.0 GT/s) [2][3][9]	$t_{jphPCIeG2-IR}$	IR (SRNS, SRIS) Architecture	41	48	N/A	fs RMS
PCIe Gen3 IR (8.0 GT/s) [2][3][5][9]	$t_{jphPCIeG3-IR}$		11	12		
PCIe Gen4 IR (16.0 GT/s) [2][3][9]	$t_{jphPCIeG4-IR}$		11	13		
PCIe Gen5 IR (32.0 GT/s) [2][3][9]	$t_{jphPCIeG5-IR}$		10	11		
PCIe Gen6 IR (64.0 GT/s) [2][3][9]	$t_{jphPCIeG6-IR}$		12	14		

1. Differential input swing = 1600mV and input slew rate = 3.5V/ns.
2. The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
3. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.
4. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of non-SSC content.
5. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
6. Note that 700fs RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 250fs RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 150fs RMS is to be used in channel simulations to account for additional noise in a real system.
9. The PCI Express Base Specification 6.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.

Table 8. PCIe Refclk Additive Phase Jitter - Degraded Conditions

Parameter	Symbol	Conditions [1]	Typical	Maximum	Industry Limits	Unit
PCIe Gen1 (2.5 GT/s) [2][3][4][5]	$t_{jphPCIeG1-CC}$	Additive Phase Jitter, Common Clocked Architecture	692	839	86,000	fs pk-pk
PCIe Gen2 Hi-Band (5.0 GT/s) [2][3][4][5]	$t_{jphPCIeG2-CC}$		41	49	3,000	fs RMS
PCIe Gen2 Lo-Band (5.0 GT/s) [2][3][4][5]			11	14	3,100	
PCIe Gen3 (8.0 GT/s) [2][3][4][5]	$t_{jphPCIeG3-CC}$		20	24	1,000	
PCIe Gen4 (16.0 GT/s) [2][3][4][5][6]	$t_{jphPCIeG4-CC}$		20	24	500	
PCIe Gen5 (32.0 GT/s) [2][3][4][5][7]	$t_{jphPCIeG5-CC}$		8	10	150	
PCIe Gen6 (64.0 GT/s) [2][3][4][5][8]	$t_{jphPCIeG6-CC}$		5	6	100	
PCIe Gen2 IR (5.0 GT/s) [2][3][9]	$t_{jphPCIeG2-IR}$	IR (SRNS, SRIS) Architecture	52	63	N/A	fs RMS
PCIe Gen3 IR (8.0 GT/s) [2][3][5][9]	$t_{jphPCIeG3-IR}$		14	17		
PCIe Gen4 IR (16.0 GT/s) [2][3][9]	$t_{jphPCIeG4-IR}$		14	17		
PCIe Gen5 IR (32.0 GT/s) [2][3][9]	$t_{jphPCIeG5-IR}$		12	15		
PCIe Gen6 IR (64.0 GT/s) [2][3][9]	$t_{jphPCIeG6-IR}$		15	19		

1. Differential input swing = 1600mV and input slew rate = 3.5V/ns.
2. The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
3. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.
4. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of non-SSC content.
5. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
6. Note that 700fs RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 250fs RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 150fs RMS is to be used in channel simulations to account for additional noise in a real system.
9. The PCI Express Base Specification 6.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.

Table 9. Non-PCIe Refclk Phase Jitter

Parameter	Symbol	Conditions	Typical	Maximum	Specification Limits	Unit
Additive Phase Jitter - Normal Conditions	$t_{jphDB2000Q}$	100MHz, Intel supplied filter. [1][2][3]	10	12	80 [4]	fs RMS
	$t_{jph12k-20M}$	156.25MHz (12kHz – 20MHz) [1][2][3]	30	36	N/A	
Additive Phase Jitter - Degraded Conditions	$t_{jphDB2000Q}$	100MHz, Intel supplied filter. [1][2][3]	10	12	80 [4]	fs RMS
	$t_{jph12k-20M}$	156.25MHz (12kHz – 20MHz) [1][2][3]	30	36	N/A	

1. See Test Loads for test configuration.
2. SMA100B used as signal source.
3. The 9QXL2000C devices meet all legacy QPI/UPI specifications by meeting the PCIe and DB2000Q specifications listed in this document.
4. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
5. Differential input swing = 1600mV and input slew rate = 3.5V/ns.
6. Differential input swing = 800mV and input slew rate = 1.5V/ns.

2.4 Power Management

Inputs					Outputs
CKPWRGD_PD#	**DIF_IN**	**OEx bit Byte[2:0]**	**OE Pin CFG bit Byte[8,9]**	**OEx# Pin**	**DIFx**
0	X	X	X	X	Low/Low
1	Running	0	X	X	Low/Low
		1	0	X	Running
1	Running	1	1	0	Running
		1	1	1	Low/Low

2.5 Power Connections

Pin Number		Description
V_{DD}	GND	
8	7	Analog Rx
1, 21, 31, 45, 58, 68	2, 26, 44, 63	DIF clocks

2.6 SMBus Addressing

Pin		SMBus Address (Read/Write bit = 0)
SMB_A1_tri	SMB_A0_tri	
0	0	D8
0	M	DA
0	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	1	CE

3. Test Loads

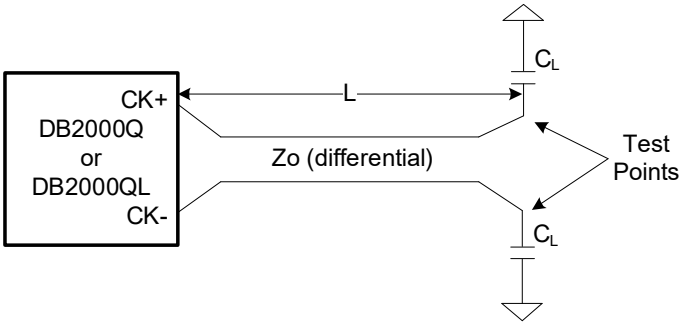


Figure 1. AC/DC Test Load for High Impedance Receivers

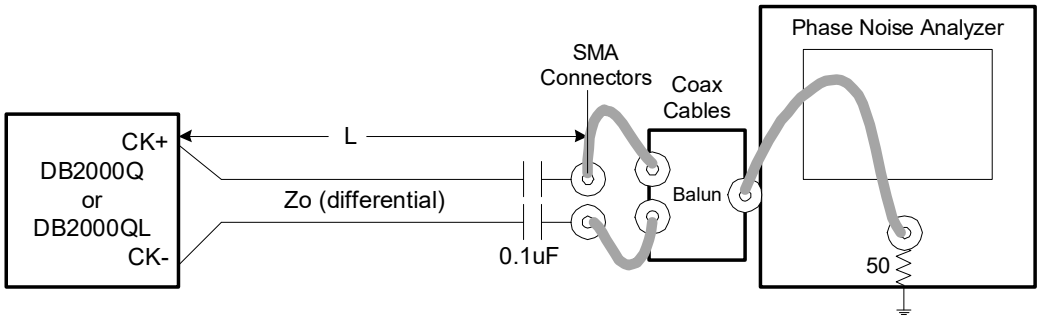


Figure 2. Test Setup for DB2000Q Additive Phase Jitter Measurement

Table 10. Parameters for Test Loads

Rs (Ω)	Zo (Ω)	L (cm)	C_L (pF)
Internal	85	30.5	2

4. Alternate Terminations

The LP-HCSL output can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with "Universal" Low-Power HCSL Outputs" for termination schemes for LVPECL, LVDS, CML and SSTL.

5. General SMBus Serial Interface Information

5.1 How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte**N – ByteN + X -1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

5.2 How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte**N + X - 1**
- Renesas clock sends **Byte0 – ByteX (if $X_{(H)}$ was written to Byte8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
	X Byte		ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 11. SMBus Output Enable Register

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	DIF_19_En	Output Enable	RW	Low/Low	Enable	1
Bit 5	DIF_18_En	Output Enable	RW	Low/Low	Enable	1
Bit 4	DIF_17_En	Output Enable	RW	Low/Low	Enable	1
Bit 3	DIF_16_En	Output Enable	RW	Low/Low	Enable	1
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

Table 12. SMBus Output Enable Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	DIF_7_En	Output Enable	RW	Low/Low	Pin Control (See Byte 8, 9 or 10)	1
Bit 6	DIF_6_En	Output Enable	RW			1
Bit 5	DIF_5_En	Output Enable	RW			1
Bit 4	DIF_4_En	Output Enable	RW			1
Bit 3	DIF_3_En	Output Enable	RW			1
Bit 2	DIF_2_En	Output Enable	RW			1
Bit 1	DIF_1_En	Output Enable	RW			1
Bit 0	DIF_0_En	Output Enable	RW			1

Table 13. SMBus Output Enable Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	DIF_15_En	Output Enable	RW	Low/Low	Pin Control (See Byte 8, 9 or 10)	1
Bit 6	DIF_14_En	Output Enable	RW			1
Bit 5	DIF_13_En	Output Enable	RW			1
Bit 4	DIF_12_En	Output Enable	RW			1
Bit 3	DIF_11_En	Output Enable	RW			1
Bit 2	DIF_10_En	Output Enable	RW			1
Bit 1	DIF_9_En	Output Enable	RW			1
Bit 0	DIF_8_En	Output Enable	RW			1

Table 14. SMBus Reserved Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	RB_OE12	Real Time Readback of OE#12	R	OE# pin Low	OE# Pin High	Real-time
Bit 6	RB_OE11	Real Time Readback of OE#11	R			Real-time
Bit 5	RB_OE10	Real Time Readback of OE#10	R			Real-time
Bit 4	RB_OE9	Real Time Readback of OE#9	R			Real-time
Bit 3	RB_OE8	Real Time Readback of OE#8	R			Real-time
Bit 2	RB_OE7	Real Time Readback of OE#7	R			Real-time
Bit 1	RB_OE6	Real Time Readback of OE#6	R			Real-time
Bit 0	RB_OE5	Real Time Readback of OE#5	R			Real-time

Byte 4 is Reserved

Table 15. SMBus Vendor and Revision ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	REVISION ID	R	B rev is 0001		0
Bit 6	RID2		R			0
Bit 5	RID1		R			x
Bit 4	RID0		R			x
Bit 3	VID3	VENDOR ID	R	Renesas/IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

Table 16. SMBus Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device ID 7 (MSB)		R	2000 is C8		1
Bit 6	Device ID 6		R			1
Bit 5	Device ID 5		R			0
Bit 4	Device ID 4		R			0
Bit 3	Device ID 3		R			1
Bit 2	Device ID 2		R			0
Bit 1	Device ID 1		R			x
Bit 0	Device ID 0		R			0

Table 17. SMBus OE Pin Configuration B Register

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	OE12#_CFGB	Controls DIF_13	RW	Does not Control	Controls	0
Bit 6	OE11#_CFGB	Controls DIF_14	RW			0
Bit 5	OE10#_CFGB	Controls DIF_15	RW			0
Bit 4	OE09#_CFGB	Controls DIF_0	RW			0
Bit 3	OE08#_CFGB	Controls DIF_1	RW			0
Bit 2	OE07#_CFGB	Controls DIF_2	RW			0
Bit 1	OE06#_CFGB	Controls DIF_3	RW			0
Bit 0	OE05#_CFGB	Controls DIF_4	RW			0

Table 18. SMBus OE Pin Configuration C and Output Amplitude Register

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	OE12#_CFGC	Controls DIF_16		Does not Control	Controls	0
Bit 6	OE11#_CFGC	Controls DIF_17				0
Bit 5	OE10#_CFGC	Controls DIF_18				0
Bit 4	OE09#_CFGC	Controls DIF_19				0
Bit 3	AMP[3]	Global Differential Output Control	RW	0.6V–1V 25mV/step. Default ~ 0.8V		0
Bit 2	AMP[2]		RW			1
Bit 1	AMP[1]		RW			1
Bit 0	AMP[0]		RW			1

Bytes 11–20 are Reserved

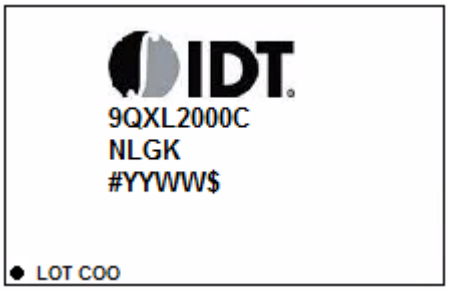
Table 19. SMBus PD_RESTORE

Byte 21	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	PD_RESTORE#	Save Configuration in Power Down	RW	Config Cleared	Config Saved	1
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram



- Lines 2 and 3: part number
  - “K” denotes extended temperature range
- Line 4:
  - “#” denotes the stepping number.
  - “YYWW” denotes the last two digits of the year and work-week the part was assembled.
  - “$” denotes the mark code.
- “LOT” denotes the lot number.
- “COO” denotes country of origin.

8. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
9QXL2000CNLGK	10 x 10 mm, 0.50mm pitch 72-VFQFPN	Trays	-40°C to +105°C
9QXL2000CNLGK8		Reel	

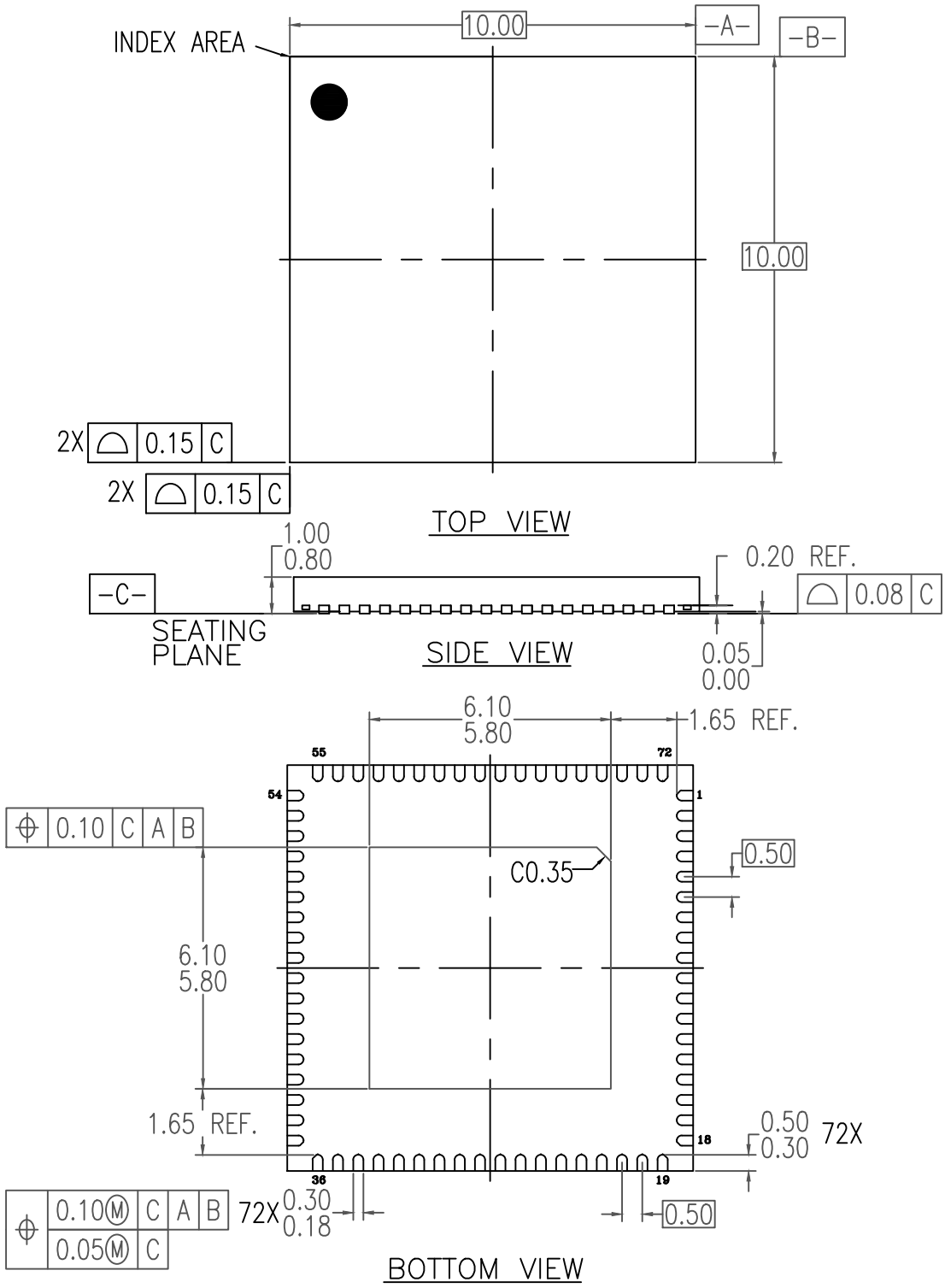
9. Revision History

Revision	Date	Description
1.01	Apr 5, 2022	▪ Inserted Signal Types table and updated Pin Types column in Pin Descriptions with latest nomenclature. ▪ Corrected footnote on Table 4 to reference 9QXL2000C instead of 9QXL2001C. ▪ Removed reference to ACP for FIN parameter and deleted extra line in Table 3. ▪ Assigned table numbers to SMBus registers. ▪ Corrected Byte 10[3:0] in Table 18 from 3 bits at 100mv/step to 4 bits at 25mV/ step.
1.00	Mar 31, 2022	Initial release.

72-VFQFPN, Package Outline Drawing

10.0 x 10.0 x 0.90 mm Body, Epad 5.95 x 5.95 mm 0.50mm Pitch

NLG72P1, PSC-4208-01, Rev 03, Page 1



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN1 IDENTIFIER)

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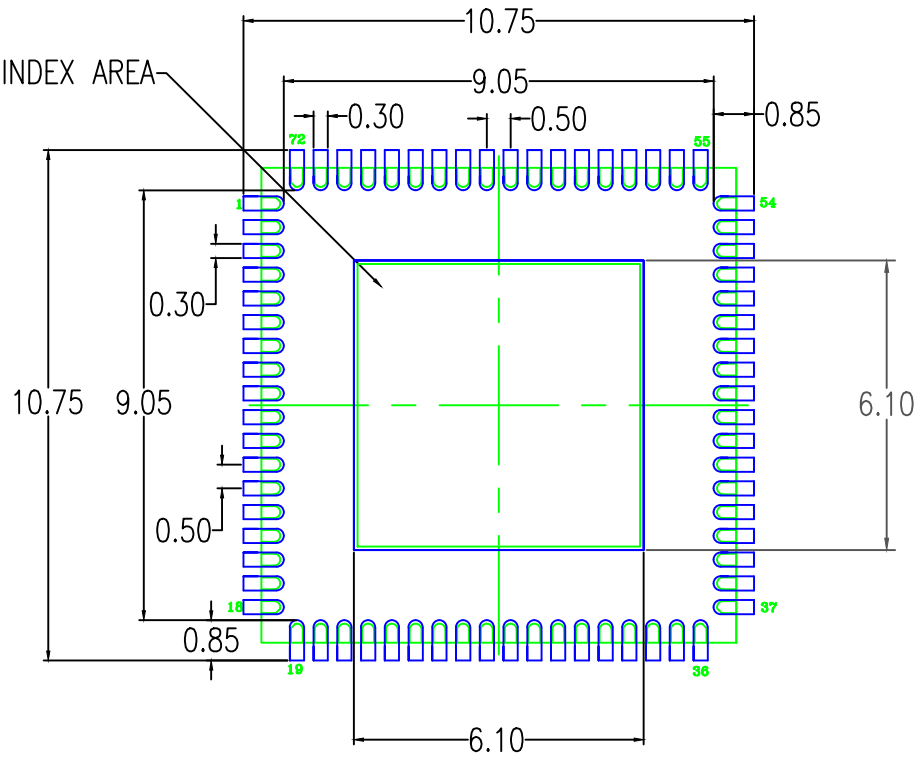

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 3, 2019	Rev 03	Update P1 Dimension from 5. 8 to 5.95 mm SQ
May 8, 2017	Rev 02	Change Package Code QFN to VFQFPN

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