

## Description

The 6V49205B is a main clock for Freescale P10xx and P20xx-based systems. It has a selectable System CCB clock and 2 DDRCLK speeds – 100M or 66.66M. The 6V49205B also provides LP-HCSL PCIe outputs for low power and reduced board space.

## Output Features

- 1 – Sys\_CCB 3.3V LVCMOS output at 100M/83.33M/80M/66.66M
- 1 – DDRCLK 3.3V LVCMOS output at 100M or 66.66M <sup>1</sup>
- 1 – 125M 3.3V LVCMOS output
- 6 – LP-HCSL PCIe pairs selectable at 100M or 125M
- 6 – 25MHz 3.3V LVCMOS outputs
- 2 – 2.048M 3.3V LVCMOS outputs
- 2 – USB 3.3V LVCMOS outputs at 12M or 24M

## Key Specifications

- PCIe Gen1–2–3 compliant
- <3p rms phase noise on REF outputs

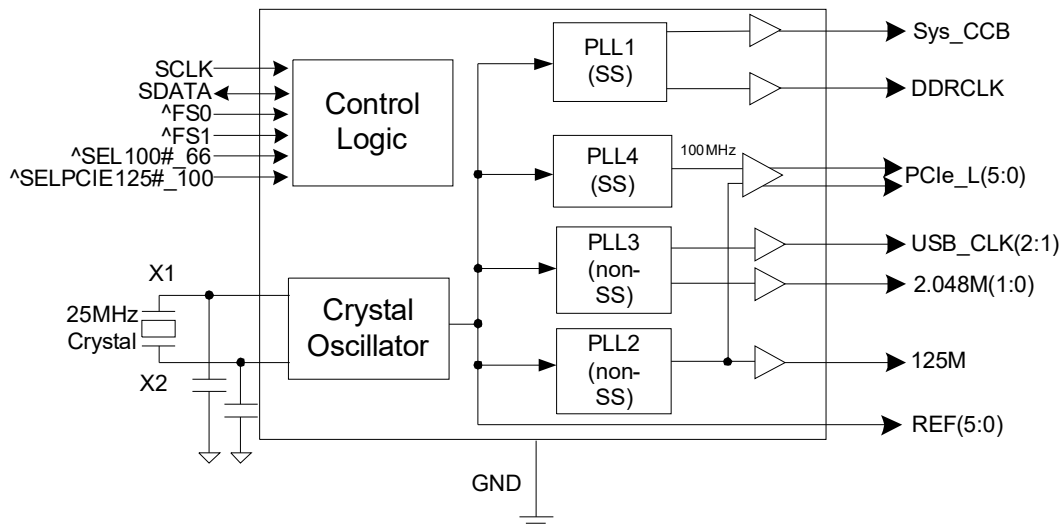
## Typical Applications

System Clock for Freescale P10xx and P20xx-based designs

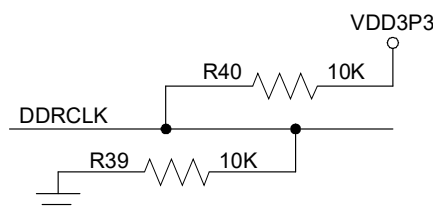
## Features

- Replaces 11 crystals, 2 oscillators and 3 clock generators; lowers cost, power and area
- Integrated terminations on LP-HCSL PCIe outputs; eliminate 24 resistors, saving 41mm<sup>2</sup> of board area
- Industrial temperature range operation; supports demanding environmental conditions
- Advanced 3.3V CMOS process; high-performance, low-power
- Supports independent spread spectrum on Sys\_CCB/DDRCLK and PCIe outputs
- Available in 48-pin TSSOP and space-saving 7 x 7 mm 48-pin VFQFPN with 0.5mm pad pitch; reduced board space without the need for fine-pitch assembly techniques

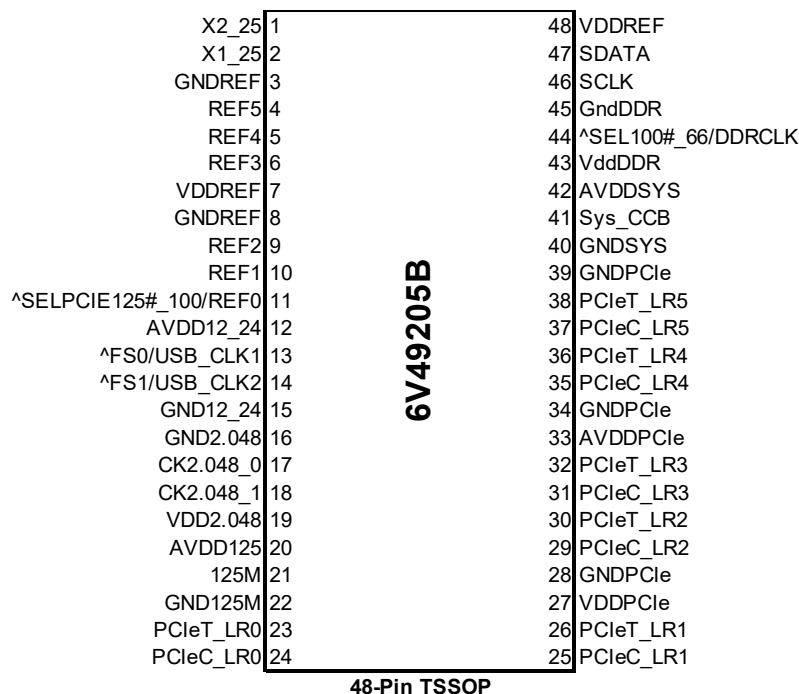
## Block Diagram



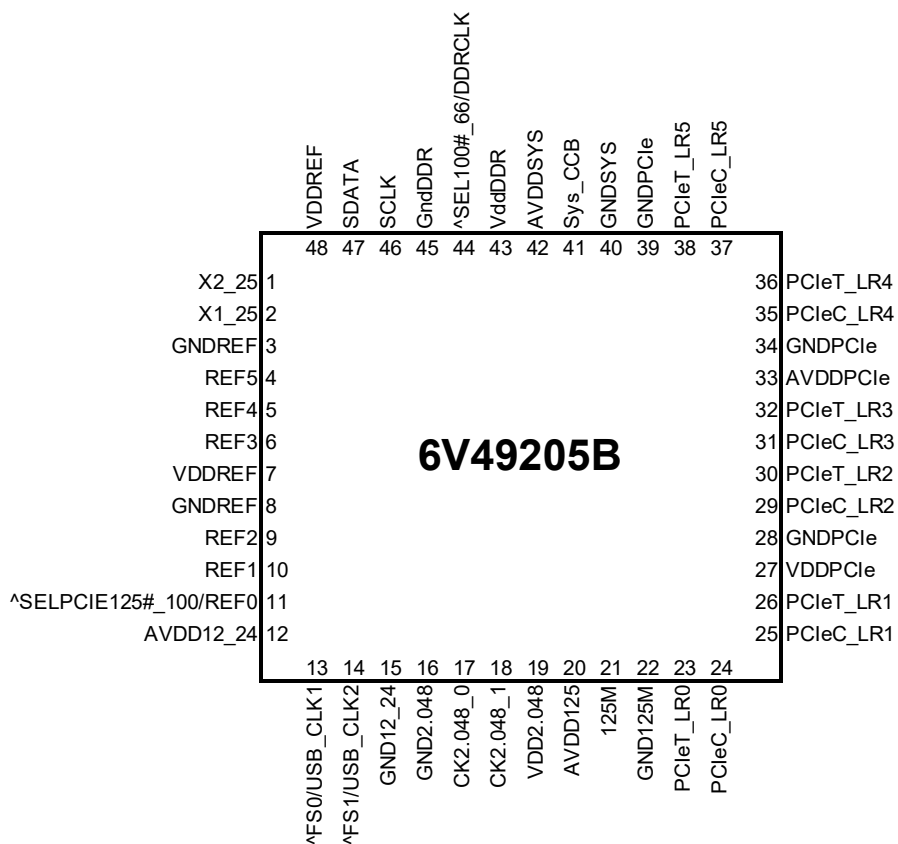
**Note 1:** For DDR Clock: Processor core and I/O supply rails must be ramped with VDD3P3 or earlier. Clock signal will be clamped LOW and output clock will be 100MHz if this is not followed (see diagram below).



## Pin Assignments



^ Indicates Internal 100kohm pull up resistor



^ Indicates Internal 100kohm pull up resistor

## Pin Descriptions

| PIN # | PIN NAME             | PIN TYPE | DESCRIPTION                                                                                                                            |
|-------|----------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------|
| 1     | X2_25                | OUT      | Crystal output, Nominally 25.00MHz.                                                                                                    |
| 2     | X1_25                | IN       | Crystal input, Nominally 25.00MHz.                                                                                                     |
| 3     | GNDREF               | PWR      | Ground pin for the REF outputs.                                                                                                        |
| 4     | REF5                 | OUT      | Copy of crystal input                                                                                                                  |
| 5     | REF4                 | OUT      | Copy of crystal input                                                                                                                  |
| 6     | REF3                 | OUT      | Copy of crystal input                                                                                                                  |
| 7     | VDDREF               | PWR      | Ref, XTAL power supply, nominal 3.3V                                                                                                   |
| 8     | GNDREF               | PWR      | Ground pin for the REF outputs.                                                                                                        |
| 9     | REF2                 | OUT      | Copy of crystal input                                                                                                                  |
| 10    | REF1                 | OUT      | Copy of crystal input                                                                                                                  |
| 11    | ^SELPIC125#_100/REF0 | I/O      | Latched input to select the PCIe output frequency/REF0 output.<br>0 = 125M<br>1 = 100M                                                 |
| 12    | AVDD12_24            | PWR      | Power for 12_24MHz PLL core, and outputs. Nominal 3.3V                                                                                 |
| 13    | ^FS0/USB_CLK1        | I/O      | Frequency select latch for Sys_CCB / 12 or 24MHz USB clock output. 3.3V. This pin has an internal pull up resistor.                    |
| 14    | ^FS1/USB_CLK2        | I/O      | Frequency select latch for Sys_CCB / 12 or 24MHz USB clock output. 3.3V. This pin has an internal pull up resistor.                    |
| 15    | GND12_24             | PWR      | Ground pin for 12_24M outputs.                                                                                                         |
| 16    | GND2.048             | PWR      | Ground pin for 2.048M outputs.                                                                                                         |
| 17    | CK2.048_0            | OUT      | 2.048M output, nominal 3.3V.                                                                                                           |
| 18    | CK2.048_1            | OUT      | 2.048M output, nominal 3.3V.                                                                                                           |
| 19    | VDD2.048             | PWR      | Power supply for 2.048M outputs, nominal 3.3V.                                                                                         |
| 20    | AVDD125              | PWR      | Power for 125MHz PLL core and output, nominal 3.3V                                                                                     |
| 21    | 125M                 | OUT      | 125M output, nominal 3.3V.                                                                                                             |
| 22    | GND125M              | PWR      | Ground pin for 125M outputs.                                                                                                           |
| 23    | PCleT_LR0            | OUT      | True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                       |
| 24    | PCleC_LR0            | OUT      | Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                 |
| 25    | PCleC_LR1            | OUT      | Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                 |
| 26    | PCleT_LR1            | OUT      | True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                       |
| 27    | VDDPCle              | PWR      | Power supply for PCI Express outputs, nominal 3.3V                                                                                     |
| 28    | GNDPCle              | PWR      | Ground pin for the PCIe outputs.                                                                                                       |
| 29    | PCleC_LR2            | OUT      | Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                 |
| 30    | PCleT_LR2            | OUT      | True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                       |
| 31    | PCleC_LR3            | OUT      | Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                 |
| 32    | PCleT_LR3            | OUT      | True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                       |
| 33    | AVDDPCle             | PWR      | Analog Power supply for PCI Express clocks, nominal 3.3V                                                                               |
| 34    | GNDPCle              | PWR      | Ground pin for the PCIe outputs.                                                                                                       |
| 35    | PCleC_LR4            | OUT      | Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                 |
| 36    | PCleT_LR4            | OUT      | True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                       |
| 37    | PCleC_LR5            | OUT      | Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                 |
| 38    | PCleT_LR5            | OUT      | True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor                                       |
| 39    | GNDPCle              | PWR      | Ground pin for the PCIe outputs.                                                                                                       |
| 40    | GNDSYS               | PWR      | Ground pin for the Sys_CCB output                                                                                                      |
| 41    | Sys_CCB              | OUT      | System CCB clock output                                                                                                                |
| 42    | AVDDSYS              | PWR      | Analog Power supply for Sys_CCB clock and outputs, nominal 3.3V                                                                        |
| 43    | VddDDR               | PWR      | Power supply for DDR Clock output, nominal 3.3V                                                                                        |
| 44    | ^SEL100#_66/DDRCLK   | I/O      | Latched input to select the DDR output frequency/DDRCLK output. See note regarding system power sequencing.<br>0 = 100M<br>1 = 66.666M |
| 45    | GndDDR               | PWR      | Ground pin for the DDR outputs.                                                                                                        |
| 46    | SCLK                 | IN       | Clock pin of SMBus circuitry.                                                                                                          |
| 47    | SDATA                | I/O      | Data pin for SMBus circuitry.                                                                                                          |
| 48    | VDDREF               | PWR      | Ref, XTAL power supply, nominal 3.3V                                                                                                   |

**Table 1: PCIEX Spread Table** (selectable via SMBUS)

| SELPCIE125#_100<br>B6b4 | B0b4 | B0b3 | Spread %            |
|-------------------------|------|------|---------------------|
| 0 (125MHz)              | x    | x    | No Spread           |
| 1 (100MHz)              | 0    | 0    | No Spread (default) |
| 1 (100MHz)              | 0    | 1    | Down -0.5%          |
| 1 (100MHz)              | 1    | 0    | Down -0.75%         |
| 1 (100MHz)              | 1    | 1    | No Spread           |

\*Once in spread mode, do not return to non spread without reset

**Table 2: Sys\_CCB and DDR Spread Table** (selectable via SMBUS)

| B0b7 | B0b6 | B0b5 | Spread %            |
|------|------|------|---------------------|
| 0    | 0    | 0    | No Spread (default) |
| 0    | 0    | 1    | Down -0.5%          |
| 0    | 1    | 0    | Down -0.75%         |
| 0    | 1    | 1    | Down -0.25%         |
| 1    | 0    | 0    | Down -1%            |
| 1    | 0    | 1    | Down -1.25%         |
| 1    | 1    | 0    | Down -1.5%          |
| 1    | 1    | 1    | Down -2%            |

**Table 3: Sys\_CCB Frequency Select Table** (Latched and selectable via SMBUS)

| FS1 /<br>B4b3 | FS0 /<br>B4b2 | Sys_CCB (MHz) |
|---------------|---------------|---------------|
| 0             | 0             | 66.66         |
| 0             | 1             | 100           |
| 1             | 0             | 80            |
| 1             | 1             | 83.33         |

**Table 4: PCI Express Amplitude Control**

| B6b7 | B6b6 | PCIe Amplitude |
|------|------|----------------|
| 0    | 0    | 700mV          |
| 0    | 1    | 800mV          |
| 1    | 0    | 900mV          |
| 1    | 1    | 1000mV         |

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 6V49205B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER              | SYMBOL          | CONDITIONS        | MIN       | TYP | MAX       | UNITS | Notes |
|------------------------|-----------------|-------------------|-----------|-----|-----------|-------|-------|
| Maximum Supply Voltage | VDDxxx          | Supply Voltage    |           |     | 4.6       | V     | 1     |
| Maximum Input Voltage  | V <sub>IH</sub> | Referenced to GND |           |     | VDD + 0.5 | V     | 1     |
| Minimum Input Voltage  | V <sub>IL</sub> | Referenced to GND | GND - 0.5 |     |           | V     | 1     |
| Storage Temperature    | T <sub>s</sub>  | -                 | -65       |     | 150       | °C    |       |
| Junction Temperature   | T <sub>j</sub>  | -                 |           |     | 125       | °C    | 1     |
| Input ESD protection   | ESD prot        | Human Body Model  | 2000      |     |           | V     | 1     |

### NOTES on Absolute Max Parameters

<sup>1</sup> Operation under these conditions is neither implied, nor guaranteed.

## Electrical Characteristics - Input/Supply/Common Output DC Parameters

T<sub>AMB</sub> = -40 to +85°C; V<sub>DD</sub> = 3.3 V +/-5%, All outputs driving test loads (unless noted otherwise).

| PARAMETER                                     | SYMBOL               | CONDITIONS                                                   | MIN                   | TYP | MAX                   | UNITS | Notes |
|-----------------------------------------------|----------------------|--------------------------------------------------------------|-----------------------|-----|-----------------------|-------|-------|
| Ambient Operating Temp                        | T <sub>AMB</sub>     | -                                                            | -40                   | 25  | 85                    | °C    |       |
| Supply Voltage                                | VDDxxx               | Supply Voltage                                               | 3.135                 | 3.3 | 3.465                 | V     |       |
| Power supply Ramp Time                        | T <sub>PWRAMP</sub>  | Power supply ramp must be monotonic                          |                       |     | 4                     | ms    |       |
| Latched Input High Voltage                    | V <sub>IH_LI</sub>   | Single-ended Latched Inputs                                  | 2.1                   |     | V <sub>DD</sub> + 0.3 | V     |       |
| Latched Input Low Voltage                     | V <sub>IL_LI</sub>   | Single-ended Latched Inputs                                  | V <sub>SS</sub> - 0.3 |     | 0.8                   | V     |       |
| Input Leakage Current                         | I <sub>IN</sub>      | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND    | -5                    |     | 5                     | uA    | 2     |
| Operating Supply Current                      | I <sub>DDOP3.3</sub> | All outputs loaded and running                               |                       | 119 | 155                   | mA    |       |
| Input Frequency                               | F <sub>i</sub>       |                                                              | 23                    | 25  | 27                    | MHz   | 3     |
| Pin Inductance                                | L <sub>pin</sub>     |                                                              |                       | 5   | 7                     | nH    |       |
| Input Capacitance                             | C <sub>IN</sub>      | Logic Inputs                                                 | 1.5                   | 3   | 5                     | pF    |       |
|                                               | C <sub>OUT</sub>     | Output pin capacitance                                       |                       | 5   | 6                     | pF    |       |
|                                               | C <sub>INX</sub>     | X1 & X2 pins                                                 |                       | 5   | 6                     | pF    |       |
| Clk Stabilization                             | T <sub>STAB</sub>    | From VDD Power-Up or de-assertion of PD to 1st clock         |                       | 3.2 | 5                     | ms    |       |
| T <sub>fall_SE</sub>                          | T <sub>FALL</sub>    | Fall/rise time of all 3.3V control inputs from 20-80%        |                       |     | 10                    | ns    | 1     |
| T <sub>rise_SE</sub>                          | T <sub>RISE</sub>    |                                                              |                       |     | 10                    | ns    | 1     |
| SMBus Voltage                                 | V <sub>DD</sub>      |                                                              | 2.7                   |     | 3.3                   | V     |       |
| Low-level Output Voltage                      | V <sub>OLSMB</sub>   | @ I <sub>PULLUP</sub>                                        |                       |     | 0.4                   | V     |       |
| Current sinking at V <sub>OLSMB</sub> = 0.4 V | I <sub>PULLUP</sub>  | SMB Data Pin                                                 | 4                     |     |                       | mA    |       |
| SCLK/SDATA Clock/Data Rise Time               | T <sub>RI2C</sub>    | (Max V <sub>IL</sub> - 0.15) to (Min V <sub>IH</sub> + 0.15) |                       |     | 1000                  | ns    |       |
| SCLK/SDATA Clock/Data Fall Time               | T <sub>FI2C</sub>    | (Min V <sub>IH</sub> + 0.15) to (Max V <sub>IL</sub> - 0.15) |                       |     | 300                   | ns    |       |
| SMBus Operating Frequency                     | F <sub>SMBUS</sub>   |                                                              |                       |     | 400                   | kHz   |       |

### NOTES on DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

<sup>1</sup> Signal is required to be monotonic in this region.

<sup>2</sup> Input leakage current does not include inputs with pull-up or pull-down resistors

<sup>3</sup> For margining purposes only. Normal operation should have F<sub>in</sub> = 25MHz

## AC Electrical Characteristics - Low Power HCSL-Compatible PCIe Outputs

| PARAMETER                            | SYMBOL                   | CONDITIONS                       | MIN    | TYP  | MAX  | UNITS | NOTES |
|--------------------------------------|--------------------------|----------------------------------|--------|------|------|-------|-------|
| Clock Frequency                      | f                        | Spread off                       | 100.00 |      |      | MHz   | 2,3   |
|                                      |                          |                                  | 125.00 |      |      | MHz   | 2,3   |
| Synthesis error                      | ppm <sub>SSoff</sub>     | PCIe 100MHz or 125MHz            | 0      |      |      | ppm   | 1,2   |
|                                      | ppm <sub>SSon</sub>      | PCIe @ -0.5% spread, 100MHz only | +/-100 |      |      | ppm   | 1,2   |
| Rising/Falling Edge Slew Rate        | t <sub>SLEW</sub>        | Differential Measurement         | 2.2    | 4.1  | 5.7  | V/ns  | 1,3,6 |
| Slew Rate Variation                  | t <sub>SLVAR</sub>       | Single-ended Measurement         |        | 1    | 20   | %     | 1,6   |
| Maximum Output Voltage               | V <sub>HIGH</sub>        | Includes overshoot               |        | 793  | 1150 | mV    | 6,7   |
| Minimum Output Voltage               | V <sub>LOW</sub>         | Includes undershoot              | -300   | -22  |      | mV    | 6,7   |
| Differential Voltage Swing           | V <sub>SWING</sub>       | Differential Measurement         | 300    |      |      | mV    | 1,6   |
| Crossing Point Voltage               | V <sub>XABS</sub>        | Single-ended Measurement         | 300    | 419  | 550  | mV    | 1,4,6 |
| Crossing Point Variation             | V <sub>XABSVAR</sub>     | Single-ended Measurement         |        | 115  | 140  | mV    | 1,4,5 |
| Duty Cycle                           | D <sub>CYC</sub>         | Differential Measurement         | 45     | 50.1 | 55   | %     | 1     |
| PCIe Jitter - Cycle to Cycle         | PCIe <sub>JC2C</sub>     | Differential Measurement         |        | 36   | 125  | ps    | 1     |
| PCIe[5:0] Skew                       | T <sub>SKEW</sub> PCIe50 | Differential Measurement         |        | 1172 | 1500 | ps    | 1,6,8 |
| Spread Spectrum Modulation Frequency | f <sub>SSMOD</sub>       | Triangular Modulation            | 30     | 31.5 | 33   | kHz   |       |

### Notes for PCIe Clocks:

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Clock Frequency specifications are guaranteed assuming that REF is at 25MHz

<sup>3</sup> Slew rate measured through V<sub>swing</sub> voltage range centered about differential zero

<sup>4</sup> V<sub>cross</sub> is defined at the voltage where Clock = Clock#.

<sup>5</sup> Only applies to the differential rising edge (Clock rising, Clock# falling.)

<sup>6</sup> At default SMBus settings.

<sup>7</sup> The Freescale P-series CPU's have internal terminations on their SerDes Reference Clock inputs. The resulting amplitude at these inputs will be 1/2 of the values listed, which are well within the 800mV Freescale specification for these inputs.

<sup>8</sup> This value includes an intentional output-to-output skew of approximately 250ps.

## Electrical Characteristics - Phase Jitter, PCIe Outputs at 100MHz

| PARAMETER     | SYMBOL                   | CONDITIONS                                 | MIN | TYP | MAX  | INDUSTRY SPEC LIMIT | UNITS       | NOTES |
|---------------|--------------------------|--------------------------------------------|-----|-----|------|---------------------|-------------|-------|
| Jitter, Phase | t <sub>jph</sub> PCIe1   | PCIe Gen 1 phase jitter                    |     | 35  | 56   | 86                  | ps          | 1,2,3 |
|               | t <sub>jph</sub> PCIe2Lo | PCIe Gen 2 phase jitter<br>Lo-band content |     | 1.6 | 2.4  | 3                   | ps<br>(RMS) | 1,2,3 |
|               | t <sub>jph</sub> PCIe2Hi | PCIe Gen 2 phase jitter<br>Hi-band content |     | 1.9 | 2.8  | 3.1                 | ps<br>(RMS) | 1,2,3 |
|               | t <sub>jph</sub> PCIe3   | PCIe Gen 3 phase jitter                    |     | 0.5 | 0.83 | 1                   | ps<br>(RMS) | 1,2,3 |

### Notes on Phase Jitter:

<sup>1</sup> See <http://www.pcisig.com> for complete specs. Guaranteed by design and characterization, not tested in production.

<sup>2</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1<sup>-12</sup>

<sup>3</sup> Applies to PCIe outputs @ default amplitude and 100MHz with spread off or at -0.5%.

## Electrical Characteristics - DDR Clock

| PARAMETER                                        | SYMBOL               | CONDITIONS                                                                                | MIN | TYP    | MAX  | UNITS | NOTES |
|--------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------|-----|--------|------|-------|-------|
| DDR Clock Frequency                              | $f_{DDR66.66}$       | SEL100#_66 = 1, $V_T = OVDD/2$ V                                                          |     | 66.666 |      | MHz   | 2,3,6 |
|                                                  | $f_{DDR100}$         | SEL100#_66 = 0, $V_T = OVDD/2$ V                                                          |     | 100.00 |      | MHz   | 2,3,6 |
| Synthesis error                                  | ppm <sub>SSoff</sub> | Spread off                                                                                |     | 0      |      | ppm   | 1,2,5 |
|                                                  | ppm <sub>SSon</sub>  | Spread on                                                                                 |     | +/-150 |      | ppm   | 1,2,5 |
| Output High Voltage                              | $V_{OH}$             | $V_{OH}$ at the selected operating frequency                                              | 2.4 |        |      | V     | 1     |
| Output Low Voltage                               | $V_{OL}$             | $V_{OL}$ at the selected operating frequency                                              |     |        | 0.4  | V     | 1     |
| Slew Rate<br>VDDO = 3.3V                         | $t_{SLEW00}$         | '00' = Hi-Z                                                                               |     | Hi-Z   |      | V/ns  |       |
|                                                  | $t_{SLEW01}$         | '01' Slow Slew Rate (Averaging on)                                                        | 1.1 | 1.6    | 2.3  | V/ns  | 1,3,8 |
|                                                  | $t_{SLEW10}$         | '10' Fast Slew Rate (Averaging on)                                                        | 1.6 | 2.3    | 3.2  | V/ns  | 1,3,8 |
|                                                  | $t_{SLEW11}$         | '11' Fastest Slew Rate (Averaging on)                                                     | 1.8 | 2.7    | 3.7  | V/ns  | 1,3,8 |
| Duty Cycle                                       | $d_{I1}$             | $V_T = OVDD/2$ V                                                                          | 40  | 51.4   | 60   | %     | 1,6   |
| Jitter, Peak period jitter                       | $t_{jpeak}$          | $V_T = OVDD/2$ V                                                                          |     | ±96    | ±150 | ps    | 1,6   |
| Phase Noise                                      | $t_{phasenoise}$     | -56dBc                                                                                    |     | 10     | 500  | kHz   | 1,7   |
| AC Input Swing Limits @ 3.3V<br>OV <sub>DD</sub> | $\Delta V_{AC}$      | This is the difference between $V_{OL}$ and $V_{OH}$ at the selected operating frequency. | 1.9 | 3.4    |      | V     | 1     |
| Spread Spectrum Modulation<br>Frequency          | $f_{SSMOD}$          | Triangular Modulation                                                                     | 30  | 32.3   | 60   | kHz   |       |

## Electrical Characteristics - Sys\_CCB

| PARAMETER                                        | SYMBOL               | CONDITIONS                                                                                | MIN | TYP    | MAX  | UNITS | NOTES |
|--------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------|-----|--------|------|-------|-------|
| Clock Frequency                                  | $f_{Sys\_CCB}$       | FS(1:0) = 00, $V_T = OVDD/2$ V                                                            |     | 66.666 |      | MHz   | 2,3,6 |
|                                                  |                      | FS(1:0) = 01, $V_T = OVDD/2$ V                                                            |     | 100.00 |      | MHz   | 2,3,6 |
|                                                  |                      | FS(1:0) = 10, $V_T = OVDD/2$ V                                                            |     | 80.00  |      | MHz   | 2,3,6 |
|                                                  |                      | FS(1:0) = 11, $V_T = OVDD/2$ V                                                            |     | 83.333 |      | MHz   | 2,3,6 |
| Synthesis error                                  | ppm <sub>SSoff</sub> | Spread off                                                                                |     | 0      |      | ppm   | 1,2,5 |
|                                                  | ppm <sub>SSon</sub>  | Spread on                                                                                 |     | +/-150 |      | ppm   | 1,2,5 |
| Output High Voltage                              | $V_{OH}$             | $V_{OH}$ at the selected operating frequency                                              | 2.4 |        |      | V     | 1     |
| Output Low Voltage                               | $V_{OL}$             | $V_{OL}$ at the selected operating frequency                                              |     |        | 0.4  | V     | 1     |
| Slew Rate<br>VDDO = 3.3V                         | $t_{SLEW00}$         | '00' = Hi-Z                                                                               |     | Hi-Z   |      | V/ns  |       |
|                                                  | $t_{SLEW01}$         | '01' Slow Slew Rate (Averaging on)                                                        | 0.8 | 1.4    | 2.1  | V/ns  | 1,3,8 |
|                                                  | $t_{SLEW10}$         | '10' Fast Slew Rate (Averaging on)                                                        | 0.9 | 1.6    | 2.5  | V/ns  | 1,3,8 |
|                                                  | $t_{SLEW11}$         | '11' Fastest Slew Rate (Averaging on)                                                     | 1.1 | 1.9    | 3.1  | V/ns  | 1,3,8 |
| Duty Cycle                                       | $d_{I1}$             | $V_T = OVDD/2$ V                                                                          | 40  | 51.4   | 60   | %     | 1,6   |
| Jitter, Peak period jitter                       | $t_{jpeak}$          | $V_T = OVDD/2$ V, SSC < 0.75%                                                             |     | ±116   | ±150 | ps    | 1     |
| Phase Noise                                      | $t_{phasenoise}$     | -56dBc                                                                                    |     | 10     | 500  | kHz   | 1,7   |
| AC Input Swing Limits @ 3.3V<br>OV <sub>DD</sub> | $\Delta V_{AC}$      | This is the difference between $V_{OL}$ and $V_{OH}$ at the selected operating frequency. | 1.9 |        |      | V     | 1     |
| Spread Spectrum Modulation<br>Frequency          | $f_{SSMOD}$          | Triangular Modulation                                                                     | 0   | 31.5   | 60   | kHz   |       |

## Electrical Characteristics - 125M

| PARAMETER                     | SYMBOL           | CONDITIONS                                   | MIN | TYP    | MAX  | UNITS | NOTES |
|-------------------------------|------------------|----------------------------------------------|-----|--------|------|-------|-------|
| Clock frequency               | $f_{125M}$       | $V_T = OVDD/2$ V                             |     | 125.00 |      | ns    | 2,3,6 |
| Synthesis error               | ppm              |                                              |     | 0      |      | ppm   | 1,2,5 |
| Output High Voltage           | $V_{OH}$         | $V_{OH}$ at the selected operating frequency | 2.2 |        |      | V     | 1     |
| Output Low Voltage            | $V_{OL}$         | $V_{OL}$ at the selected operating frequency |     |        | 0.5  | V     | 1     |
| Rise/Fall time<br>VDDO = 3.3V | $t_{RF125M3.3V}$ | Measured between 0.6V and 2.7V               |     | 0.7    | 1    | ns    | 1,3   |
| Duty Cycle                    | $d_{I1}$         | $V_T = OVDD/2$ V                             | 47  | 52     | 53   | %     | 1     |
| Jitter, Peak period jitter    | $t_{jpeak}$      | $V_T = OVDD/2$ V                             |     |        | ±150 | ps    | 1     |

## Electrical Characteristics - REF(5:0)

| PARAMETER                  | SYMBOL       | CONDITIONS                                                                         | MIN | TYP   | MAX  | UNITS  | NOTES |
|----------------------------|--------------|------------------------------------------------------------------------------------|-----|-------|------|--------|-------|
| Clock Frequency            | f            | $V_T = OVDD/2\text{ V}$                                                            |     | 25.00 |      | MHz    | 2,3   |
| Crystal Frequency Error    | ppm          | Including all aging and tuning effects                                             | -50 |       | 50   | ppm    | 1,2   |
| Output High Voltage        | $V_{OH}$     | $V_{OH}$ at the selected operating frequency                                       | 2.2 |       |      | V      | 1     |
| Output Low Voltage         | $V_{OL}$     | $V_{OL}$ at the selected operating frequency                                       |     |       | 0.4  | V      | 1     |
| Slew Rate                  | $t_{SLEW}$   | '00' = Hi-Z                                                                        | 1.0 | 1.7   | 2.7  | V/ns   | 1,3,4 |
| Duty Cycle                 | $d_{l1}$     | $V_T = OVDD/2\text{ V}$                                                            | 40  | 51    | 60   | %      | 1     |
| Pin to Pin Skew            | $t_{skew}$   | $V_T = 1.5\text{ V}$ , odd/even outputs have an intentional 180degree phase shift. |     | N/A   |      | ps     | 1     |
| Jitter, Peak period jitter | $t_{jpeak}$  | $V_T = OVDD/2\text{ V}$                                                            |     | ±78   | ±200 | ps     | 1     |
| Jitter, Phase              | $t_{jphase}$ | (12kHz-5MHz), $V_T = 1.5\text{ V}$                                                 |     | 1.7   | 3    | ps rms | 1     |

## Electrical Characteristics - USB\_CLK(2:1)

| PARAMETER                             | SYMBOL          | CONDITIONS                                   | MIN | TYP   | MAX | UNITS | NOTES |
|---------------------------------------|-----------------|----------------------------------------------|-----|-------|-----|-------|-------|
| Clock Frequency                       | $f_{USB\_CLK}$  | $V_T = OVDD/2\text{ V}$                      |     | 12.00 |     | MHz   | 2,3   |
|                                       |                 |                                              |     | 24.00 |     | MHz   | 2,3   |
| Synthesis error                       | ppm             |                                              |     | 0     |     | ppm   | 1,2,5 |
| Output High Voltage                   | $V_{OH}$        | $V_{OH}$ at the selected operating frequency | 2.2 |       |     | V     | 1     |
| Output Low Voltage                    | $V_{OL}$        | $V_{OL}$ at the selected operating frequency |     |       | 0.4 | V     | 1     |
| Slew Rate<br>$V_{DDO} = 3.3\text{ V}$ | $t_{SLEW00}$    | '00' = Hi-Z                                  |     | Hi-Z  |     | V/ns  |       |
|                                       | $t_{SLEW01}$    | '01' Slow Slew Rate (Averaging on)           | 1.0 | 1.4   | 1.8 | V/ns  | 1,3,4 |
|                                       | $t_{SLEW10}$    | '10' Fast Slew Rate (Averaging on)           | 1.5 | 2.0   | 2.7 | V/ns  | 1,3,4 |
|                                       | $t_{SLEW11}$    | '11' Fastest Slew Rate (Averaging on)        | 1.8 | 2.3   | 3.1 | V/ns  | 1,3,4 |
| Duty Cycle                            | $d_{l1}$        | $V_T = OVDD/2\text{ V}$                      | 45  | 50.3  | 55  | %     | 1     |
| Jitter, RMS                           | $t_{jRMS}$      | 12kHz to Nyquist                             |     | 23    | 120 | ps    | 1     |
| Jitter, Cycle to cycle                | $t_{jcy c-cyc}$ | $V_T = OVDD/2\text{ V}$                      |     | 142   | 350 | ps    | 1     |

## Electrical Characteristics - 2.048M(1:0)

| PARAMETER                             | SYMBOL         | CONDITIONS                                   | MIN | TYP   | MAX  | UNITS | NOTES |
|---------------------------------------|----------------|----------------------------------------------|-----|-------|------|-------|-------|
| Clock Frequency                       | $f_{USB\_CLK}$ | $V_T = OVDD/2\text{ V}$                      |     | 2.048 |      | MHz   | 2,3,6 |
| Synthesis error                       | ppm            |                                              |     | 0     |      | ppm   | 1,2,5 |
| Output High Voltage                   | $V_{OH}$       | $V_{OH}$ at the selected operating frequency | 2.2 |       |      | V     | 1     |
| Output Low Voltage                    | $V_{OL}$       | $V_{OL}$ at the selected operating frequency |     |       | 0.4  | V     | 1     |
| Slew Rate<br>$V_{DDO} = 3.3\text{ V}$ | $t_{SLEW00}$   | '00' = Hi-Z                                  |     | Hi-Z  |      | V/ns  |       |
|                                       | $t_{SLEW01}$   | '01' Slow Slew Rate (Averaging on)           | 1.1 | 1.7   | 2.5  | V/ns  | 1,3,4 |
|                                       | $t_{SLEW10}$   | '10' Fast Slew Rate (Averaging on)           | 1.6 | 2.3   | 3.2  | V/ns  | 1,3,4 |
|                                       | $t_{SLEW11}$   | '11' Fastest Slew Rate (Averaging on)        | 1.8 | 2.6   | 3.6  | V/ns  | 1,3,4 |
| Duty Cycle                            | $d_{l1}$       | $V_T = OVDD/2\text{ V}$                      | 45  | 46.7  | 55   | %     | 1     |
| Pin to Pin Skew                       | $t_{skew}$     | $V_T = OVDD/2\text{ V}$                      |     | 108   | 250  | ps    | 1     |
| Jitter, RMS                           | $t_{jRMS}$     | 12kHz to Nyquist                             |     | 47    | 70   | ps    | 1     |
| Jitter, Peak period jitter            | $t_{jpeak}$    | $V_T = OVDD/2\text{ V}$                      |     | ±170  | ±250 | ps    | 1     |

### Notes for single-ended clocks:

- <sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.
- <sup>2</sup> Clock Frequency specifications are guaranteed assuming that REF is at 25MHz
- <sup>3</sup> At default SMBus settings
- <sup>4</sup> Measured between 20% and 80% of OVDD
- <sup>5</sup> This is the frequency error with respect to the crystal frequency.
- <sup>6</sup> Measured at the rising and/or falling edge at OVDD/2 V.
- <sup>7</sup> Phase noise is calculated as the FFT of the TIE jitter.
- <sup>8</sup> Slew rate is measured from  $\pm 0.3\Delta V_{AC}$  at the center of peak to peak voltage at the clock input.

# General SMBus Serial Interface Information for 6V49205B

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N+X-1**
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation     |           |                          |
|---------------------------------|-----------|--------------------------|
| Controller (Host)               |           | Renesas (Slave/Receiver) |
| T                               | starT bit |                          |
| Slave Address D2 <sub>(H)</sub> |           |                          |
| WR                              | WRite     |                          |
|                                 |           | ACK                      |
| Beginning Byte = N              |           |                          |
|                                 |           | ACK                      |
| Data Byte Count = X             |           |                          |
|                                 |           | ACK                      |
| Beginning Byte N                | X Byte    |                          |
|                                 |           | ACK                      |
| O                               |           |                          |
| O                               |           | O                        |
| O                               |           | O                        |
|                                 |           | O                        |
| Byte N + X - 1                  |           |                          |
|                                 |           | ACK                      |
| P                               | stoP bit  |                          |

**Note: I<sup>2</sup>C compatible.** Native mode is SMBus Block mode protocol. To use I<sup>2</sup>C Byte mode set the 2<sup>7</sup> bit in the command Byte. No Byte count is used.

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends **Byte N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation      |                 |                          |
|---------------------------------|-----------------|--------------------------|
| Controller (Host)               |                 | Renesas (Slave/Receiver) |
| T                               | starT bit       |                          |
| Slave Address D2 <sub>(H)</sub> |                 |                          |
| WR                              | WRite           |                          |
|                                 |                 | ACK                      |
| Beginning Byte = N              |                 |                          |
|                                 |                 | ACK                      |
| RT                              | Repeat starT    |                          |
| Slave Address D3 <sub>(H)</sub> |                 |                          |
| RD                              | ReaD            |                          |
|                                 |                 | ACK                      |
|                                 |                 | Data Byte Count=X        |
| ACK                             |                 |                          |
|                                 |                 | Beginning Byte N         |
| ACK                             |                 |                          |
|                                 |                 | O                        |
| O                               |                 | O                        |
| O                               |                 | O                        |
| O                               |                 |                          |
|                                 |                 | Byte N + X - 1           |
| N                               | Not acknowledge |                          |
| P                               | stoP bit        |                          |

**Byte 0 Frequency and Spread Select Register**

| Bit | Name     | Description                               | Type | 0                                            | 1              | Default |
|-----|----------|-------------------------------------------|------|----------------------------------------------|----------------|---------|
| 7   | SS4      | Sys_CCB and DDRCLK Spread Selection Table | RW   | See Table 2: Sys_CCB and DDRCLK Spread Table |                | 0       |
| 6   | SS3      |                                           | RW   |                                              |                | 0       |
| 5   | SS2      |                                           | RW   |                                              |                | 0       |
| 4   | SS1      | PCIE Spread Selection Table               | RW   | See Table 1: PCIE Spread Table               |                | 0       |
| 3   | SS0      |                                           | RW   |                                              |                | 0       |
| 2   | REF_5_EN | Output enable for REF_5                   | RW   | Output Disabled                              | Output Enabled | 1       |
| 1   | REF_4_EN | Output enable for REF_4                   | RW   | Output Disabled                              | Output Enabled | 1       |
| 0   | REF_3_EN | Output enable for REF_5                   | RW   | Output Disabled                              | Output Enabled | 1       |

**Byte 1 Output Enable Register**

| Bit | Name         | Description                 | Type | 0               | 1              | Default |
|-----|--------------|-----------------------------|------|-----------------|----------------|---------|
| 7   | REF_2_EN     | Output enable for REF_2     | RW   | Output Disabled | Output Enabled | 1       |
| 6   | REF_1_EN     | Output enable for REF_1     | RW   | Output Disabled | Output Enabled | 1       |
| 5   | REF_0_EN     | Output enable for REF_0     | RW   | Output Disabled | Output Enabled | 1       |
| 4   | USB_CLK1_EN  | Output enable for USB_CLK1  | RW   | Output Disabled | Output Enabled | 1       |
| 3   | USB_CLK2_EN  | Output enable for USB_CLK2  | RW   | Output Disabled | Output Enabled | 1       |
| 2   | CK2.048_0_EN | Output enable for CK2.048_0 | RW   | Output Disabled | Output Enabled | 1       |
| 1   | CK2.048_1_EN | Output enable for CK2.048_1 | RW   | Output Disabled | Output Enabled | 1       |
| 0   | DDRCLK_EN    | Output enable for DDRCLK    | RW   | Output Disabled | Output Enabled | 1       |

**Byte 2 Output Enable Register**

| Bit | Name       | Description               | Type | 0               | 1              | Default |
|-----|------------|---------------------------|------|-----------------|----------------|---------|
| 7   | Sys_CCB_EN | Output enable for Sys_CCB | RW   | Output Disabled | Output Enabled | 1       |
| 6   | PCle5_EN   | Output enable for PCle5   | RW   | Output Disabled | Output Enabled | 1       |
| 5   | PCle4_EN   | Output enable for PCle4   | RW   | Output Disabled | Output Enabled | 1       |
| 4   | PCle3_EN   | Output enable for PCle3   | RW   | Output Disabled | Output Enabled | 1       |
| 3   | PCle2_EN   | Output enable for PCle2   | RW   | Output Disabled | Output Enabled | 1       |
| 2   | PCle1_EN   | Output enable for PCle1   | RW   | Output Disabled | Output Enabled | 1       |
| 1   | PCle0_EN   | Output enable for PCle0   | RW   | Output Disabled | Output Enabled | 1       |
| 0   | 125M_EN    | Output enable for 125M    | RW   | Output Disabled | Output Enabled | 1       |

**Byte 3 Slew Rate Control Register**

| Bit | Name          | Description                               | Type | 0                             | 1 | Default |
|-----|---------------|-------------------------------------------|------|-------------------------------|---|---------|
| 7   | USB1_SLEW1    | USB_CLK1 Slew Rate Control                | RW   | See USB Electrical Tables     |   | 0       |
| 6   | USB1_SLEW0    |                                           | RW   |                               |   | 1       |
| 5   | USB2_SLEW1    | USB_CLK2 Slew Rate Control                | RW   | See USB Electrical Tables     |   | 0       |
| 4   | USB2_SLEW0    |                                           | RW   |                               |   | 1       |
| 3   | CK2.048_SLEW1 | CK2.048_0 and CK2.048_1 Slew Rate Control | RW   | See CK2.048 Electrical Tables |   | 1       |
| 2   | CK2.048_SLEW0 |                                           | RW   |                               |   | 1       |
| 1   | Sys_CCB_SLEW1 | Sys_CCB Slew Rate Control                 | RW   | See Sys_CCB Electrical Tables |   | 0       |
| 0   | Sys_CCB_SLEW0 |                                           | RW   |                               |   | 1       |

**Byte 4 Slew Rate Control Register**

| Bit | Name      | Description                     | Type | 0                                        | 1     | Default |
|-----|-----------|---------------------------------|------|------------------------------------------|-------|---------|
| 7   | DDR_Slew1 | DDRCLK Slew Rate Control        | RW   | See DDR Electrical Tables                |       | 0       |
| 6   | DDR_Slew0 |                                 | RW   |                                          |       | 1       |
| 5   | Reserved  |                                 |      |                                          |       | 0       |
| 4   | Reserved  |                                 |      |                                          |       | 1       |
| 3   | FS1       | Sys_CCB Frequency Select Latch  | RW   | See Table 3: Sys_CCB Frequency Selection |       | Latch   |
| 2   | FS0       |                                 | RW   |                                          |       | Latch   |
| 1   | USB1_fSel | USB_CLK1 Clock Frequency Select | RW   | 12MHz                                    | 24MHz | 0       |
| 0   | USB2_fSel | USB_CLK2 Clock Frequency Select | RW   | 12MHz                                    | 24MHz | 1       |

Byte 5 is Reserved

### Byte 6 PCI Express Amplitude Control Register

| Bit | Name            | Description                   | Type | 0                                           | 1      | Default |
|-----|-----------------|-------------------------------|------|---------------------------------------------|--------|---------|
| 7   | PCIE_AMP1       | PCI Express Amplitude Control | RW   | See Table 4: PCIe Amplitude Selection Table |        | 0       |
| 6   | PCIE_AMP0       |                               | RW   |                                             |        | 1       |
| 5   | SEL100#_66      | DDRCLK latch select           | R    | 100MHz                                      | 66MHz  | latch   |
| 4   | SELPCIE125#_100 | PCI Express latch select      | R    | 125MHz                                      | 100MHz | latch   |
| 3   | Reserved        | Reserved                      | RW   | -                                           | -      | 0       |
| 2   | Reserved        | Reserved                      | RW   | -                                           | -      | 1       |
| 1   | Reserved        | Reserved                      | RW   | -                                           | -      | 0       |
| 0   | Reserved        | Reserved                      | RW   | -                                           | -      | 1       |

### Byte 7 Revision and Vendor ID Register

| Bit | Name      | Description | Type | 0 | 1 | Default |
|-----|-----------|-------------|------|---|---|---------|
| 7   | REV ID    | Revision ID | R    | - | - | 0       |
| 6   | REV ID    |             | R    | - | - | 0       |
| 5   | REV ID    |             | R    | - | - | 0       |
| 4   | REV ID    |             | R    | - | - | 1       |
| 3   | Vendor ID | Vendor ID   | R    | - | - | 0       |
| 2   | Vendor ID |             | R    | - | - | 0       |
| 1   | Vendor ID |             | R    | - | - | 0       |
| 0   | Vendor ID |             | R    | - | - | 1       |

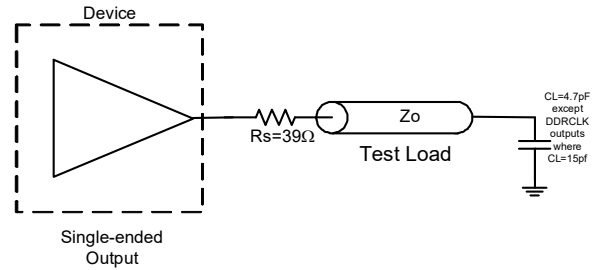
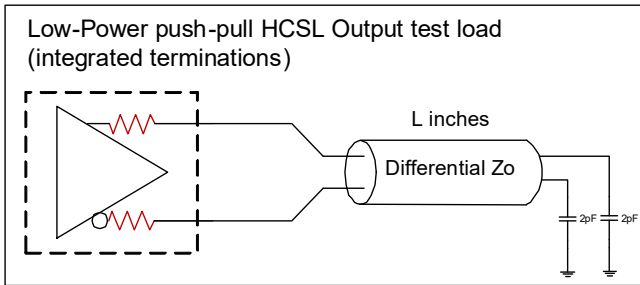
### Byte 8 Byte Count Register

| Bit | Name | Description                   | Type | 0                                                                         | 1 | Default |
|-----|------|-------------------------------|------|---------------------------------------------------------------------------|---|---------|
| 7   | BC7  | Byte Count Programming b(7:0) | RW   | Writing to this register will configure how many bytes will be read back. |   | 0       |
| 6   | BC6  |                               | RW   |                                                                           |   | 0       |
| 5   | BC5  |                               | RW   |                                                                           |   | 0       |
| 4   | BC4  |                               | RW   |                                                                           |   | 0       |
| 3   | BC3  |                               | RW   |                                                                           |   | 0       |
| 2   | BC2  |                               | RW   |                                                                           |   | 1       |
| 1   | BC1  |                               | RW   |                                                                           |   | 0       |
| 0   | BC0  |                               | RW   |                                                                           |   | 1       |

## Recommended Crystal Characteristics

| PARAMETER                                                        | VALUE       | UNITS   |
|------------------------------------------------------------------|-------------|---------|
| Frequency                                                        | 25          | MHz     |
| Resonance Mode                                                   | Fundamental | -       |
| Frequency Tolerance @ 25°C                                       | ±20         | PPM Max |
| Frequency Stability, ref @ 25°C Over Operating Temperature Range | ±20         | PPM Max |
| Temperature Range (commercial)                                   | 0~70        | °C      |
| Temperature Range (industrial)                                   | -40~85      | °C      |
| Equivalent Series Resistance (ESR)                               | 50          | Ω Max   |
| Shunt Capacitance (C <sub>O</sub> )                              | 7           | pF Max  |
| Load Capacitance (C <sub>L</sub> )                               | 8           | pF Max  |
| Drive Level                                                      | 0.1         | mW Max  |
| Aging per year                                                   | ±5          | PPM Max |

## Test Loads



Differential Test Load,  $Z_o = 100\Omega$ ,  $L = 5$  inches

## Thermal Characteristics (48-TSSOP) PAG48

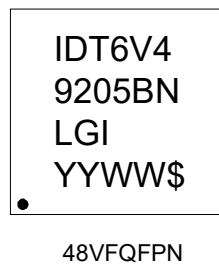
| PARAMETER          | SYMBOL         | CONDITIONS                      | PKG   | TYP VALUE | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|-----------|-------|-------|
| Thermal Resistance | $\theta_{JC}$  | Junction to Case                | PAG48 | 28        | °C/W  | 1     |
|                    | $\theta_{Jb}$  | Junction to Base                |       | 42        | °C/W  | 1     |
|                    | $\theta_{JA0}$ | Junction to Air, still air      |       | 62        | °C/W  | 1     |
|                    | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow |       | 54        | °C/W  | 1     |
|                    | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow |       | 51        | °C/W  | 1     |

## Thermal Characteristics (48-VFQFPN) NLG48

| PARAMETER          | SYMBOL         | CONDITIONS                      | PKG   | TYP VALUE | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|-----------|-------|-------|
| Thermal Resistance | $\theta_{JC}$  | Junction to Case                | NLG48 | 25        | °C/W  | 1     |
|                    | $\theta_{Jb}$  | Junction to Base                |       | 3.1       | °C/W  | 1     |
|                    | $\theta_{JA0}$ | Junction to Air, still air      |       | 32        | °C/W  | 1     |
|                    | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow |       | 25        | °C/W  | 1     |
|                    | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow |       | 22        | °C/W  | 1     |

<sup>1</sup>ePad soldered to board

## Marking Diagrams



Notes:

- '\$' is the mark code.
- YYWW is the last two digits of the year, and the week number that the part was assembled.
- "G" after the two-letter package code denotes Pb free package.
- "I" denotes industrial temperature range.
- Bottom marking for TSSOP: country of origin if not USA.

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Ordering Information

| Part / Order Number | Shipping Packaging | Marking     | Package       | Temperature  |
|---------------------|--------------------|-------------|---------------|--------------|
| 6V49205BPAGI        | Tubes              | see page 12 | 48-pin TSSOP  | -40 to +85°C |
| 6V49205BPAGI8       | Tape and Reel      |             |               | -40 to +85°C |
| 6V49205BNLGI        | Tray               | see page 12 | 48-pin VFQFPN | -40 to +85°C |
| 6V49205BNLGI8       | Tape and Reel      |             |               | -40 to +85°C |

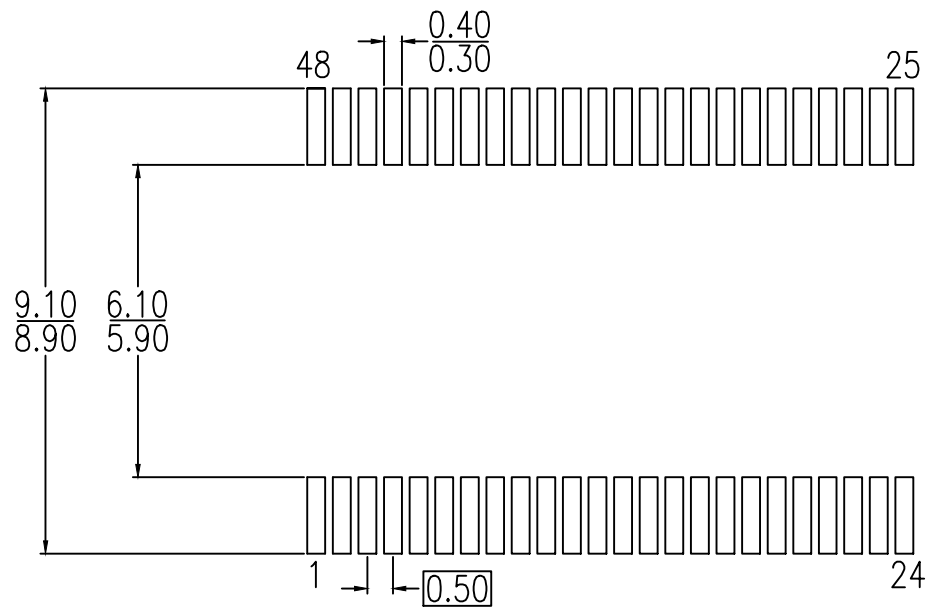
“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

## Revision History

| Revision Date      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| September 29, 2021 | 1. Removed notes column from Crystal Characteristics table.<br>2. Update Package Outline Drawings section.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| October 21, 2020   | 1. Corrected Table 3 FS1 and FS0 values for the Sys_CCB frequency selection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| May 5, 2017        | 1. Updated bit values in the “Sys_CCB Frequency Select” table.<br>2. Updated 48-TSSOP and 48-VFQFPN package outline drawings.<br>3. Updated legal disclaimer.                                                                                                                                                                                                                                                                                                                                                                  |
| November 22, 2016  | 1. Undo Revision Q<br>2. PCIe outputs have integrated terminations for 100ohm differential Zo.<br>3. Update Test Loads<br>4. Update Features/Benefits                                                                                                                                                                                                                                                                                                                                                                          |
| May 11, 2016       | 1. Correct PCIeT_LRn and PCIeC_LRn to be PCIeT_Ln and PCIeC_Ln to indicate that the Rs for the PCIe outputs is outside the part and to correct the pin description accordingly. The test loads for the device are correct.<br>2. Update block diagram PCIe pin names to be consistent.                                                                                                                                                                                                                                         |
| August 10, 2015    | 1. Updated SMBus operating frequency from 100KHz minimum to 400KHz maximum.                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| June 2, 2014       | 1. Corrected pin description for pin 44.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| December 9, 2013   | 1. Extensive overhaul of Electrical tables to more closely align with Freescale published specifications.<br>2. Updated electrical tables with characterization data.<br>3. Clarified SMBus registers for Slew Rate Controls.<br>4. Moved electrical tables in front of SMBus for consistency with other data sheets.<br>5. Updated Thermal Data and added test loads for clarity.<br>6. Updated front page text.<br>7. Minor updates to pin names (mainly power and ground) for consistency and clarity.<br>8. Move to Final. |



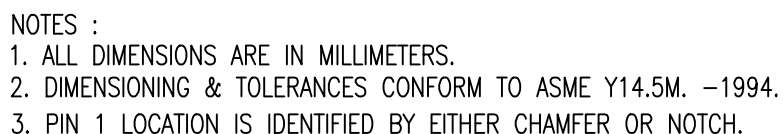
| DATE<br>CREATED                              | REVISIONS |                          |          |
|----------------------------------------------|-----------|--------------------------|----------|
|                                              | REV       | DESCRIPTION              | APPROVED |
| 7/16/18                                      | 00        | Revised from PSC-4039_06 | R.C      |
| NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE |           |                          |          |



RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:  
 1. ALL DIMENSIONS ARE IN MILLIMETERS

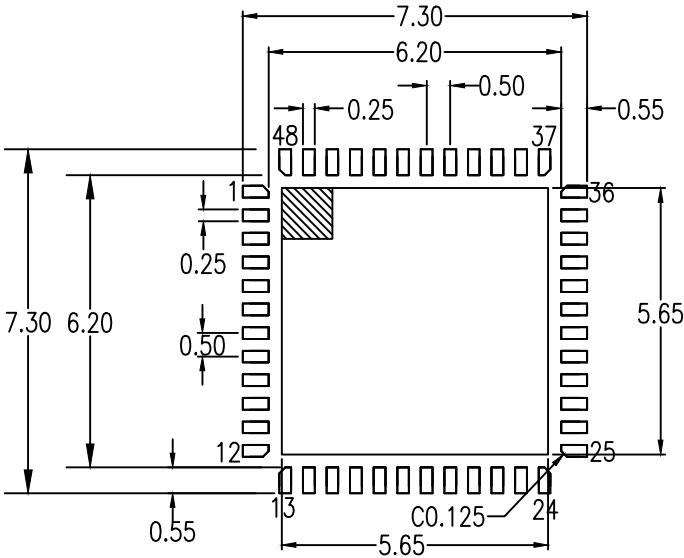
|                                |         |                                                                                                                                                                                                                                                            |
|--------------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TOLERANCES<br>UNLESS SPECIFIED |         |  <div>           6024 Silver Creek Valley Rd<br/>           San Jose, CA 95138<br/>           PHONE: (408) 284-8200<br/>           FAX: (408) 284-3572         </div> |
|                                |         |                                                                                                                                                                                                                                                            |
| DECIMAL                        | ANGULAR | <div>           TITLE           PAC48 Package Outline Drawing<br/>           6.10 mm Body, 0.50mm Pitch<br/>           TSSOP         </div>                                                                                                                |
| XX±                            | ±       |                                                                                                                                                                                                                                                            |
| XXX±                           |         | SIZE                                                                                                                                                                                                                                                       |
| XXXX±                          |         | C                                                                                                                                                                                                                                                          |
|                                |         | DRAWING No.                                                                                                                                                                                                                                                |
|                                |         | PSC-4765                                                                                                                                                                                                                                                   |
|                                |         | REV                                                                                                                                                                                                                                                        |
|                                |         | 00                                                                                                                                                                                                                                                         |
|                                |         | DO NOT SCALE DRAWING                                                                                                                                                                                                                                       |
|                                |         | SHEET 2 OF 2                                                                                                                                                                                                                                               |



48-VFQFPN, Package Outline Drawing

7.0 x 7.0 x 0.85 mm Body, 0.5mm Pitch, Epad 5.65 x 5.65 mm

NLG48P1, PSC-4203-01, Rev 02, Page 2



RECOMMENDED LAND PATTERN

- NOTES:
- 1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
  - 2. TOP DOWN VIEW. AS VIEWED ON PCB.
  - 3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History |         |                                                          |
|--------------------------|---------|----------------------------------------------------------|
| Date Created             | Rev No. | Description                                              |
| May 29, 2018             | Rev 02  | Add Corner Lead Chamfer                                  |
| Mar 7, 2018              | Rev 01  | New Format, Change Pin1 Identifier, Change QFN to VFQFPN |
| Nov 20, 2015             | Rev 00  | Initial Release                                          |

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(Rev.1.0 Mar 2020)

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