Low Quiescent Current 410 kHz Automotive Synchronous Buck Controller

NCV881930

The NCV881930 is a 410 kHz fixed−frequency low quiescent current buck controller with spread spectrum that operates up to 38 V (typical). It may be synchronized to a clock or to separate NCV881930. Peak current mode control is employed for fast transient response and tight regulation over wide input voltage and output load ranges. Feedback compensation is internal to the device, permitting design simplification. The NCV881930 is capable of converting from an automotive input voltage range of 3.5 V (4.5 V during startup) to 18 V at a constant base switching frequency. Under load dump conditions up to 45 V the regulator shuts down. A high voltage bias regulator with automatic switchover to an external 5 V bias supply is used for improved efficiency. Several protection features such as UVLO, current limit, short circuit protection, and thermal shutdown are provided. High switching frequency produces low output voltage ripple even when using small inductor values and an all−ceramic output filter capacitor, forming a space−efficient switching solution.

(2 MHz version offered with NCV891930)

Features

- 30 μA Operating Current at No Load
- 50 mV Current Limit Sensing
- Capable of 45 V Load Dump
- Board Selectable Fixed Output Voltages with Lockout
- 410 kHz Operating Frequency
- Adaptive Non−Overlap Circuitry
- Integrated Spread Spectrum
- Logic level Enable Input Can be Tied Directly to Battery
- Short Circuit Protection Pulse Skip
- Battery Monitoring for UVLO and Overvoltage Protection
- Thermal Shutdown (TSD)
- Adjustable Soft−Start
- SYNCI, SYNCO, Enable, RSTB, ROSC
- QFN Package with Wettable Flanks (pin edge plating)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Typical Applications

- Radio and Infotainment
- Instrumentations & Clusters
- ADAS (safety applications)
- Telematics

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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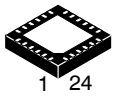
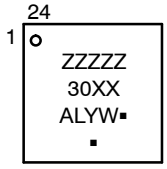


QFNW24 4x4, 0.5P
CASE 484AE

Note: With wettable flanks − meets JEDEC MO220

MARKING DIAGRAM

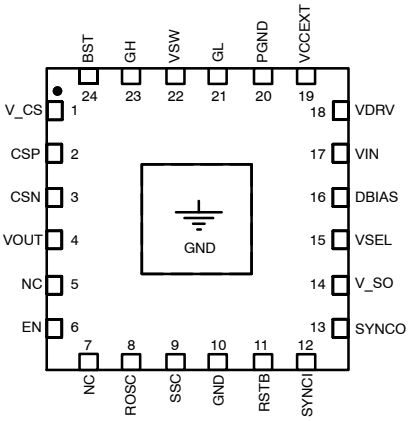


ZZZZZ	= V8819, 8819A
XX	= 00
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

(Top View)



ORDERING INFORMATION

See detailed ordering and shipping information on page 27 of this data sheet.

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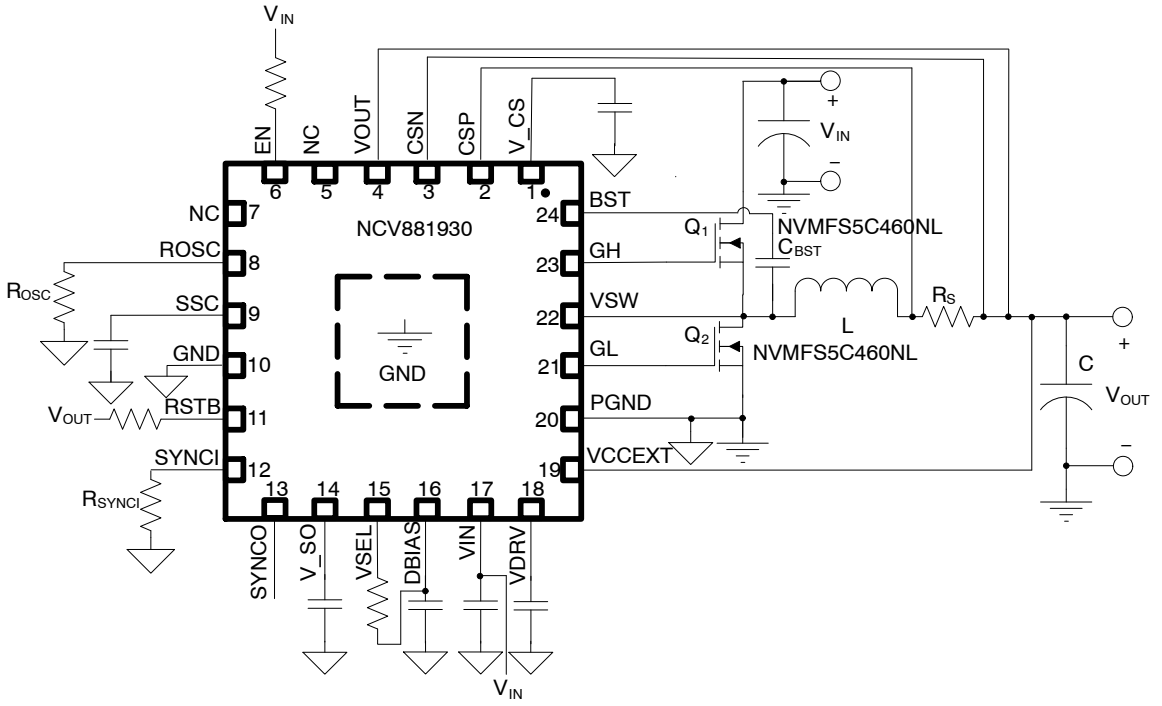

Figure 1. 5 V Application Schematic Example

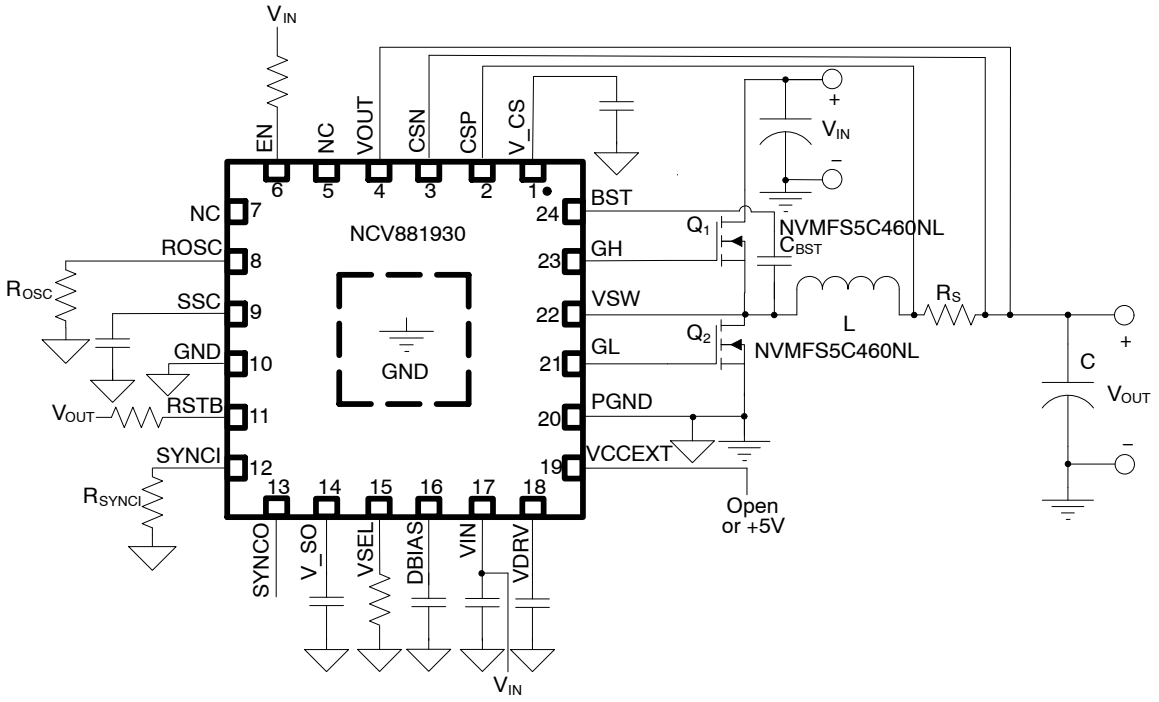

Figure 2. 3.3 V Application Schematic Example

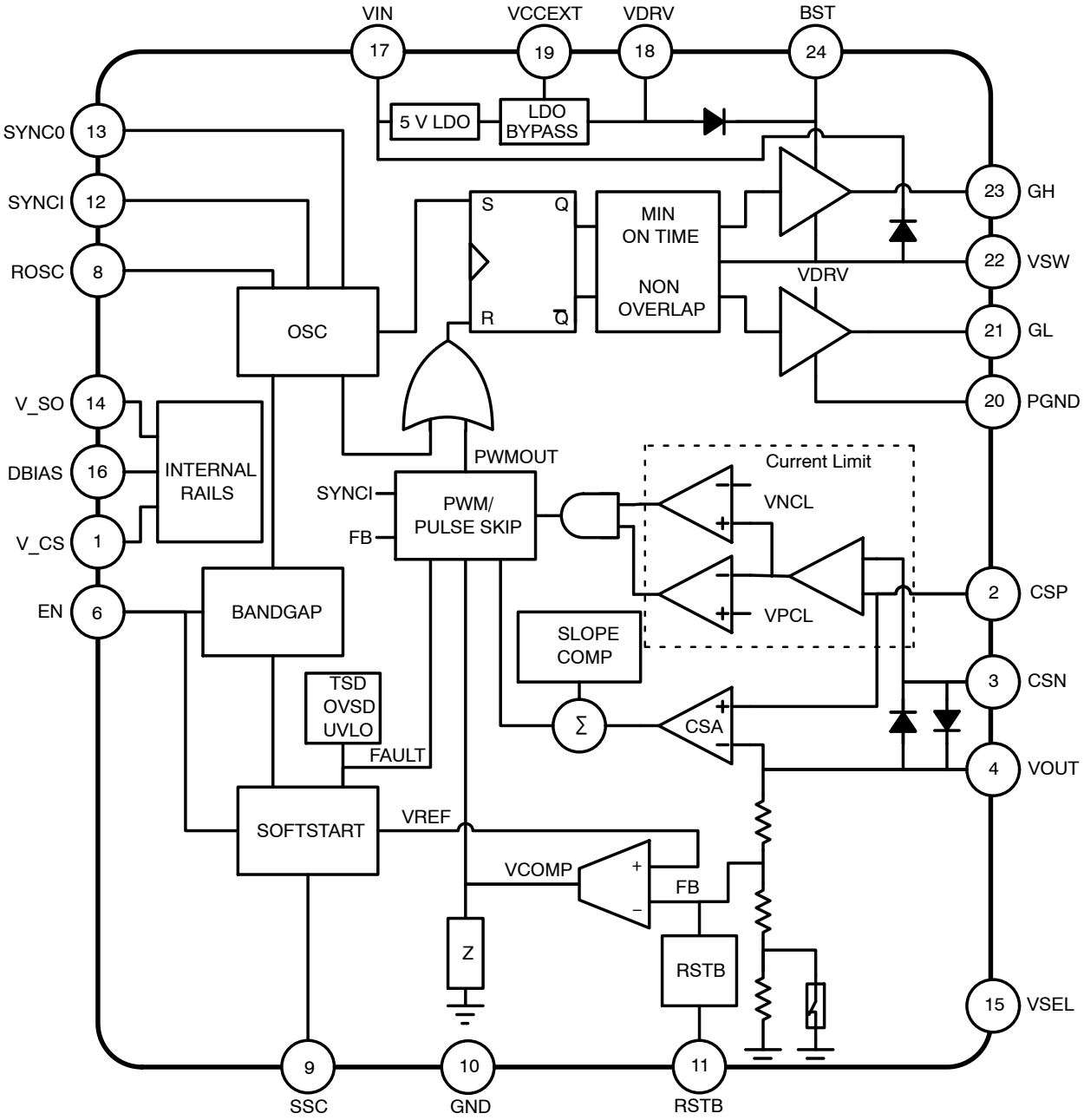

Figure 3. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. QFN24	Pin Name	Description
1	V_CS	Supply input for the internal current sense amplifier. Not intended for external use. Application board requires a 0.1 μF decoupling capacitor located next to IC referenced to quiet GND.
2	CSP	Differential current sense amplifier non−inverting input.
3	CSN	Differential current sense amplifier inverting input.
4	VOUT	SMPS's voltage feedback. Inverting input to the voltage error amplifier. Connect VOUT to nearest point−of−load.
5	NC	No connection (Note 1)
6	EN	Logic level inputs for enabling the controller. May be connected to battery.
7	NC	No Connection (Note 1)
8	ROSC	Use a resistor to ground to raise the frequency above default value.
9	SSC	Soft−start current source output. A capacitor to ground sets the soft−start time.
10	GND	Signal ground. Ground reference for the internal logic, analog circuitry and the compensators.
11	RSTB	Reset with adjustable delay. Goes low when the output is out of regulation.
12	SYNCI	A logic low enables Low I_Q capable operating mode. External synchronization is realized with an external clock. A logic high enables continuous synchronous operating mode (low I_Q mode is disabled). Ground this pin if not used.
13	SYNCO	Synchronization output active in synchronous operation mode. Refer to table for activation delay when coming out of low I_Q mode. Connecting to the SYNCI pin of a downstream NCV881930 results in synchronized operation.
14	V_SO	Supply voltage for the SYNCO output driver. Not intended for external use. Application board requires a 0.1 μF decoupling capacitor located next to IC referenced to quiet GND.
15	VSEL	Output programmed to VSEL_LO when connected to ground or when pin is not connected. Output programmed to VSEL_HI when connected to DBIAS via a 10 kΩ resistor (optional). Voltage setting option will be latched prior to PWM soft−start. Latch will be reset whenever the EN pin is toggled or during a UVLO event.
16	DBIAS	IC internal power rail. Not intended for external use other than for VSEL. Application board requires a 0.1 μF decoupling capacitor located next to IC referenced to quiet GND.
17	VIN	Input voltage for controller, may be connected to battery.
18	VDRV	5 V linear regulator supply for powering NFET gate drive circuitry and supply for bootstrap capacitor.
19	VCCEXT	External 5 V bias supply. Overrides internal high voltage LDO when used. Application board requires a 1 μF decoupling capacitor located next to IC referenced to PGND.
20	PGND	Power ground. Ground reference for the high−current path including the N−FETs and output capacitor.
21	GL	Push−pull driver output that swings between VDRV and PGND to drive the gate of an external low side N−FET of the synchronous buck power supply.
22	VSW	Terminal of the high side push−pull gate driver connected to the source of the high side N−FET of the synchronous buck power supply.
23	GH	Push−pull driver output that swings between SW and BST to drive the gate of an external high side N−FET of the synchronous buck power supply.
24	BST	The BST pin is the supply rail for the gate drivers. A 0.1 μF capacitor must be connected between this pin and the VSW pin. Bootstrap pin to be connected with an external capacitor for powering the high side NFET gate with SW + (VDRV − 0.5 V) and PGND. Blocking diode is internal to the IC.
EPAD		Connect to pin 20 (electrical ground) and to a low thermal resistance path to the environment.

1. True no connect. Printed circuit board traces are allowable.

Table 2. MAXIMUM RATINGS (Voltages with respect to GND unless otherwise indicated)

Rating	Symbol	Value	Unit
DC Supply Voltage (Note 2)	EN, VIN, V_CS	−0.3 to 45	V
Pin Voltage t ≤ 50 ns	VSW	−0.3 to 40 −2	V
Pin Voltage	GH, BST	−0.3 to 45 −0.3 to 7 V with respect to VSW	V
Pin Voltage	CSN, CSP, VOUT	−0.3 to 10	V
Pin Voltage	VDRV, GL, VCCEXT	−0.3 to 7	V
Pin Voltage	RSTB, SYNCI	−0.3 to 6	V
Pin Voltage	DBIAS, ROSC, SSC, SYNCO, V_SO, VSEL	−0.3 to 3.6	V
Operating Junction Temperature	$T_{J(max)}$	−40 to 150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	2	kV
Moisture Sensitivity Level	MSL	1	−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 4)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics (Note 5) Thermal Resistance, Junction−to−Ambient (Note 6) Thermal Characterization Parameter, Junction−to−Top (Note 6)	 $R_{\theta JA}$ ψ_{JT}	 50 13	°C/W

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
6. Values based on copper area of 600 mm^2, 4 layer PCB, 0.062 inch FR−4 board with 2 oz. copper on top/bottom layers and 1 oz. copper on the inside layers in a still air environment with T_A = 25°C.

Table 4. ELECTRICAL CHARACTERISTICS
(V_{EN} = V_{BAT} = V_{IN} = 4.5 V to 37 V, V_{BST} = V_{SW} + (V_{DRV} − 0.5 V), C_{BST} = 0.1 μF, C_{DRV} = 1 μF. Min/Max values are valid for the temperature range −40°C < T_J < 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VIN_LOW						
VIN_low threshold	VIN falling VIN rising	V_{INLF} V_{INLR}	7.0 7.3	7.31 7.65	7.65 8.0	V
VIN_low hysteresis		V_{INLH}	0.25	0.32	0.45	V
Response time			−	5.8	−	μs
SPREAD SPECTRUM DEACTIVATION (VIN_HIGH)						
VIN_high threshold	VIN rising VIN falling	V_{INHR} V_{INHF}	18.4 18.0	− −	20 19.8	V
VIN_high hysteresis		V_{FLHY}	0.15	0.32	0.45	V
Response time			−	16	−	μs

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Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VIN OVERVOLTAGE SHUTDOWN MONITOR						
Overvoltage stop threshold		V_{OVSP}	37.0	38.0	39.0	V
Overvoltage hysteresis		V_{OVHY}	0.5	1.0	1.5	V
QUIESCENT CURRENT						
Quiescent current	VIN = 13 V, EN = 0 V, T_J = 25°C	$I_{Q,SLEEP}$	–	6.0	–	μA
	VIN = 13 V, EN = 0 V, −40°C ≤ T_J ≤ 125°C	$I_{Q,SLEEP}$	–	6.0	10	μA
	VIN = 13 V, EN = 5 V, No switching, T_J = 25°C	$I_{Q,OFF}$	–	30	40	μA
	VIN = 13 V, 100 μA load, VOUT = 5 V, VCCEXT = VOUT, EN = VIN, $T_{ambient}$ = 25°C (Not production tested. Measured on demo board, refer to application note section)	I_{Q100}	–	82	100	μA
DBIAS						
DBIAS voltage	C_{DBIAS} = 0.1 μF	V_{DBIAS}	2.0	–	2.4	V
UNDERVOLTAGE LOCKOUT (Note 8)						
UVLO start threshold	V_{IN} rising	V_{UVST}	4.0	–	4.5	V
UVLO stop threshold	V_{IN} falling	V_{UVSP}	3.2	–	3.5	V
UVLO hysteresis		V_{UVHY}	–	0.9	–	V
ENABLE						
Logic low threshold voltage	Will be disabled at maximum value	V_{ENLO}	0	–	0.8	V
Logic high threshold voltage	Will be enabled at minimum value	V_{ENHI}	1.4	–	–	V
Enable pin input Current	V_{EN} = 5 V	$E_{I,EN}$	–	0.125	0.26	μA
OUTPUT VOLTAGE						
Output voltage during regulation	IOUT > 100 μA NCV881930MW00R2G/A2RG 3.3 V (VSEL = GND) 5.0 V (VSEL = DBIAS)	$V_{OUT,REG}$	 3.234 4.90	 3.30 5.00	 3.366 5.10	V
VOUT−GND resistance	EN = V_{ENLO}, V_{IN} > 4.5 V	$R_{ENLO,VOUT}$	70	100	130	Ω
VSEL						
VSEL input low threshold voltage		V_{LVSEL}	0	–	0.8	V
VSEL input high threshold voltage		V_{HVSEL}	2.0	–	3.3	V
VSEL pin input current	VSEL = DBIAS	$V_{I,SEL}$	–	0.25	0.37	μA
RESET						
Reset threshold 1 (as a function of VOUT)	VOUT decreasing VOUT increasing	K_{UVFAL} K_{UVRIS}	90 90.5	92.5 –	95 97	%
Reset hysteresis (ratio of VOUT)		K_{RES_HYS}	0.5	–	2	%
Noise−filtering delay		t_{RES_FILT}	5	–	25	μs
Reset delay time	I_{RSTB} = 1 mA I_{RSTB} = 500 μA I_{RSTB} = 100 μA	t_{RESET}	– 4 17	1.0 5 24	– 6 32	μs ms ms
Reset delay modes	Power good mode (no delay) Delay mode (see Detailed Operating Description)		1000 –	– –	– 600	μA

Table 4. ELECTRICAL CHARACTERISTICS
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Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET						
Reset output low level	I_{RSTB} = 1 mA	V_{RESL}	–	–	0.4	V
Reset threshold 2 (as a function of VOUT)	VOUT increasing VOUT decreasing	K_{OVRIS} K_{OVFAL}	105 104	106.5 106.5	110 109	%
VOUT Output Clamp Current	VOUT = $V_{OUT,reg(typ)}$ + 10%	$I_{CL,OUT}$	0.5	1.0	1.5	mA
ERROR AMPLIFIER						
Transconductance (Note 3)	Internal to IC	$g_{M,OTA}$	–	26.6	–	μS
Compensation network	Internal to IC NCV881930MW00DRG 3.3 V 5.0 V	$R_{COMP,OTA}$	 – –	 293 347	 – –	kΩ
	Internal to IC (refer to application note section for die distributed capacitance modeling information)	$C_{COMP,OTA}$	–	190	–	pF
	Internal to IC	$R_{0,OTA}$	–	56.7	–	MΩ
Slope compensation		S_a	–	4.1	–	mV/μs
OSCILLATOR						
Switching frequency	4.5 V < VIN < V_{OVSP}, R_{OSC} = open	f_{SW}	369	410	451	kHz
Switching frequency − R_{OSC}	4.5 V < VIN < V_{INHR}/V_{INHF}, R_{OSC} = 9.01 kΩ	f_{ROSC}	471	512	574	kHz
R_{OSC} reference voltage	R_{OSC} = 9.01 kΩ	V_{ROSC}	0.36	0.40	0.44	V
Minimum off time		$t_{OFF,MIN}$	–	49	75	ns
SPREAD SPECTRUM						
Modulation Frequency Range	V_{INLF}/V_{INLR} < VIN < V_{INHR}/V_{INHF}	f_{MOD}	f_{sw}	–	f_{sw}+14%	kHz
SYNCHRONIZATION						
SYNCO output pulse duty ratio	C_{LOAD} = 40 pF, SYNCI = 0 or SYNCI = 1	$D_{(SYNC)}$	40	–	60	%
SYNCO output pulse fall time	C_{LOAD} = 40 pF, 90% to 10%	$t_{R(SYNC)}$	–	4.7	–	ns
SYNCO output pulse rise time	C_{LOAD} = 40 pF, 10% to 90%	$t_{F(SYNC)}$	–	7.0	–	ns
SYNCO Logic High	I_{SYNCO} = 100 μA source current	$V_{SYNCOHI}$	2.2	–	3.45	V
SYNCO Logic Low	I_{SYNCO} = 2 mA sink current	$V_{SYNCOLO}$	–	–	0.4	V
SYNCI pull−down resistance		R_{SYNCI}	50	100	200	kΩ
SYNCI input low threshold voltage		V_{LSYNCI}	0	–	0.8	V
SYNCI input high threshold voltage		V_{HSYNCI}	2.0	–	5.5	V
SYNCI high pulse width		t_{HSYNCI}	100	–	–	ns
External SYNCI Frequency		f_{SYNCI}	369	–	512	kHz
Master Reassertion Time	Time from last rising SYNCI edge to first un−synchronized turn−on. SYNCI = VLSYNCI after falling SYNCI edge SYNCI = VHSYNCI after falling SYNCI edge	$t_{I(SYNC)}$	 – –	 6.10 8.54	 – –	μs
SOFT−START CURRENT						
Soft−start charge current		I_{SS}	6.9	10	14.3	μA
Soft−start complete threshold		V_{SS}	–	1.0	–	V

Table 4. ELECTRICAL CHARACTERISTICS
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Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SOFT−START CURRENT						
Soft−start delay	From EN = 1 until start of charging of soft−start capacitor (DBIAS external capacitor = 0.1 μF)	t_{SSDLY}	−	240	−	μs
PEAK CURRENT LIMITS						
Positive current limit threshold voltage	0 ≤ (CSP − CSN) ≤ 200 mV 1.2 V ≤ CSN ≤ 10.0 V, VIN < VIN_HIGH	$V_{PCL,N}$	45	50	55	mV
	0 ≤ (CSP − CSN) ≤ 200 mV 1.2 V ≤ CSN ≤ 10.0 V, VIN > V_{INH} (Guaranteed by design)	$V_{PCL,H}$	48	53.3	58.7	mV
Current limit response time	Comparator tripped until GH falling edge, (V_{CSP} − V_{CSN}) = $V_{CL(typ)}$ + 5 mV	t_{CL}	−	39	125	ns
Negative current limit threshold voltage	−200 mV ≤ (CSP − CSN) ≤ 0 1.2 V ≤ CSN ≤ 10.0 V	V_{NCL}	−20.5	−35.0	−52.0	mV
Common−mode range			−	VOUT	−	V
CSP input bias source current			−	0.1	1.0	μA
CSN input bias source current		$I_{BIAS,CSN}$	−	30	−	μA
GATE DRIVERS						
GH sourcing ON resistance	V_{BST} − V_{GH} = 2 V	$R_{GHSOURCE}$	1.6	2.5	5.3	Ω
GH sinking ON resistance	V_{GH} − V_{SW} = 2 V	R_{GHSINK}	1.3	2.5	4.3	Ω
GH−VSW resistance		$R_{GH,VSW}$	−	20	−	kΩ
GL sourcing ON resistance	V_{VDRV} − V_{GL} = 2 V	$R_{GLSOURCE}$	1.6	2.5	5.3	Ω
GL sinking ON resistance	V_{GL} = 2 V	R_{GLSINK}	1.3	2.5	4.3	Ω
GL−PGND resistance		$R_{GL,PGND}$	−	20	−	kΩ
GATE DRIVE SUPPLY						
Driving voltage dropout	V_{IN} − V_{DRV}, I_{VDRV} = 25 mA	$V_{DRV,DO}$	−	0.3	0.6	V
Driving voltage source current	V_{IN} − V_{DRV} = 1 V	I_{DRV}	65	100	−	mA
Backdrive diode voltage drop	V_{DRV} − V_{IN}, $I_{d,bd}$ = 5 mA	$V_{D,BD}$	−	−	0.7	V
Driving voltage	I_{VDRV} = 0.1 − 25 mA	V_{DRV}	4.75	5.00	5.30	V
VDRV POR start threshold	(Note 8)	V_{DRVST}	3.75	4.0	4.25	V
VDRV POR stop threshold	(Note 8)	V_{DRVSP}	2.85	3.1	3.35	V
LDO bypass start threshold	VCCEXT rising		4.48	−	4.80	V
LDO bypass stop threshold	VCCEXT falling		4.31	−	4.65	V
LDO bypass input current	Pulse−skip, VCCEXT = 5 V		−	3.1	−	μA
LDO bypass $R_{DS(on)}$	VCCEXT = 5 V, VDRV load = 50 mA		1.07	1.93	2.79	Ω
THERMAL SHUTDOWN						
Thermal shutdown threshold	T_J rising	T_{SD}	155	170	190	°C
Thermal shutdown hysteresis	T_J falling	$T_{SD,HYS}$	5	15	20	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Spread spectrum function will be disabled when IC operated using external frequency synchronization.
8. Operating with VIN near IC UVLO thresholds may result in insufficient gate drive voltage drive amplitude to permit switching of external MOSFETs. Use of an external bias voltage to maintain sufficient VDRV voltage may be required.

Table 5. FUNCTIONALITY INFORMATION TABLE

VIN (V)	SYNCI Pin	Behavior	Frequency	SYNCI Function	SYNCO	Spread Spectrum	ROSC
VIN < Vin_low	Logic−0	Synchronous mode, recirculation FET turns−off when −35 mV current sense voltage is detected. Pulse skip not allowed when VIN < Vin_low.	410 kHz* or less. Minimum off−time may be skipped depending on VIN, output voltage option and operating current.	Disabled	Enabled, 410 kHz	Disabled	Disabled
	Logic−1						
	F_{sync}		F_{sync} if minimum off−time is not skipped	Enabled	F_{sync}		
Vin_low < VIN < Vin_high (No Pulse Skip Condition)	Logic−0	Synchronous mode, recirculation FET turns−off when when < 0 V current sense voltage is detected.	f_{ROSC} with spread spectrum. Upon exiting Pulse Skip mode, first 1−3 pulses 103 kHz followed by 410 kHz pulses.	Disabled	Enabled, follows spread spectrum	Enabled (When exiting Pulse Skip mode, function resumes within 14 410 kHz pulses)	Enabled (Disabled during 1−3 103 kHz pulses upon exiting Pulse Skip mode)
	Logic−1	Forced PWM mode, recirculation FET turns−off when −35 mV current sense voltage is detected.	f_{ROSC} with spread spectrum	Disabled	Enabled	Enabled	Enabled
	F_{sync}		F_{sync}	Enabled	F_{sync}	Disabled	Disabled
Vin_low < VIN < Vin_high (Pulse Skip Condition)	Logic−0	Pulse skip mode	Disabled	Disabled	Disabled	Disabled	Disabled
VIN > Vin_high	X	Synchronous mode, recirculation FET turns−off when −35 mV current sense voltage is detected. Pulse skip not allowed when VIN > Vin_high.	410 kHz	Disabled	Enabled, 410 kHz	Disabled	Disabled
Soft−start	X	Forced PWM mode with pulse skip allowed, recirculation FET turns−off when when < 0 V current sense voltage is detected.	410 kHz	Disabled	Disabled	Disabled	Disabled
Vout undervoltage (K_{UV})	X	RSTB activated	410 kHz	No change in behavior	No change in behavior	Disabled	No change in behavior
Vout overvoltage (K_{OV})	X	RSB activated	No PWM	No PWM	No Change in behavior	No PWM	No PWM

*GH off pulses will be skipped to maintain output voltage regulation whenever GH t_{off} is less than $t_{off,MIN}$ occurs.

THERMAL CHARACTERISTICS

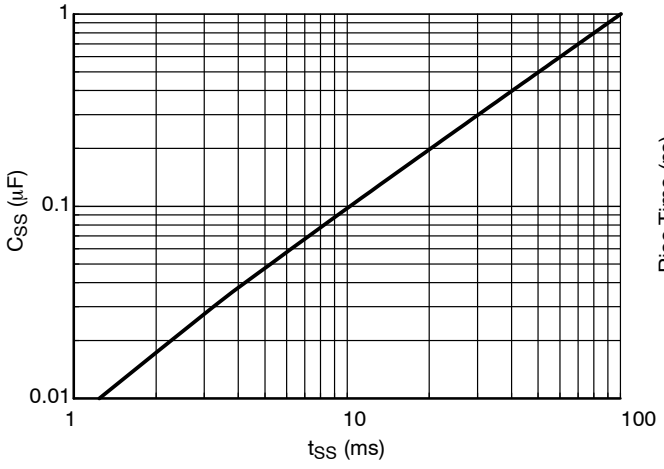


Figure 4. Soft−Start Time vs Capacitance

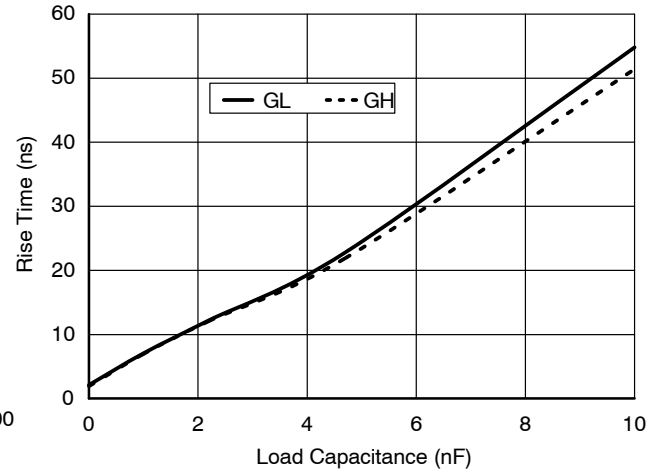


Figure 5. Driver Rise Time vs Load Capacitance

THERMAL CHARACTERISTICS

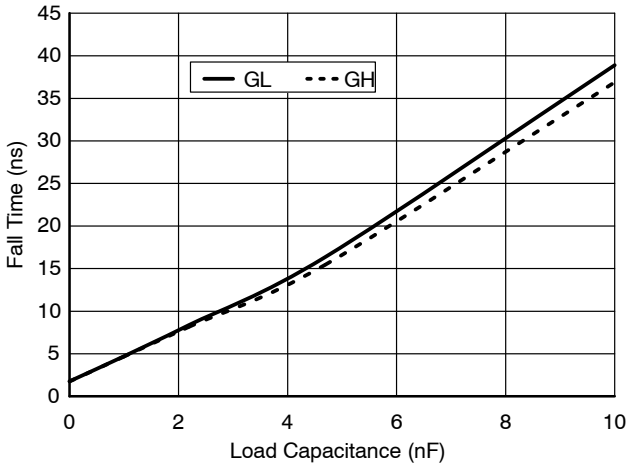


Figure 6. Driver Fall Time vs Load Capacitance

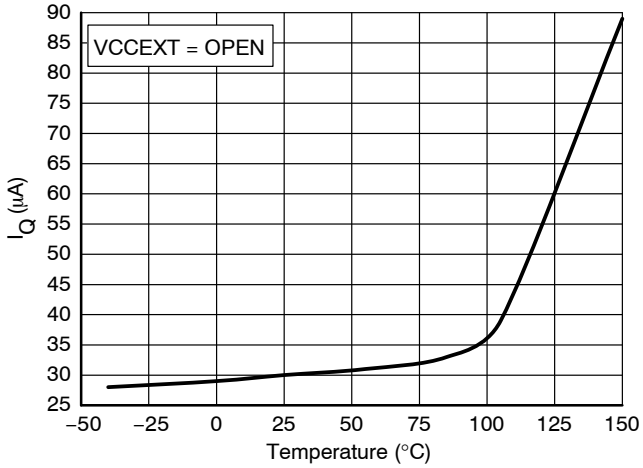


Figure 7. Operating Quiescent Current vs Temperature (5 V/100 μA)

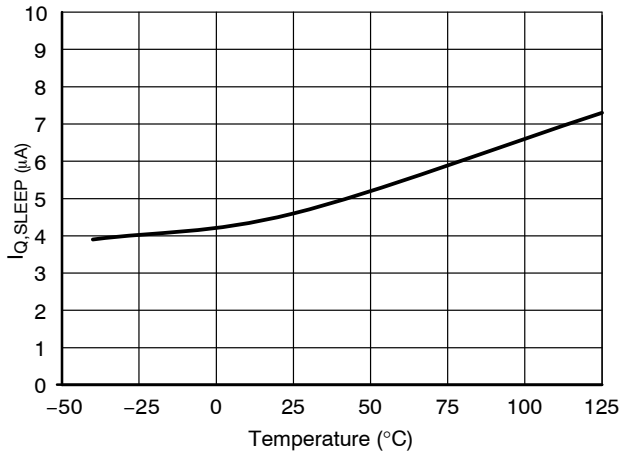


Figure 8. Quiescent Current (Shutdown) vs Temperature

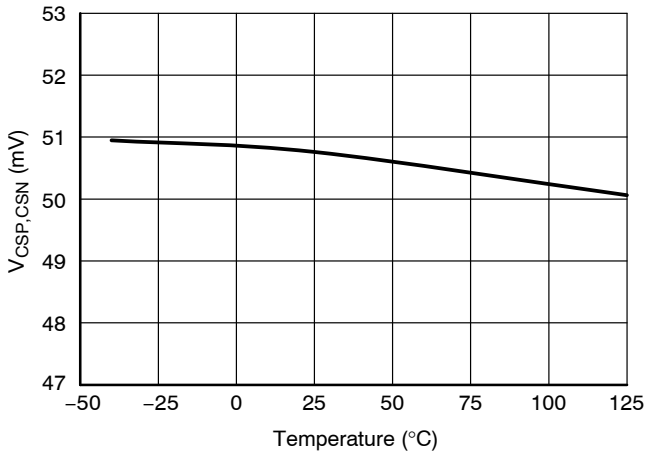


Figure 9. Peak Current−Limit Threshold vs Temperature

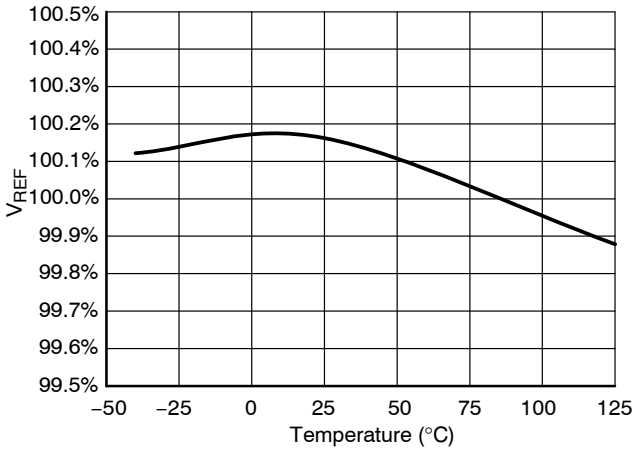


Figure 10. VREF vs Temperature

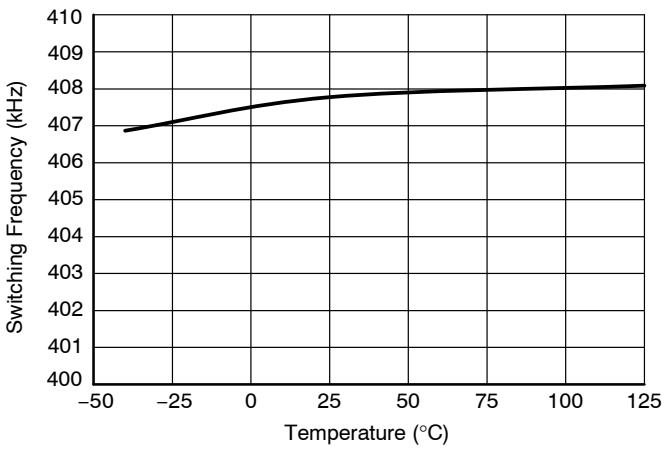


Figure 11. Oscillator Frequency vs Temperature

THERMAL CHARACTERISTICS

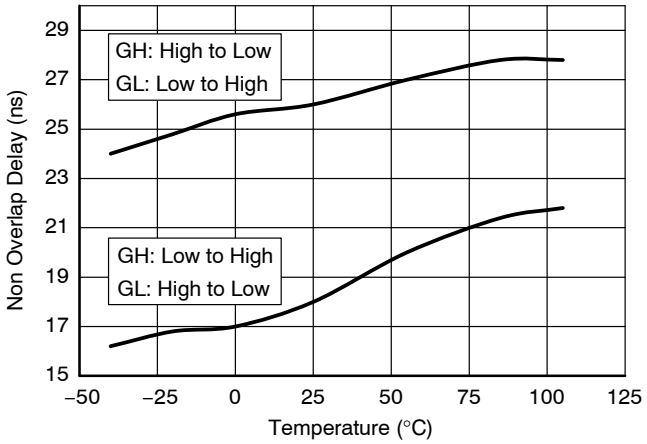


Figure 12. Non−Overlap Delay vs Temperature

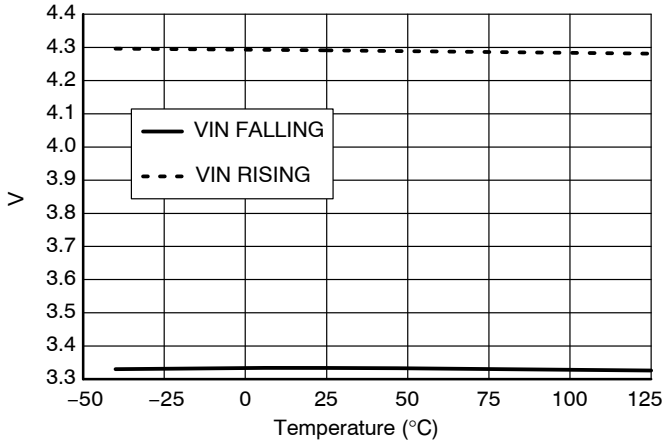


Figure 13. UVLO vs Junction Temperature

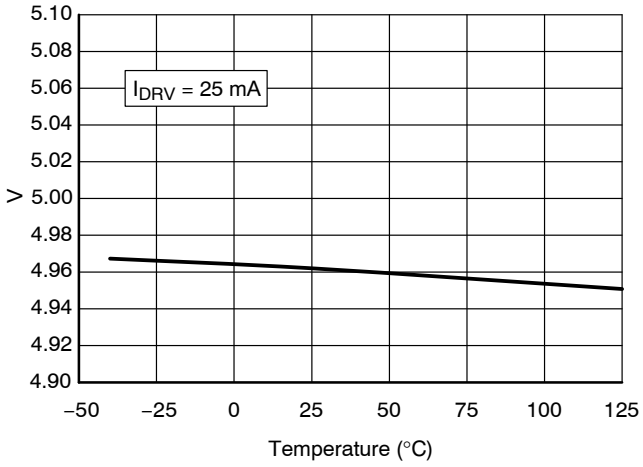


Figure 14. VDRV vs Temperature

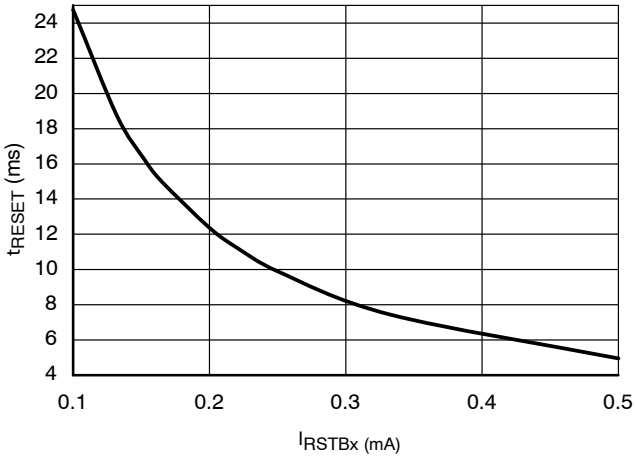


Figure 15. Reset Delay Time vs I_{RSTBx}

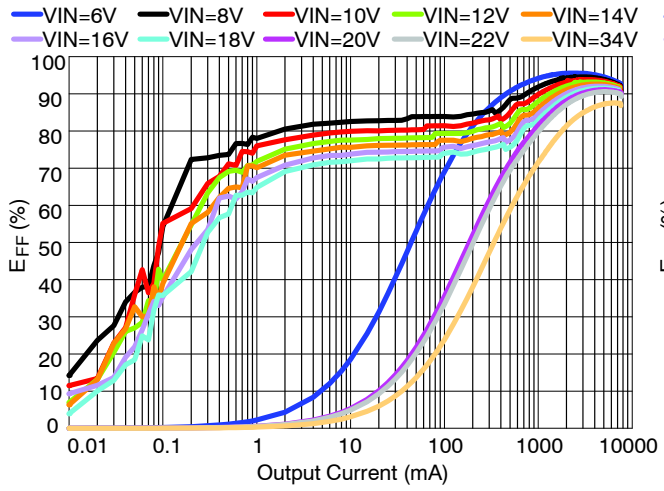


Figure 16. 3.3 V Demo Board Efficiency (SYNCI = 0 V)

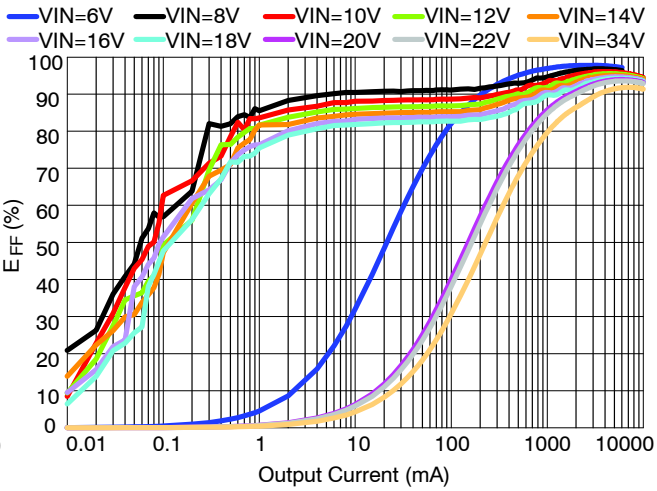


Figure 17. 5 V Demo Board Efficiency (SYNCI = 0 V)

DETAILED OPERATING DESCRIPTION

General

Preset internal slope and feedback loop compensation results in predetermined values for current sense resistors and output filtering.

A capacitor technology mix of ceramic and aluminum polymer or solid aluminum electrolytic capacitors results in a cost effective solution. Non−solid aluminum electrolytic capacitors are not recommended due to their large cold temperature ESR properties. An all ceramic solution filter implementation using 22 μF capacitor (like the GRJ32ER71A226KE11) was considered for Table 6 and Table 7 for a design objective of ±3% transient voltage for a 50% load transient. Tolerances used in determining the number of required capacitors were:

- Initial tolerance
  - −10%
- Temperature tolerance
  - −10.5% at −40 C.
- DC bias voltage
  - −4.5% for 3.3 V, −18.8% for 5 V.
- 100 mV AC RMS voltage
  - −10.5%

At higher currents, optimal inductor and current sense resistor values may become limited. It may be necessary to parallel 3 resistor values to achieve the desired current sense resistor value. The manufacturer's inductor tolerance and properties must be considered when determining the current sense resistor for desired current limiting under worst case component values.

Table 6. VALUE RECOMMENDATIONS

Output Current (A)	MOSFET	3.3 V Option			5 V Option		
		Inductor Value (μH)	Current Sense Resistor (Ω)	Output Capacitance (Ceramic) (μF)	Inductor Value (μH)	Current Sense Resistor (Ω)	Output Capacitance (Ceramic) (μF)
6	NVMFS5C460NL	3.3	(2x0.012) 0.006	242	4.7	(2x0.012) 0.006	198
7	NVMFS5C460NL	3.3	(2x0.011) 0.0055	286	3.3	(2x0.010) 0.005	176
8	NVMFS5C460NL	2.2	(2x0.009) 0.0045	330	3.3	(2x0.009) 0.0045	264
9	NVMFS5C460NL	2.2	(2x0.008) 0.004	352	3.3	(2x0.008) 0.004	286
10	NVMFS5C460NL	2.2	(2x0.007) 0.0035	396	2.2	(2x0.007) 0.0035	286

Input Voltage

An undervoltage lockout (UVLO) circuit monitors the input and can inhibit switching and reset the soft−start circuit if there is insufficient voltage for proper regulation. Depending on the output conditions (voltage option and loading), the NCV881930 may lose regulation and run in drop−out mode before reaching the UVLO threshold. When the input voltage is sufficiently low so that the part cannot regulate due to maximum duty cycle limitation, the high−side MOSFET can be kept on continuously for up to 8 clock cycles (19.5 μs), to help lower the minimum voltage at which the controller loses regulation.

An overvoltage monitoring circuit automatically terminates switching and disables the output if the input exceeds 37 V (minimum). However, the NCV881930 can withstand input voltages up to 45 V.

Output Voltage

The output may be programmed to VSEL_LO when VSEL is ground referenced.

When VSEL is connected to DBIAS via an optional 10 kΩ resistor, the output voltage is programmed to VSEL_HI.

The output voltage setting option must be selected prior to enabling the IC via the EN pin. The voltage setting option will be latched prior to initiation of soft−start. The voltage option latch will be reset whenever the EN pin is toggled or during a UVLO event.

IC−VIN

A 1 μF decoupling capacitor is recommended between IC−VIN and ground. PCB layout inductance separating this decoupling capacitor and the input EMI capacitor may result in low amplitude high−Q ringing. A 1 Ω damping resistor between the PCB VIN and IC−VIN is recommended.

Switching noise will be greater at the high side drain than at the input EMI ceramic filter capacitor. The trace providing voltage to IC−VIN should originate from the EMI ceramic filter capacitor.

The VOUT pin sinks 0 mA under typical conditions when the SYNCI pin is logic−low. The VOUT pin sinks 1 mA when any of the following conditions are present:

- SYNCI = logic−high
- SYNCI is driven by an external clock

- VIN < VIN_low threshold
- VIN > frequency foldback threshold voltage

VCCEXT

VIN supplies VDRV and logic power via the IC's internal LDO. VCCEXT pin is ignored if connected to a voltage less than 5 V or is left unconnected. For improved efficiency, an external 5 V source may be connected to VCCEXT to permit bypassing of the internal LDO (Table 7). The LDO bypass efficiency improvement is reduced at lower currents when the IC enters pulse−skip mode. An IC power consumption reduction of about 100 mW has been measured on a demo board configured with NVMFS5C460NL power transistors at an input voltage of 13 V.

Table 7. NCV881930MW00R2G/AR2G 5 V DEMO BOARD TYPICAL IC POWER CONSUMPTION IMPROVEMENT

VCCEXT = VOUT vs VCCCEXT = OPEN, I_{OUT} > 1 A							
VIN (V)	6	8	10	12	14	16	18
mW	8.7	33.7	58.6	83.3	108	131	156

When the NCV881930MW00R2G/AR2G is configured for a 5 V output (VSEL connected to DBIAS) and VCCEXT is connected to the power supply's output, VFB and CSN traces must be independent from the VCCEXT power trace. VDRV circuitry gate drive current pulses circulate through the VCCEXT PCB trace. Voltage disturbance from the trace parasitic layout inductance will distort CSN and IC−VOUT measurements.

The IC structure has a 2 series anode−cathode diode path between pins VCCEXT and VIN (Figure 18). If the controller VIN power source is disconnected while VCCEXT is connected to an independent external 5 V supply, the diode path will deliver current to the converter's input. VIN pin may remain biased to VCCEXT minus 2 diode drops and could supply other devices sharing the same rail as the IC. To avoid unpredictable operating behavior, the EN pin must be set to a logic−low state to disable PWM operation upon disconnection of the IC's power source and independent VCCEXT power source must be disabled if the IC VIN rail is shared by other devices.

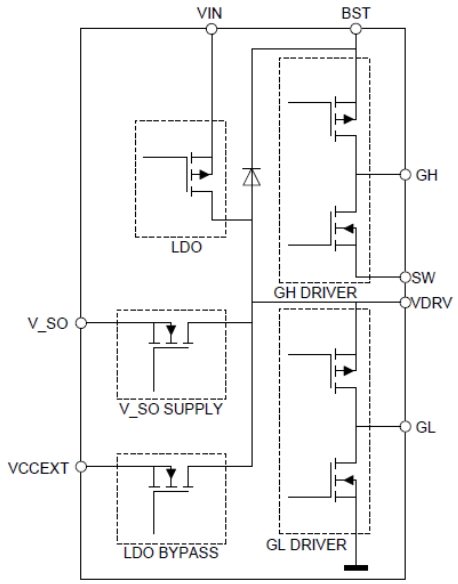


Figure 18. VCCEXT to VIN Diode Path

Soft−Start

The NCV881930 features an externally adjustable soft−start function, which reduces inrush current and overshoot of the output voltage. Figure 19 shows a typical soft−start sequence.

Soft−start is achieved by charging an external soft−start capacitor connected to the SSC pin via an internal 10 μA current source. Should the FB voltage slew rate be less than that of the SSC, the SSC pin will be clamped to V(FB) + 123 mV. Once the SSC voltage is greater than 0.75 V, the clamp is released.

During soft−start, the SYNCI function is disabled and the controller will operate in diode−emulation mode. Pulse skip is allowed. The logic will enable the SYNCI function once SSC voltage exceeds 1.075 V.

Following activation of the EN pin, there will be eight ~250 ns GL pulses (102.5 kHz repetition rate) prior to initiation of the soft−start to charge the bootstrap capacitor. During this event, there will be no GH pulses. If VOUT is < ~0.2 V at EN activation, the pulses are not required and the logic may disable the eight GL pulses.

Should the power supply output voltage foldback from current limiting, it is necessary to prevent the feedback opamp from clamping high to avoid output overshoot when current limiting ends. If the opamp feedback pin is less than 750 mV, the SSC pin voltage will be discharged to the opamp feedback voltage + 123 mV (Figure 19). Voltage returns to nominal regulation via soft−start behavior.

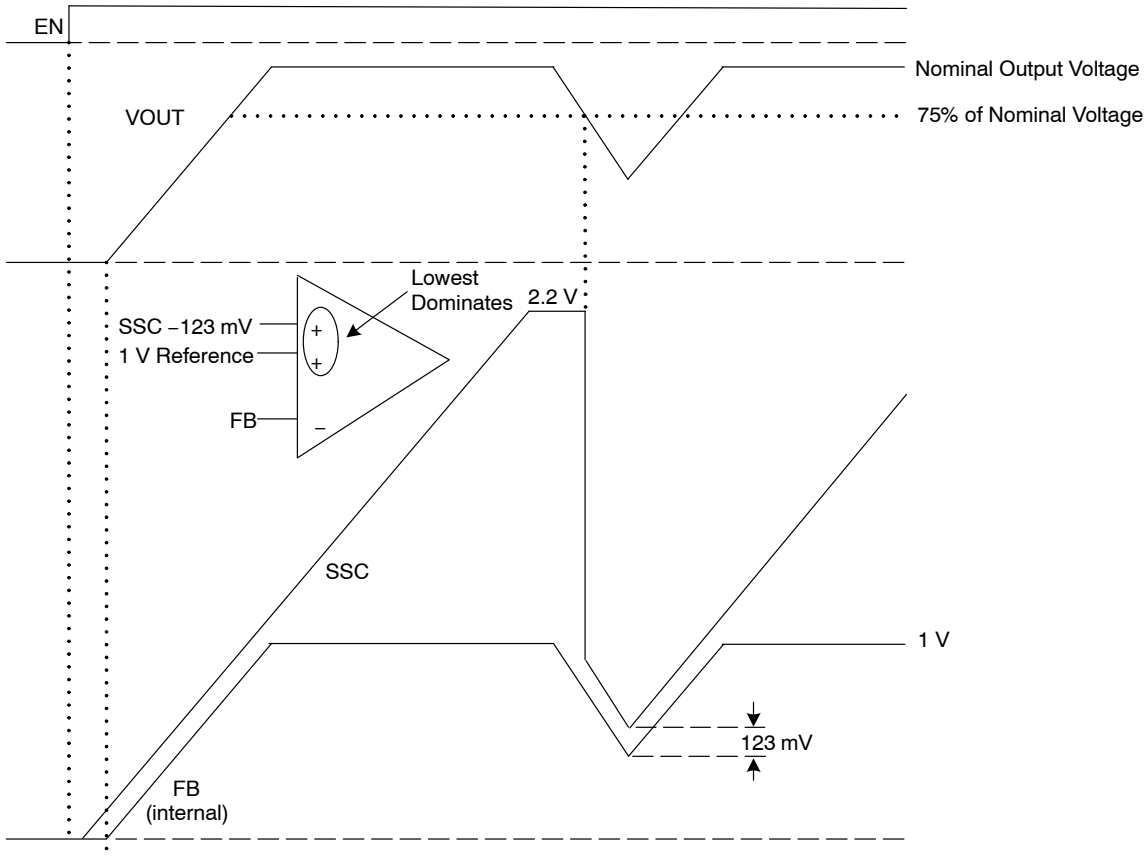


Figure 19. Soft−Start Behavior During Output Overload Current Limiting Event

Equation 1 t_{ss} may be used to calculate soft−start time for soft−start capacitor C_{ssc} (Farads).

$$t_{SS} = t_{SSDLY} + C_{SSC} \frac{1\ V}{10\ \mu A}\ (s) \qquad \text{(eq. 1)}$$

State Diagram

Figure 20 and Figure 21 illustrate the state diagram for the NCV881930.

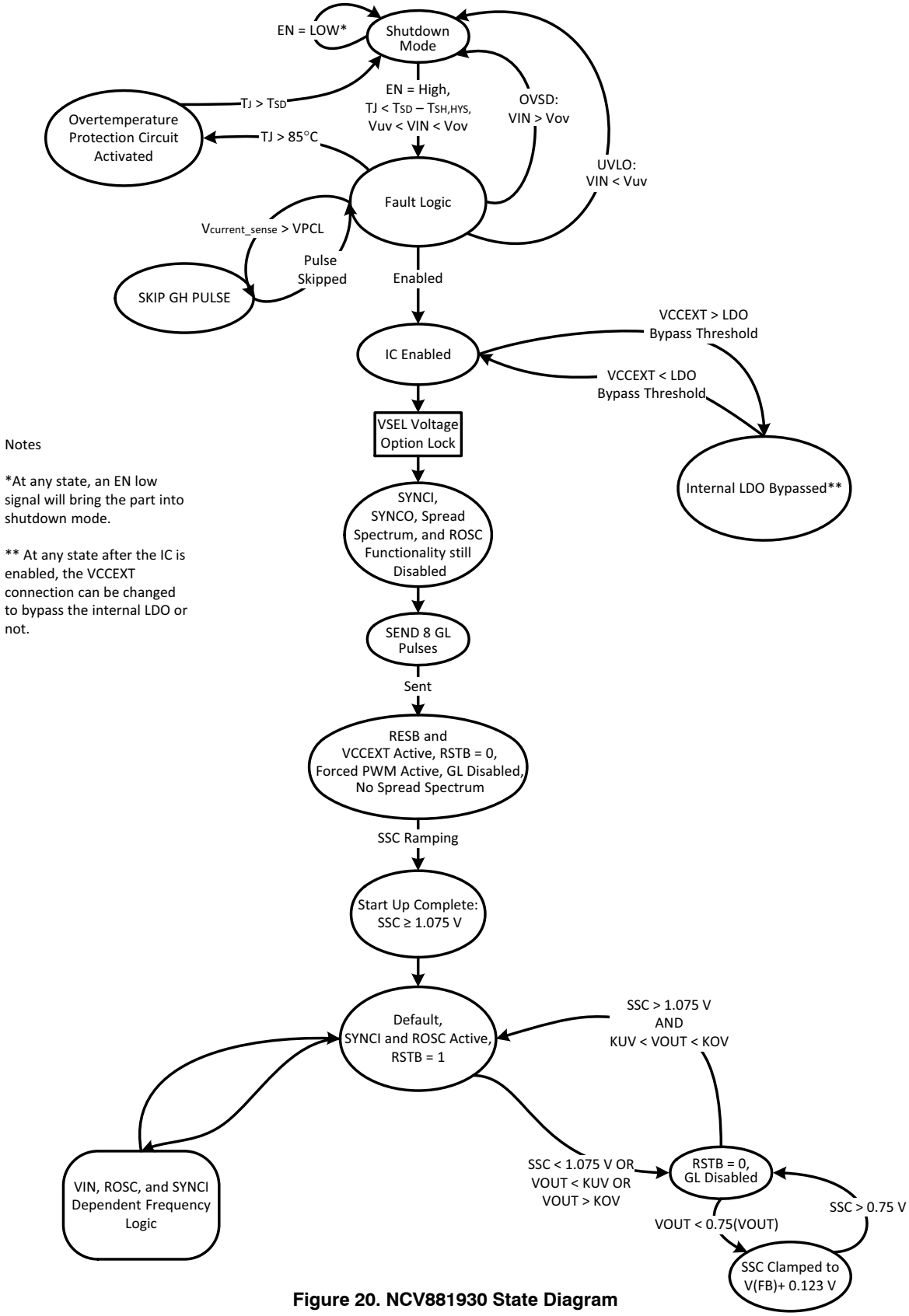


Figure 20. NCV881930 State Diagram

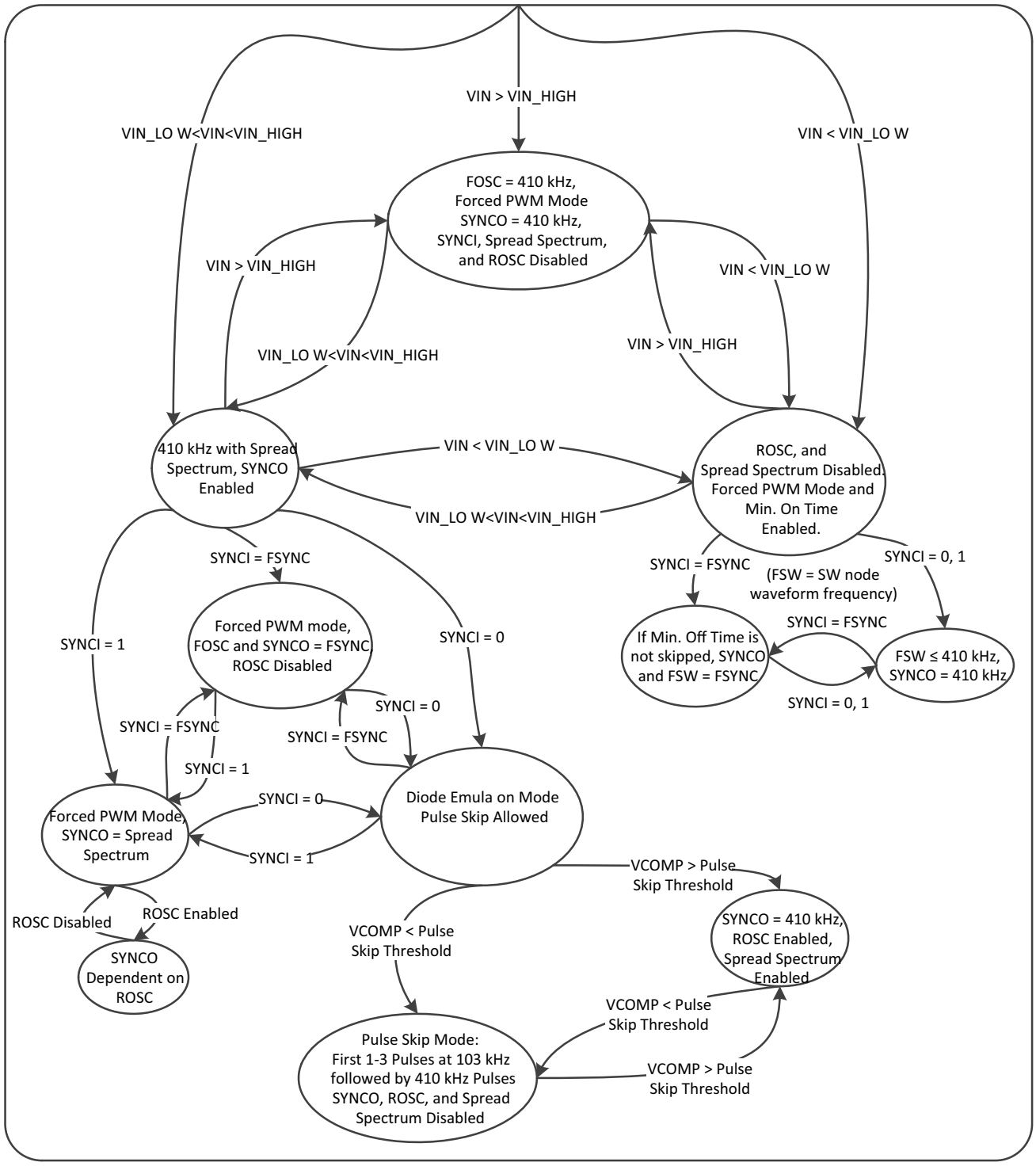


Figure 21. NCV881930 State Diagram – Dependent Switching Logic

Peak Current Mode Control

The NCV881930 incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as the frequency clock to ensure a PWM switching operation. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage transients. This eliminates the delay caused by the output filter and the error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse−by−pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This permits simpler internal compensation.

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope compensation signal requires the inductor to be less than a maximum value, depending on output voltage, in order to avoid sub−harmonic oscillations. Recommended inductor values are described in Table 6. Other values may be possible.

Current Sensing (CSP−CSN):

V_CS is derived from VIN. It is a supply input for the internal current sense amplifier and should never be used to power external circuitry. The V_CS ceramic decoupling capacitor a minimum of 50 V voltage rating. Ground this pin if not used.

Kelvin connections to current sense resistor (RSNS) are required. CSP−CSN feedback nodes must not be in−line with the power path. An example of a good design practice is to connect the sense lines at the center of the inside edge of the sense resistors (Figure 22).

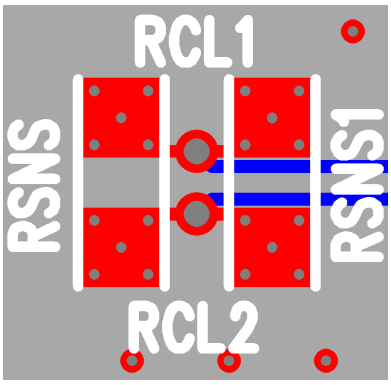


Figure 22. Kelvin Sense Location for Parallel Current Sense Resistors

As a result of the IC's CSP−CSN high input impedance, noise reduction measures should be used for effective noise immunity from the current sense feedback traces.

- Current sense resistors have a small inherent parasitic inductance that will result in a small voltage excursion equaling $L_{RSNS} \bullet \delta I_L/\delta t$ distortion superimposed on the triangular current sense waveform. The differential noise resulting from such a distortion can be minimized with the use of parallel sense resistors. The amplitude of such a distortion is difficult to predict (data not normally provided in resistor datasheets), validation of current limit response during power supply bench evaluation is required.
- Trace routing must not be adjacent to a switch node or other high noise trace.
- Traces should be coincident with of each other on inner layers to minimize coupling from external radiated fields. Traces should be shielded by a top or bottom ground layer (use both layers when possible).
- On layers having the feedback traces, there should be a ground poor next on each side of the traces for additional shielding.
- It is recommended that an output filter ceramic capacitor be located near RSNS/RSNS1 to help mitigate output switching noise at RSF2.
- An optional R−C−R π−filter on the IC's CSP/CSN pins (Figure 23) is sometimes used to filter differential and common mode noise.
- To avoid creating a common−mode noise filter imbalance at the IC current sense pins, simple RC differential filters are not recommended.
- The π−filter must be adjacent to the IC to minimize field induced noise sensitivity on the high impedance side (IC side) of the filter.
- If used, a π−filter −3 dB roll−off frequency > 1 MHz is recommended to prevent the filter transfer function zero from influencing the feedback loop response. RSF1 = RSF2 = 49.9 Ω and CSF1 =100 pF is a recommended starting point.

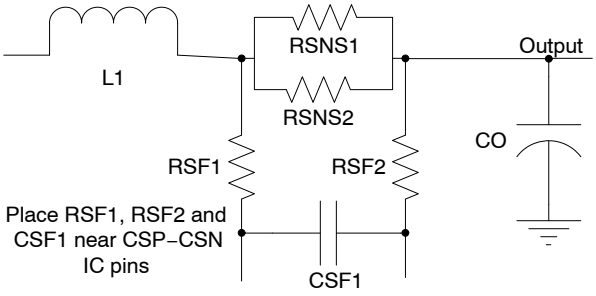


Figure 23. Current Sense Resistor π−Filter

CSN pin sources a bias current of amplitude $I_{BIAS,CSN}$. RSF2 will create a voltage offset on the CSP−CSN differential current sense current. This offset may be taken into account using the following current CSP−CSN current sense expression.

$$I_{L_PEAK} = \frac{V_{CSP_CSN}}{RSNS} = \frac{V_{RSNS} + R_{SF2} \cdot I_{BIAS_CSN}}{RSNS} \quad \text{(eq. 2)}$$

There is a diode path between IC−CSN and IC−VOUT. This diode path could conduct and interfere with the feedback loop if an appreciable voltage drop is present between the 2 pins. Intentional voltage drop on the power path between the CSN side of the current sense resistors (CSN) and the IC−VOUT feedback kelvin point is to be avoided.

Short Circuit Protection

When the peak inductor current reaches the current limit threshold, duty−cycle limiting occurs and output voltage will be foldback accordingly.

A GH pulse skip will occur under severe short−circuit conditions if the inductor current exceeds the peak current limit threshold at the beginning of the next GH activation cycle. GL pulses will continue to operate during this GH pulse skip operation.

Reset

The RSTB pin is a high impedance node. To minimize noise coupling onto its PCB connected trace, care must be exercised during PCB layout to avoid running the trace adjacent to a switching node.

When EN is in low−state irrespective of VIN voltage, RSTB is floating (high impedance). When the voltage on the VOUT pin is out of regulation below K_{UVFALL} or greater than K_{UVRIS}, the open−drain output RSTBx is asserted (pulled low) after a short noise−filtering delay ($t_{RES-FILT}$). A pull−up resistor is required to generate a logic−high signal on this open−drain pin and to set the delay time, simplifying the connection to a micro−controller. The pin can be left unconnected if the function is unused.

The RSTB signal can either be used as a reset with delay or as a power good (no delay). The delay is determined by the current into the RSTB pin, set by a resistor, show in Figure 24.

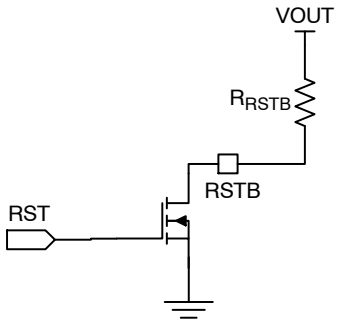


Figure 24. Reset Delay Time

Use the following equation to determine the ideal reset delay time using currents less than 500 μA:

$$t_{RESET} = \frac{9.9}{4 \cdot I_{RSTBx}} \quad \text{(eq. 3)}$$

where

t_{RESET}: ideal reset delay time (ms)
I_{RSTB}: current into the RSTB pin (mA)
Using I_{RSTB} = 1 mA removes the delay and allows the reset to function as a “power good” pin.

The RSTB resistor is commonly tied to VOUT. A RSTB resistor value setting the current at the reset pin in the range of 0.6 mA to 1 mA is not recommended due to the variation of the threshold between a set delay time and power good. Depending on the output voltage option, typical reset delay times for a 3.3 V pull−up can be achieved with the following resistor values.

Table 8.

R_{RSTB} (kΩ, VOUT pull−up)	t_{RESET} (ms) – VSEL_LO (VOUT = 3.3 V)	t_{RESET} (ms) – VSEL_HI (VOUT = 5 V)
6.65	5	–
10	7.5	5
15	11.3	7.4
20	15.0	9.9
24.9	18.7	12.3
33.2	24.9	16.4

In the event of an overvoltage (VOUT > K_{UVRIS}), an internal comparator enables a 1 mA current source discharge path on VOUT within typically 2.7 μs. The overvoltage comparator is set 7.5% above the 1 V feedback voltage reference (i.e. 1.075 V) and has a 68 mV hysteresis.

Enable

An EN pin ground referenced resistor is not required. The IC has a pull−down current ($E_{I,EN}$). For low system I_Q operating requirements, such a resistor would result in a larger input quiescent current consumption when the IC is in an enabled state.

The NCV881930 is designed to accept either a logic−level signal or battery voltage as an Enable signal. However, if voltages above 45 V are expected, EN should be tied to VIN through a 10 kΩ resistor to limit the current flowing into the pin’s internal ESD clamp.

A low signal on Enable induces a shutdown mode which shuts off the regulator and minimizes its supply current to less than 6 μA by disabling all functions. Pull−down R_{ENLO_VOUT} between IC−VOUT and IC−GND is present if VIN > 4.5 V to permit discharging the power supply output voltage.

Once the IC is enabled, a soft−start is always initiated.

The IC has internal filtering to prevent spurious operation from noise on EN. There is a t_{SSDLY} delay between the EN command entering a logic−high state and initiation of

soft−start activity on pin SSC. There is an approximately 15 μs delay between the EN command entering a logic−low state and cessation of PWM activity.

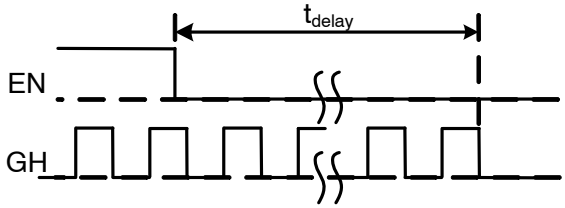


Figure 25. EN Low Response Behavior

The low I_Q IC feature is active in diode−emulation mode only. With exception of the overtemperature protection function and output voltage monitoring function used to initiate GH pulse bursts for output voltage regulation, non−essential functions are turned−off to minimize quiescent current consumption.

Duty Cycle and Maximum Pulse Width Limits

Maximum GH duty ratio is defined by $t_{off,MIN}$, the minimum permissible GH off time. When this maximum duty ratio is reached while VIN < VIN_LOW, one or more GH off cycle pulse will be skipped to permit maintaining output voltage regulation. Although the internal 410 kHz clock frequency remains unchanged, skipping a GH off pulse results in a measured reduction of the operating frequency. For instance, skipping a single GH off pulse results in a 205 kHz measured waveform frequency.

When VIN < VIN_LOW and VOUT falls below regulation, the period on GH pin on−time is 19.5 μs and the off−time is 200 ns (Figure 26). If this occurs while operating under light load, the VSW pin has 70 ns to decay below 0.4 V for the internal logic to set the GL pin high. If the VSW pin is greater than 0.4 V after 70ns, the GL pin will be forced high for 100 ns (Figure 27).

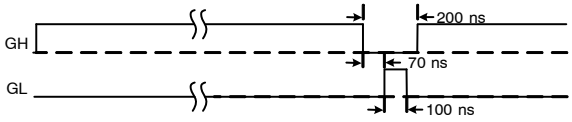


Figure 26. Gate Drive Waveforms for VSW < 0.4 V Within 70ns of GH Going Low

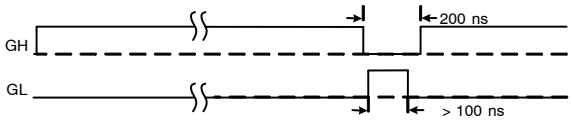


Figure 27. Gate Drive Waveforms for VSW > 0.4 V After 70ns of GH Going Low

Feedback Voltage Error Amplifier

An operational transconductance amplifier (OTA) is used to condition the feedback voltage information. The OTA output can sink/source up to 3 μA. During normal operation, the minimum error amplifier voltage operates between a minimum of 1.0 V and 2.2 V.

During startup, there is no minimum clamp voltage on the OTA output.

At light load, the logic will enter pulse−skip operating mode. During pulse−skip mode the minimum voltage clamp is 0.975 V, changing to 1.075 V during initial low frequency pulse burst (up to 3 pulses).

The voltage feedback and compensation networks are represented in Figure 28. $Z_U(s)$ and $Z_L(s)$ are resistor networks used as the input voltage feedback divider. R_o and C_o are the OTA output impedance characteristic. $Z_{comp}(s)$ is the OTA compensation network establishing the cross−over frequency and phase margin. Block A(s) is a level shift block having an AC gain of 0.1875.

The silicon implementation of the compensation resistor in $Z_U(s)$, $Z_L(s)$, and $Z_{comp}(s)$ consists of numerous series connected high resistance segments. Each resistor segment has a very low parasitic capacitance to ground. On a cumulative basis, the distributed capacitances may not be neglected as they affect the feedback loop phase response at cross−over frequency. A feedback loop analysis making use of datasheet parameters R_{comp} and C_{comp} without taking into account the described distributed capacitances is to be avoided.

The web model contains the necessary information to establish analytical models for $Z_U(s)$, $Z_L(s)$, $Z_{comp}(s)$ and A(s). $Z_L(s)$ and $Z_{comp}(s)$ will be different between VSEL output voltage options.

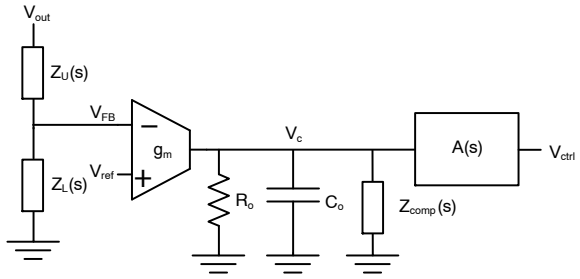


Figure 28. OTA Feedback and Compensation Block Diagram

Bootstrap

During startup, the bootstrap capacitor is charged by a sequence of eight 250 ns GL pulses having a 2 μs period before the SSC pin is allowed to ramp up. For additional details, refer to the Soft−Start detailed application information.

Drivers

The NCV881930 has gate drivers to switch external N−Channel MOSFETs. This allows the NCV881930 to address high−power, as well as low−power conversion requirements. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry increases

efficiency, which minimizes power dissipation, by minimizing the body diode conduction time, while protecting against cross−conduction (shoot−through) of the MOSFETs. A block diagram of the non−overlap and gate drive circuitry used in the chip and related external components are shown in Figure 29.

The GL driver is enabled when VSW is less than the non−overlap detection comparator threshold of 0.4 V. The GL driver response time is dependent on the comparator differential voltage that develops below the 0.4 V detection threshold; approximately 25 ns response time may be expected when operating in continuous conduction mode.

To maintain output voltage regulation when SYNCI = 0 V (or open) and VINLx < VIN < VIN_HIGH, GH on−time may be as low as 0 ns during non−pulse skipping mode operation. MOSFET response will depend on its Q_g(tot) characteristics.

If the SW pin voltage is still greater than 0.4 V 70 ns following the rising edge of the SYNCI pulse, the IC logic will send a GL pulse to force a recharge of the bootstrap capacitor. The GL pulse width will be no greater than the SYNCI pulse width minus 70 ns. The GL pulse width must be of sufficient duration to fully turn−on the low side MOSFET. The time duration required to turn−on the low side MOSFET will be dependent on the MOSFET's gate charge specification.

The GH driver is enabled when GL voltage is less than the non−overlap detection comparator threshold of 2 V. The GH driver response time is dependent on the comparator differential voltage that develops below the 0.4 V detection threshold; response time is approximately 40 ns.

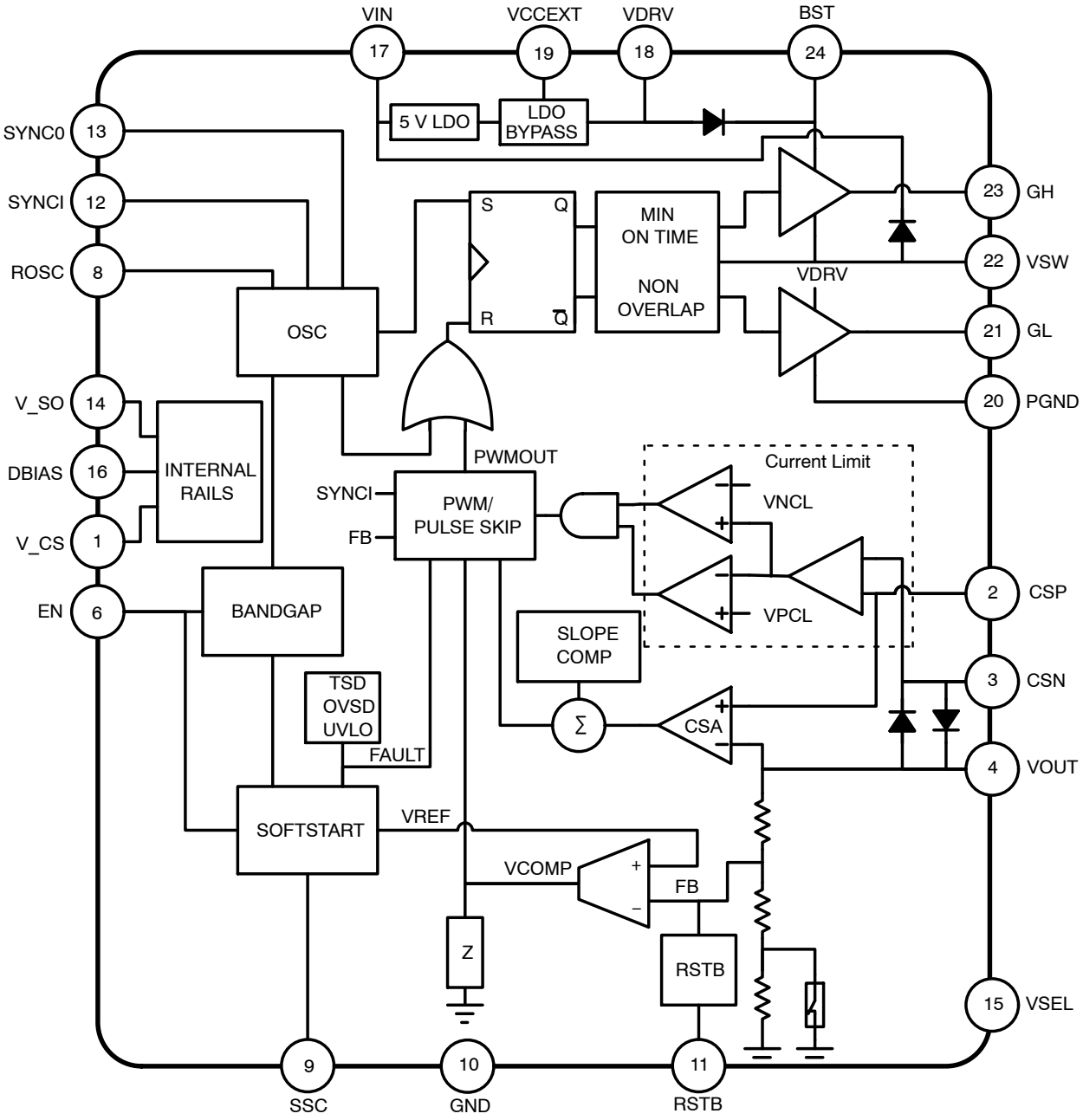


Figure 29. Simplified Block Diagram

A capacitor is placed from Vsw to BST and an internal bootstrap diode is located between VDRV to BST to create a bootstrap supply on the BST pin for the high−side floating gate driver. This ensures that the voltage on BST is about 4.5 V higher than V_{SW} to drive the high−side MOSFET. The boost capacitor supplies the charge used by the gate driver to charge up the input capacitance of the high−side MOSFET, and is typically chosen to be at least a decade larger than its gate capacitance. Since the BST capacitor recharges when the low−side MOSFET is on, pulling Vsw down to ground, the NCV881930 has a minimum off−time. This also means that the BST capacitor cannot be arbitrarily large, since VDRV needs to be able to replenish charge during this minimum off−time so the high−side gate driver doesn't run out of headroom. VDRV must supply charge to both the BST capacitor and the low−side driver, so the VDRV capacitor must be sufficiently larger than the BST capacitor. A 10:1 VDRV/BST capacitor ratio is effective. A 1 μF VDRV capacitor along with a 0.1 μF BST capacitor is recommended.

Careful selection and layout of external components is required to realize the full benefit of the onboard drivers. The capacitors between VIN and GND and between BST and Vsw must be placed as close as possible to the IC. The current paths for the GH and GL connections must be optimized to minimize PCB parasitic resistance and inductance.

SYNC Feature

V_SO is a supply voltage strictly intended for the SYNCO output driver and should never be used to power external circuitry. The V_SO ceramic decoupling capacitor a minimum of 5 V voltage rating. Ground this pin if not used.

An external pulldown resistor is recommended at the SYNCI pin if the function is unused. The SYNCO pulse may be used to synchronize other NCV881930 ICs. If a part does not have its switching frequency controlled by the SYNCI input, the part will operate at the oscillator frequency. A rising edge of the SYNCI pulse causes an NCV881930 to send a GH pulse. If another rising edge does not arrive at the SYNCI pin, the NCV881930 oscillator will take control after the master reassertion time delay which may last up to 3 clock cycles if SYNCI is stopped at logic−low level, up to 4 cycles if SYNCI is stopped at logic−high level. During the master reassertion time, GH will be off and GL will be active−high (i.e. switch node tied to ground). As a result, SYNCI operating mode change should be avoided.

After soft−start event, SYNCO becomes active when SSC voltage > 1.075V. V_{HSYNCI} requires about 2 V headroom from VIN to for its rated amplitude. Amplitude will be reduced when VIN is below approximately 5 V.

During pulse−skip mode, the oscillator enters sleep mode for low I_Q operation power management and SYNCO is inactive. SYNCO functionality resumes when the IC exits pulse−skip mode.

When active, SYNCO is in phase with SYNCI (Figure 30). Rise/fall edge waveforms have a typical 10 ns delay relative to corresponding SYNCI waveform edges.

SYNCO will be a fixed frequency 410 kHz signal under normal voltage when part is in current limit and VOUT drops by 7.5% (K_{UVFAL}).

The VOUT pin sinks 0 mA under typical conditions when the SYNCI pin is logic−low. The VOUT pin sinks 1 mA when any of the following conditions are present:

- SYNCI = logic−high
- SYNCI is driven by an external clock
- VIN < VIN_low threshold
- VIN > frequency foldback threshold voltage



Figure 30. SYNCO Behavior

Ch 1: SYNCI (2 V/div)
Ch 2: SYNCO (5 V/div)
Ch 3: GH (10 V/div)
Ch 4: GL (5 V/div)

Diode−Emulation Mode

Diode−emulation mode is active when SYNCI is either open or grounded. A comparator in the current sense block detects the CSP−CSN voltage transition from a positive voltage (positive inductor current) to 0 V (0 A inductor current). When 0 A is detected, the bottom GL signal turns off the low side MOSFET to prevent negative inductor current.

Pulse−Skip Mode

Pulse−skipping is used at near discontinuous conduction mode operation as a method to improve low current operating efficiency. Pulse−skip PWM regulation is used to mimic discontinuous conduction mode (DCM) behavior (Figure 31). The architecture does not use current sensing for pulse−skip detection. The current sense amplifier response time and its input voltage hysteretic characteristics would have resulted in potentially objectionable output voltage ripple. Instead, the internal voltage feedback OTA compensation output voltage (VCOMP) is used to monitor near−DCM operating condition.

- When VCOMP reaches a predetermined lower voltage threshold, the IC control logic enters pulsed−skip mode to maintain regulation. Some output voltage ripple associated with the pulse skipping is to be expected.
- Low−I_Q operating mode is entered during pulse−skipping event, permitting higher efficiency operation under low output power operation. The duration is dependent on operating conditions. When the controller exits pulse−skip mode, normal PWM regulation is preceded by up to three ~103 kHz pulses (410 kHz/4) as internal logic comes out of low−I_Q mode.
- As the OTA VCOMP is used for feedback control, the VCOMP will not remain constant, increasing to resume PWM activity.

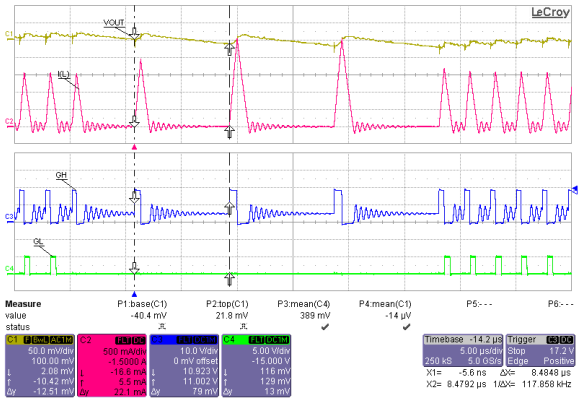


Figure 31. IC Pulse−Skip PWM Behavior, Borderline Pulse−Skip Region

Ch 1: Power supply output voltage (50 mV/div)

Ch 2: Output inductor current (0.5 A/div)

Ch 3: IC gate high (GH) (10 V/div)

Ch 4: IC gate low (GL) (5 V/div)

The thermal shutdown protection circuitry is activated at $T_J \approx 85°C$ and remains active during pulse−skipping, consuming additional quiescent current.

Feedback Loop Measurement

The compensation network and voltage feedback OTA are internal to the IC. Monitoring points permitting measurements of the modulator control−to−output response and the OTA compensation network are not accessible. The open−loop−response in closed−loop−form may be measured by injecting a signal between the power supply output and IC−VOUT. The signal injection path must not share a power path; traces to IC−VCCEXT and IC−CSN must kept outside the signal injection path.

When operating in diode−emulation mode, the OTA feedback loop is disabled when pulse skipping occurs and a hysteretic type mode control is activated. It may be found in literature that feedback loop measurements from small signal injection with hysteretic control yields meaningless information.

Current Limiting and Overcurrent Protection

Current limit activation propagation delay between the sense resistor reaching the threshold and the GH gate turning off is typically about 39 ns. Voltage regulation continues despite slight increase in peak inductor current as a consequence of this current limit propagation delay. If the peak inductor current occurs after this propagation delay, duty ratio will decrease.

Oscillator

The ROSC resistor ground connection should not share a power path. Kelvin connection to IC−GND is recommended.

ROSC resistance value will have no influence on f_{SW} below 410 kHz. ROSC and f_{ROSC} may be calculated for a frequency range of 410 kHz (46 k**Ω**) to 512 kHz (9.01 k**Ω**) with the following expression.

$$R_{OSC} = \frac{a + b \cdot f_{ROSC}}{1 + c \cdot f_{ROSC} + d \cdot f_{ROSC}^{\,2}} k\Omega \quad \text{(eq. 4)}$$

where

a = 2.7144E4
b = 1.3422E2
c = −6.2272E1
d = 1.6262E−1
f_{ROSC} expressed in kHz

$$f_{ROSC} = 410 \cdot \left[A + \frac{B}{1 + \left(\frac{ROSC}{C}\right)^{D}} \right] kHz \quad \text{(eq. 5)}$$

where

A = 0.93976
B = 3.6294
C = 0.93511
D = 1.04638
ROSC expressed in kΩ

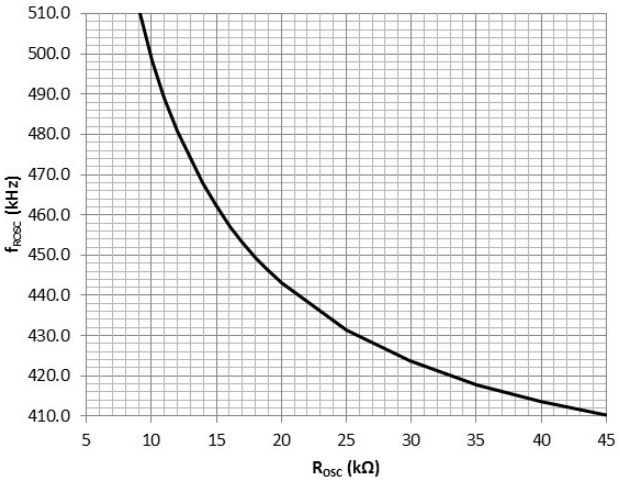


Figure 32. f_{ROSC} vs ROSC

Spread Spectrum

In SMPS devices, switching translates to higher efficiency. As a consequence, the switching also leads to a higher EMI profile. We can greatly reduce some of the peak radiated emissions with some spread spectrum techniques. Spread spectrum is a method used to reduce the peak electromagnetic emissions of a switching regulator.

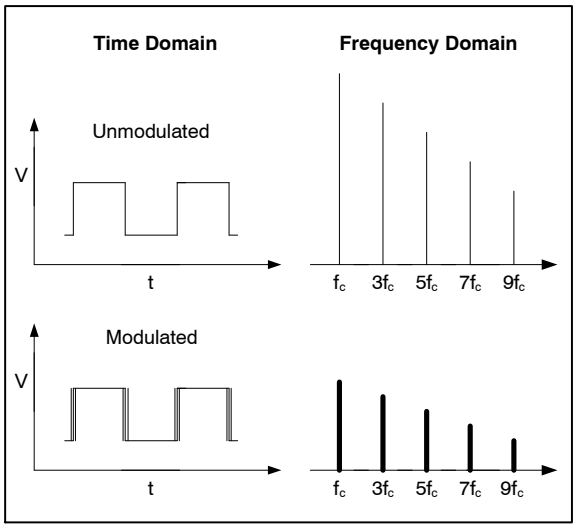


Figure 33. Spread Spectrum Comparison

The NCV881930 has spread spectrum functionality for reduced peak radiated emissions. This IC uses a pseudo−random generator to set the oscillator frequency to one of 8 discrete frequency bins. Each digital bin represents a shift in frequency by 8.2 kHz over the range 410 kHz to 467 kHz. Over time, each bin is used an equal number of times to ensure an even spread of the spectrum. This reduces the peak energy at the fundamental 410 kHz frequency, and spreads it into a wider band.

Table 9. PSEUDO−RANDOM FREQUENCY BINS

14% Pseudo Random Bin #	Switching Frequency
0	410 kHz
1	418 kHz
2	426 kHz
3	435 kHz
4	443 kHz
5	451 kHz
6	459 kHz
7	467 kHz

The period of each cycle will change inversely to the switching frequency but the duty cycle, however, will remain constant.

Thermal Shutdown

A thermal shutdown circuit inhibits switching and resets the soft−start circuit if internal temperature exceeds a safe level indicated by the thermal shutdown activation temperature (T_{SD}). Switching is automatically restored when temperature returns to a safe level based on the thermal shutdown hysteresis ($T_{SD,HYS}$).

Efficiency

During the brief time duration when both high−side and low−side transistors are turned−off, free−wheeling current flows through the low−side transistor's intrinsic body diode. An optional Schottky diode across the low−side transistor may be used for an incremental efficiency improvement.

Efficiency curves for NCV881930 5 V demo board (VCCEXT = VOUT) are shown in Figure 34.

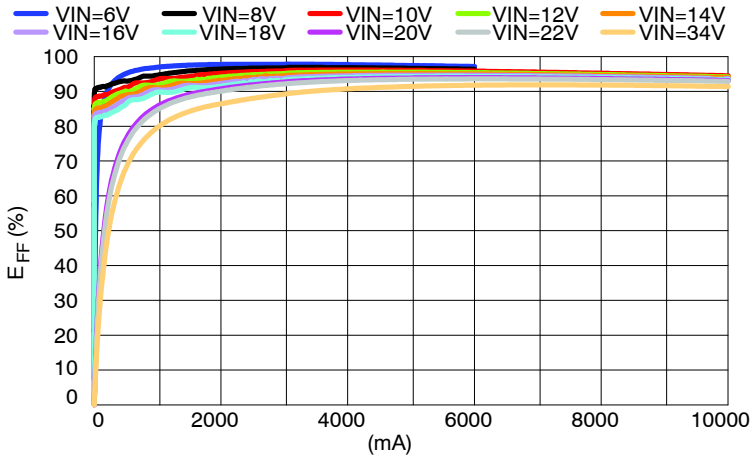


Figure 34. Efficiency vs Load Current (5 V Demo Board, SYNCI = 0 V)

Exposed Pad

The EPAD must be electrically connected to both the analog and the power electrical ground GND and PGND pins on the PCB for proper, noise−free operation. It is recommended to connect these two pins directly to the EPAD with a PCB trace. Recommended layout information may be found on the web accessible demo board information.

APPLICATIONS INFORMATION

Design Methodology

Choosing external components encompasses the following design process:

1. Operational parameter definition
2. Switching frequency selection (ROSC)
3. Output inductor selection
4. Current sense resistor selection
5. Output capacitor selection
6. Input capacitor selection
7. Thermal considerations

(1) Operational Parameter Definition

Before proceeding with the rest of the design, certain operational parameters must be defined. These are application dependent and include the following:

V_{IN}: input voltage, range from minimum to maximum with a typical value [V]
V_{OUT}: output voltage [V]
I_{OUT}: output current, range from minimum to maximum with initial start−up value [A]
I_{CL}: desired typical current limit [A]

A number of basic calculations must be performed up−front to use in the design process, as follows:

$$D_{MIN} = \frac{V_{OUT}}{V_{IN(MAX)}} \quad \text{(eq. 6)}$$

$$D = \frac{V_{OUT}}{V_{IN(typ)}} \quad \text{(eq. 7)}$$

$$D_{MAX} = \frac{V_{OUT}}{V_{IN(MIN)}} \quad \text{(eq. 8)}$$

where: D_{MIN}: minimum duty cycle (ideal) [%]
$V_{IN(MAX)}$: maximum input voltage [V]
D: typical duty cycle (ideal) [%]
$V_{IN(TYP)}$: typical input voltage [V]
D_{MAX}: maximum duty cycle (ideal) [%]
$V_{IN(MAX)}$: minimum input voltage [V]

These are ideal duty cycle expressions; actual duty cycles will be marginally higher than these values. Actual duty cycles are dependent on load due to voltage drops in the MOSFETs, inductor and current sense resistor.

(2) Switching Frequency Selection (ROSC)

Selecting the switching frequency is a trade−off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values to achieve the same inductor current ripple and output voltage ripple. However, increasing the frequency increases the switching losses of the MOSFETs, leading to decreased efficiency, especially noticeable at light loads.

Typically, the switching frequency is selected to avoid interfering with signals of known frequencies. Often, in this case, the frequency can be programmed to a lower value with ROSC and then a higher−frequency signal can be applied to the SYNC pin to increase the frequency dynamically to avoid given frequencies. A spread spectrum signal could also be used for the SYNC input, as long as the lowest frequency in the range is above the programmed frequency set by ROSC. Additionally, the highest SYNC frequency must not exceed maximum switching frequency limits.

There are two limits on the maximum allowable switching frequency: minimum off−time and minimum on−time. These set two different maximum switching frequencies, as follows:

$$f_{S(MAX)1} = \frac{1 - D_{MAX}}{T_{MinOff}} \quad \text{(eq. 9)}$$

$$f_{S(MAX)2} = \frac{1 - D_{MIN}}{T_{MinOn}} \quad \text{(eq. 10)}$$

where: $f_{S(MAX)1}$: maximum switching frequency due to minimum off−time [Hz]
T_{MinOff}: minimum off−time [s]
$f_{S(MAX)2}$: maximum switching frequency due to minimum on−time [Hz]
T_{MinOn}: minimum on−time [s]

Alternatively, the minimum and maximum operational input voltage can be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1 - T_{MinOff} \cdot f_S} \quad \text{(eq. 11)}$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{T_{MinOn} \cdot f_S} \quad \text{(eq. 12)}$$

where: f_S: switching frequency [Hz]

The switching frequency is programmed by selecting the resistor connected between the ROSC pin and ground. The grounded side of this resistor should be directly connected to the GND pin. Avoid running any noisy signals beneath the resistor, as injected noise could cause frequency jitter. The graph in Figure 49 shows the required resistance to program the frequency.

(3) Output Inductor Selection

Both mechanical and electrical considerations influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the power supply, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, an inductor is chosen for a set amount of ripple current and to assure adequate transient response.

Larger inductor values limit the switcher's ability to slew current through the output inductor in response to output load transients, impacting incremental dynamic response. While the inductor is slewing current during this time, output capacitors must supply the load current. Therefore, decreasing the inductance allows for less output capacitance to hold the output voltage up during a load transient.

A ripple current δI_L equaling 20−40% of the output rated current is a typical objective when selecting an inductor value for a duty ratio D normally selected at the nominal input operating voltage. The inductor value may be calculated using the following expression:

$$L = \frac{V_{OUT} \cdot (1 - D)}{\delta I_L \cdot f_S} \quad \text{(eq. 13)}$$

Inductor saturation current is specified by inductor manufacturers as the current at which the inductance value has dropped a certain percentage from the nominal value, typically 10−30%. It is recommended to choose an inductor with saturation current sufficiently higher than the peak output current, such that the inductance is very close to the nominal value at the peak output current. This introduces a safety factor and allows for more optimized compensation.

Inductor efficiency is another consideration when selecting an output inductor. Inductor losses include DC and AC winding losses as well as core losses. Core losses are proportional to the amplitude of the ripple current and operating frequency.

AC winding losses are based on the AC resistance of the winding and the RMS ripple current through the inductor, which is much lower than the DC current. AC winding losses are due to skin and proximity effects and are typically much less than the DC losses, but increase with frequency. The DC winding losses in the inductor can be calculated with the following equation:

$$P_{L(DC)} = I_{OUT}^2 \cdot R_{DC} \quad \text{(eq. 14)}$$

where: $P_{L(DC)}$: DC winding losses in the output inductor
R_{DC}: DC resistance of the output inductor (DCR)

(4) Current Sense Resistor Selection

Current sensing for peak current mode control relies on the amplitude of the inductor current. The current is translated into a voltage via a current sense resistor placed in series with the output inductor located between the output inductor and capacitors. The resulting voltage is then measured differentially by a current sense amplifier, generating a single−ended output to use as a control signal. If a current sense π−filter is implemented as in Figure , the following expression may be used to determine the current sense resistor value.

$$R_i = \frac{V_{PCL,N} + R_{SF2} \cdot I_{CSN}}{I_{L(PK)} \cdot \kappa} \quad \text{(eq. 15)}$$

where: $V_{PCL,N}$: positive current limit threshold voltage [V]
R_{SF2}: π−filter CSN−V_{OUT} resistor [Ω] (set value in expression to 0 Ω if there is no filter)
$I_{L(PK)}$: peak inductor current at rated output current [A]
κ : design margin to account for inductor variation as well as extra current required to support load transient response. A value of ~120% is commonly used [%].

Alternative current measurement methods such as lossless inductor current sensing may be feasible but beyond the scope of this document.

(5) Output Capacitor Selection

When used in conjuncture with ceramic capacitors, aluminum polymer/hybrid bulk capacitors are recommended instead of aluminum electrolytic capacitors due to their low −40°C/25°C ESR ratio. Use of EMI bulk capacitors having a high −40°C/25°C ESR ratio may result in an ineffective output filter along with potential stability issues under cold temperature operating conditions.

The output capacitor is a basic component for the fast response of the power supply. During the first few microseconds following a load step, it supplies the incremental load current. The controller immediately recognizes the load step and increases the duty cycle, but the current slew rate is limited by the inductor. During a load release, the output voltage will overshoot. The capacitance will decrease this undesirable response, decreasing the amount of voltage overshoot.

The worst case is when initial current is at the current limit and the initial voltage is at the output voltage set point, calculating. The overshoot is:

$$\delta V_{OS(MAX)} = \sqrt{\frac{L}{C} \cdot I_{CL}^2 + V_{OUT}^2} - V_{OUT} \quad \text{(eq. 16)}$$

Accordingly, a minimum amount of capacitance can be chosen for a maximum allowed output voltage overshoot:

$$C_{min} = \frac{L \cdot I_{CL}^2}{\delta V_{OS(MAX)} \cdot \left(2 \cdot V_{OUT} + \delta V_{OS(MAX)}\right)} \quad \text{(eq. 17)}$$

where: C_{MIN}: minimum amount of capacitance to minimize voltage overshoot to $\delta V_{OS(MAX)}$ [F]
$\delta V_{OS(MAX)}$: maximum allowed voltage overshoot during a load release to 0 A [V]

A maximum amount of capacitance can be found based on the output inductor overshoot current and current limit. To calculate the output inductor startup overshoot current, the following approximation may be used (inductor ripple current not considered):

$$I_{L(OS)} = \frac{C_{OUT} \cdot V_{OUT}}{t_{ss}} + I_{OUT(i)} \quad \text{(eq. 18)}$$

where: $I_{L(OS)}$: Output inductor overshoot current during startup [A]
$I_{OUT(i)}$: Output current during startup [A]

During soft−start, the inductor current must provide current to the load as well as current to charge the output capacitor. The current limit defines the maximum current which the inductor is allowed to conduct. Setting the inrush current to the current limit places a limit on the maximum capacitor size as follows:

$$C_{MAX} = \frac{\left(I_{CL} - I_{OUT}\right) \cdot t_{ss}}{V_{OUT}} \quad \text{(eq. 19)}$$

where: C_{MAX}: maximum output capacitance [F]

Capacitors should also be chosen to provide acceptable output voltage ripple with a DC load, in addition to limiting voltage overshoot during a dynamic response. Key specifications are equivalent series resistance (ESR) and equivalent series inductance (ESL). The output capacitors must have very low ESL for best transient response. The PCB traces will add to the ESL, but by positioning the output capacitors close to the load, this effect can be minimized and ESL neglected when determining output voltage ripple.

The total peak−to−peak ripple δV_{OUT} is defined as:

$$\delta V_{OUT} = \delta I_L \cdot \left(\frac{1}{8 \cdot C \cdot f_{SW}} + r_{ESR} \right) \quad \text{(eq. 20)}$$

Where: δV_{OUT}: total output voltage ripple due to output capacitance and its ESR [V_{pp}]
r_{ESR}: output capacitor ESR [Ω]

Capacitor ESR corresponding to the operating frequency f_s must be used. The steady−state power lost from the capacitor ESR may be calculated as follows:

$$P_{C(ESR)} = \frac{1}{3} \cdot \delta I_L{}^2 \cdot r_{ESR} \quad \text{(eq. 21)}$$

(6) Input Capacitor Selection

The input EMI capacitors must sustain the ripple current produced during the on time of the high−side MOSFET and must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$I_{IN(RMS)} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)} \quad \text{(eq. 22)}$$

where: $I_{IN(RMS)}$ = input RMS current [A]

The peak harmonic current will be at the switching frequency. The above equation reaches its maximum value with D = 0.5, $I_{IN(RMS)} = I_{OUT}/2$. The input capacitors must be rated to handle the RMS ripple current.

Input capacitor RMS current losses may be calculated with the following equation:

$$P_{CIN} = I_{IN(RMS)}{}^2 \cdot R_{ESR(CIN)} \quad \text{(eq. 23)}$$

where: P_{CIN} = power loss from the input capacitors
$R_{ESR(CIN)}$ = effective series resistance of the input capacitance

Due to large current transients through the input capacitors, electrolytic, polymer or ceramics should be used. Aluminum electrolytic specifications often require closer scrutiny due to poor ESR cold temperature characteristics. As a result of the large ripple current, it is common to place ceramic capacitors in parallel with the bulk electrolytic/polymer input capacitors to reduce switching voltage ripple. A value of 0.01 μF to 0.1 μF placed near the MOSFETs is also recommended.

Output impedance magnitude of the EMI filter $Z_{outFILTER}(f)$ must be much smaller than input impedance magnitude of the filtered converter $Z_{inSMPS}(f)$.

$$|Z_{outFILTER}(f)| << |Z_{inSMPS}(f)| \quad \text{(eq. 24)}$$

Analysis of these impedances may require complex calculations or simulations. For simple LC input EMI filters, a good first order approximation for evaluating the inequality may be obtained with the use of the following approximation:

$$Z_{outFILTER} \approx \sqrt{\frac{L_{EMI}}{C_{EMI}}} \quad \text{(eq. 25)}$$

$$Z_{inSMPS} \approx \frac{V_{IN}{}^2 \cdot \eta}{P_{OUT}} \quad \text{(eq. 26)}$$

where: η = power supply efficiency [%]

(7) Thermal Considerations

This controller is intended to be used in applications where currents of above 10 A may exist. The following should be considered for best performance.

- Use of 2 oz (70 micron) copper for the high current handling layers.
- 4 layer (or more) boards are best suited to facilitate thermal management of lossy devices (output inductor, MOSFETs, IC)
  - High frequency layout methods dictate that the controller will be placed near the synchronous MOSFET switches. Inadequate thermal management of the power dissipating devices will result in significant localized PCB temperature rise from thermal coupling between devices and case−ambient thermal resistances. Resulting IC (and MOSFET) case temperatures may become significantly higher than ambient temperature.

Maximizing thermal dissipation surface area beneath the IC along with liberal use of thermal vias is recommended.

Table 10. ORDERING INFORMATION

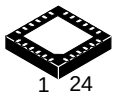
Device	Status	Output Voltage	Marking	Package	Shipping†
NCV881930MW00R2G	Not Recommended for New Designs	3.3 V/5.0 V	V8819 3000	QFN24 (Pb−Free)	4000 / Tape & Reel
NCV881930MW00AR2G	Recommended	3.3 V/5.0 V	8819A 3000	QFN24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: The NCV881930 will not offer the alternate construction leadframe version illustrated in Detail A and Detail B in the Package Dimensions.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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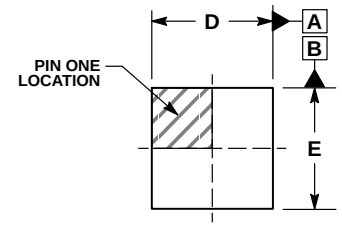
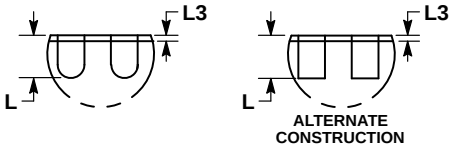
QFNW24 4x4, 0.5P
CASE 484AE
ISSUE A

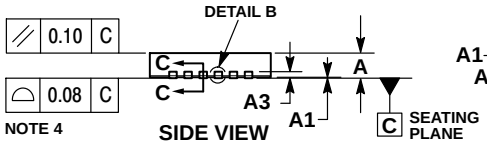
DATE 07 AUG 2018



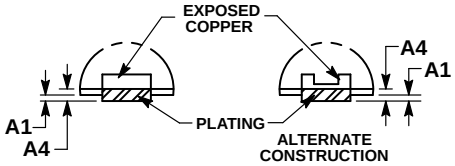
TOP VIEW



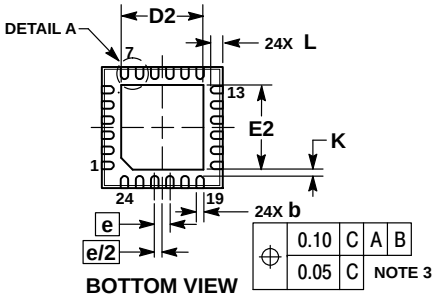
DETAIL A



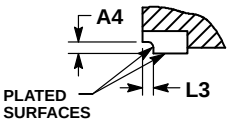
SIDE VIEW



DETAIL B



BOTTOM VIEW



SECTION C−C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	–––	–––	0.05
A3		0.20 REF	
A4	0.10	–––	–––
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e		0.50 BSC	
K	0.20	–––	–––
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

GENERIC MARKING DIAGRAM*

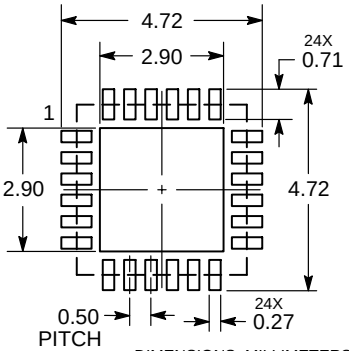


XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**QFNW24 4x4, 0.5P**		**PAGE 1 OF 1**

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