NCS36000

Passive Infrared (PIR) Detector Controller

The NCS36000 is a fully integrated mixed−signal CMOS device designed for low−cost passive infrared controlling applications. The device integrates two low−noise amplifiers and a LDO regulator to drive the sensor. The output of the amplifiers goes to a window comparator that uses internal voltage references from the regulator. The digital control circuit processes the output from the window comparator and provides the output to the OUT and LED pin.

Features

- 3.0 − 5.75 V Operation
- −40 to 85°C
- 14 Pin SOIC Package
- Integrated 2−Stage Amplifier
- Internal LDO to Drive Sensor
- Internal Oscillator with External RC
- Single or Dual Pulse Detection
- Direct Drive of LED and OUT
- This is a Pb−Free Device

Typical Applications

- Automatic Lighting (Residential and Commercial)
- Automation of Doors
- Motion Triggered Events (Animal photography)

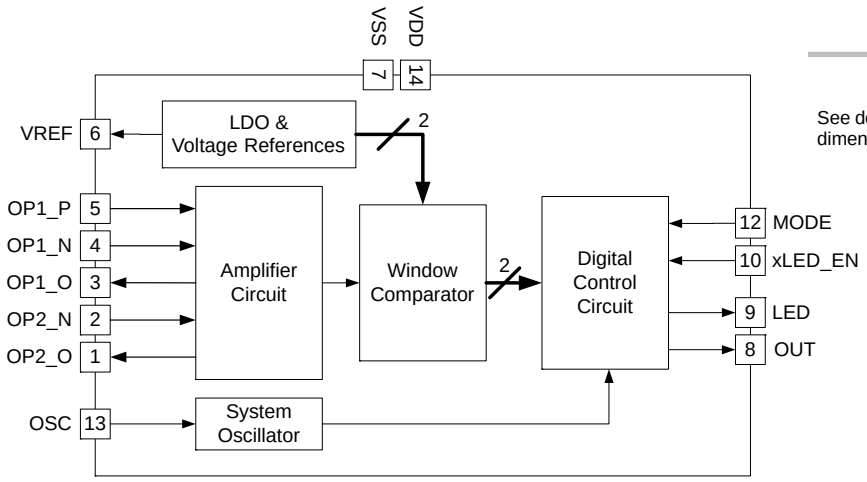

Figure 1. Simplified Block Diagram

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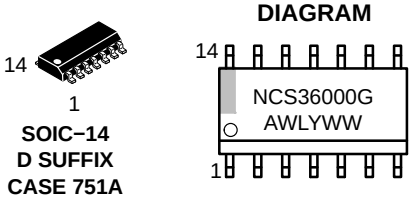
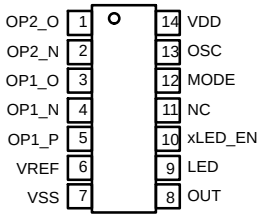
MARKING DIAGRAM



SOIC−14
D SUFFIX
CASE 751A

A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OP2_O	Output of second amplifier
2	OP2_N	Inverting input of second amplifier
3	OP1_O	Output of first amplifier
4	OP1_N	Inverting input of first amplifier
5	OP1_P	Non−inverting input of first amplifier
6	VREF	Regulated voltage reference to drive sensor
7	VSS	Analog ground reference.
8	OUT	CMOS output (10 mA Max)
9	LED	CMOS output to drive LED (10mA Max)
10	xLED_EN	Active low LED enable input
11	NC	No Connect
12	MODE	Pin used to select pulse count mode
13	OSC	External oscillator to control clock frequency
14	VDD	Analog power supply

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{in}	−0.3 to 6.0	V
Output Voltage Range	V_{out}	−0.3 to 6.0 V or (V_{in} + 0.3), whichever is lower	V
Maximum Junction Temperature	$T_{J(max)}$	140	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, DFN6, 3x3.3 mm (Note 4) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Lead2 (Note 5)	 $R_{\theta JA}$ $R_{\Psi JL}$	Will be Completed once package and power consumption is finalized	°C/W
Thermal Characteristics, TSOP−5 (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	 $R_{\theta JA}$	 See note above.	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 6)

Rating		Symbol	Min	Typ	Max	Unit
Analog Power Supply		V_{DD}	3.0	5.0	5.75	V
Analog Ground Reference		V_{SS}		0.0	0.1	V
Supply Current (Standby, No Loads)		I_{DD}			170µ	A
Digital Inputs (MODE)		V_{ih}	0.7 * V_{DD}	V_{DD}	V_{DD} + 0.3	V
		V_{il}	VSS		V_{DD} * 0.28	
Digital Output (OUT, LED)	Push−Pull Output (10 mA Load)	V_{oh}	0.67 * V_{DD}		V_{DD}	V
		V_{ol}	VSS		V_{DD} * 0.3	
OP1_P (Sensor Input) (Note 7)		AMP 1 IN	0.1		V_{DD} − 1.1	V
Ambient Temperature		T_A	−40		85	°C

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
7. Guaranteed By Design (Non−tested parameter).

ELECTRICAL CHARACTERISTICS V_{in} = 1 V, C_{in} = 100 nF, C_{out} = 100 nF, for typical values T_A = 25°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LDO Voltage Reference						
Output Voltage	V_{DD} = 3.0 V to 5.75 V	VREF	2.6	2.7	2.8	V
Supply Current	V_{DD} = 3.0 V to 5.75V	IREF		20	50	µA
Comparator High Trip Level		V_h	2.413	2.5	2.588	V
Comparator Low Trip Level		V_l	1.641	1.7	1.760	V
Reference voltage for non−inverting input of second amplifier		V_m	2.007	2.1	2.174	V
System Oscillator						
Oscillator Frequency	V_{DD} = 5.0 V R_3 = 220 kΩ C_2 = 100 nF	OSC		62.5		Hz
Window Comparator						
Lower Trip Threshold	See Vl above					
Higher Trip Threshold	See Vh above					
Differential Amplifiers (Amplifier Circuit)						
DC Gain	V_{DD} = 5.0 V (Note 8)	Av	80			dB
Common−mode Input Range	V_{DD} = 5.0 V (Note 8)	CMIR	0.1		V_{DD} − 1.1	V
Power Supply Rejection Ratio	V_{DD} = 5.0 V (Note 8)	PSRR		60		dB
Output Drive Current	V_{DD} = 5.0 V (Note 8)	I_{out1}			25	µA
POR						
POR Release Voltage		V_{POR}	1.35		2.85	V

8. Guaranteed By Design (Non−tested parameter).

APPLICATIONS INFORMATION

Oscillator

The oscillator uses an external resistor and capacitor to set the system clock frequency. Multiple clock frequencies can be selected using different combinations of resistors and capacitors. Figure 2 shows a simplifier block diagram for the system oscillator.

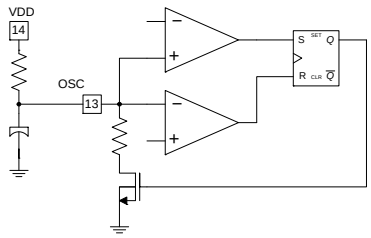


Figure 2. Block Diagram of System Oscillator Circuit

LDO Regulator

The LDO regulator provides the reference voltage for the sensor and all other analog blocks within the system. The nominal voltage reference for the sensor is 2.7 V ±5%. An external capacitor is needed on the VREF pin to guarantee stability of the regulator.

Differential Amplifiers

The two differential amplifiers can be configured as a bandpass filter to condition the PIR sensor signal for the post digital signal processing. The cutoff frequencies and passband gain are set by the external components. See Figure 5.

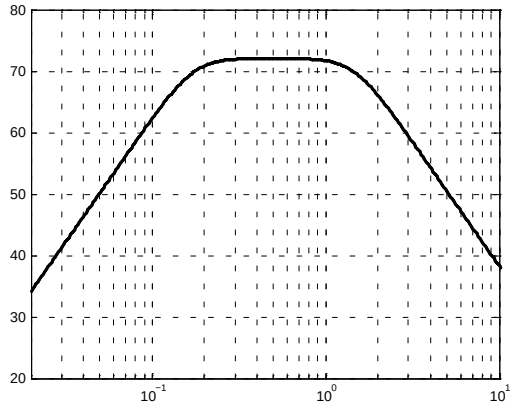


Figure 3. Plot Showing Typical Magnitude Response of Differential Amplifiers When Configured as a Bandpass Filter

Window Comparator

The window comparator compares the voltage from the second differential amplifier to two reference voltages from the LDO regulator. COMP_P triggers if OP2_O is greater than the Vh voltage and COMP_N triggers if OP2_O is lower than the Vl voltage. See Figures 4 and 5.

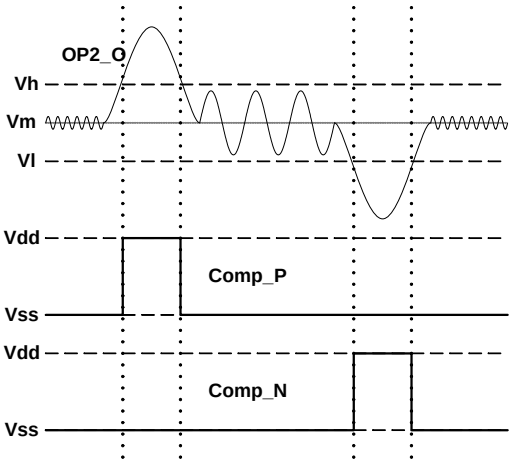


Figure 4. Plot Showing Functionality of Window Comparator for an Analog Input OP2_O

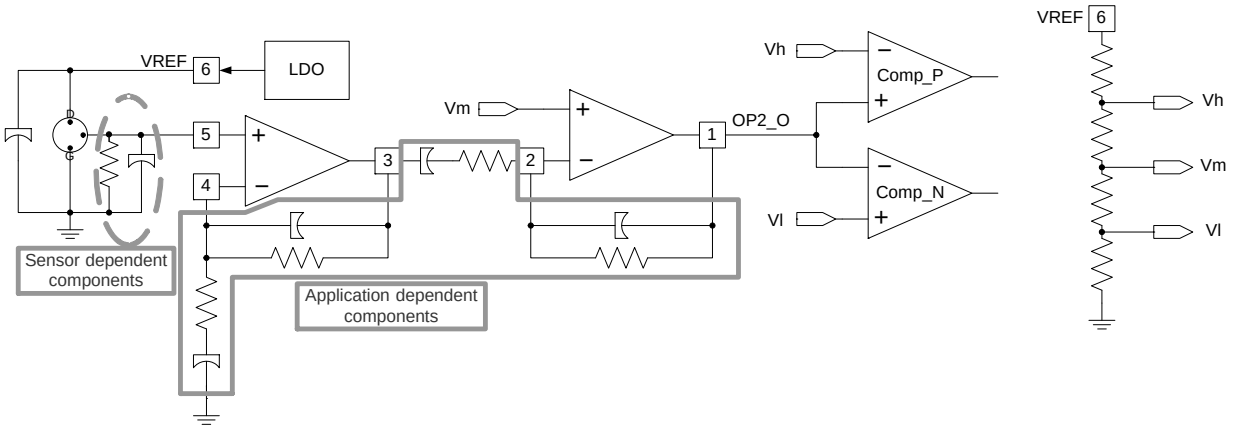


Figure 5. Figure Showing Simplified Block Diagram of Analog Conditioning Stages

Digital Signal Processing Block (all times assume a 62.5 Hz system oscillator frequency)

The digital signaling processing block performs three major functions.

The first function is that the device toggles LED during the start−up sequencing at approximately two hertz regardless of the state of the XLED_EN pin. The startup sequence lasts for thirty seconds. During that time the OUT pin is held low regardless of the state of OP2_O.

The second function of the digital signal processing block is to insure a certain glitch width is seen before OUT is toggled. The digital signal processing block is synchronous with the system oscillator frequency and therefore the deglitch time is related to when the comparators toggle within the oscillator period. A signal width less than two clock period is guaranteed to be deglitched as a zero. A signal width of greater than three clock cycles is guaranteed to be de−glitched. It should be noted that down−sampling can occur if sufficient anti−aliasing is not performed at the input of the circuit (OPI_P) or if noise is injected into the amplifiers, an example would be a noisy power supply.

The third function of the digital signal processing block is to recognize different pulse signatures coming from the window comparator block. The device is equipped with two pulse recognition routines. Single pulse mode (MODE tied to VSS) will trigger the OUT pin if either comparator toggles and the deglitch time is of the appropriate length. (See Figure 6). Dual pulse mode (MODE tied to V_{DD}) requires two pulses with each pulse coming from the opposite comparator to occur within a timeout window of five seconds or 312 clock cycles (See Figure 7). If the adjacent pulses occur outside the timeout window then the digital processing block will restart the pulse recognition routine.

xLED_EN Pin

The xLED_EN pin enables the LED output driver when motion has been detected. If xLED_EN is tied high the LED pin will not toggle after motion is detected. If the xLED_EN is tied low the LED pin will toggle when motion is detected. During start-up the LED pin will toggle irrespective of how the xLED_EN pin is tied. (See Figure 6).

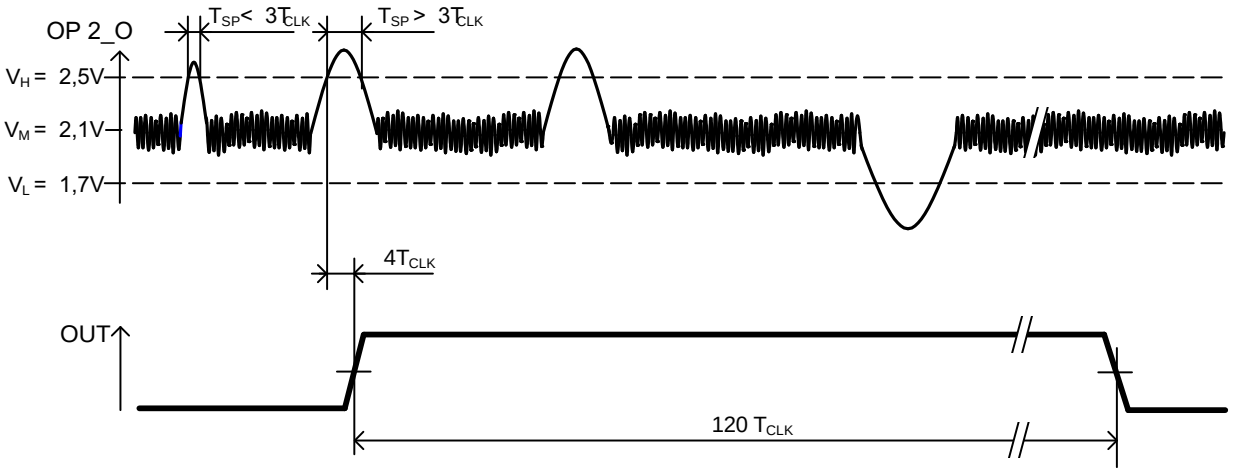


Figure 6. Timing Diagram for Single−Pulse Mode Detection

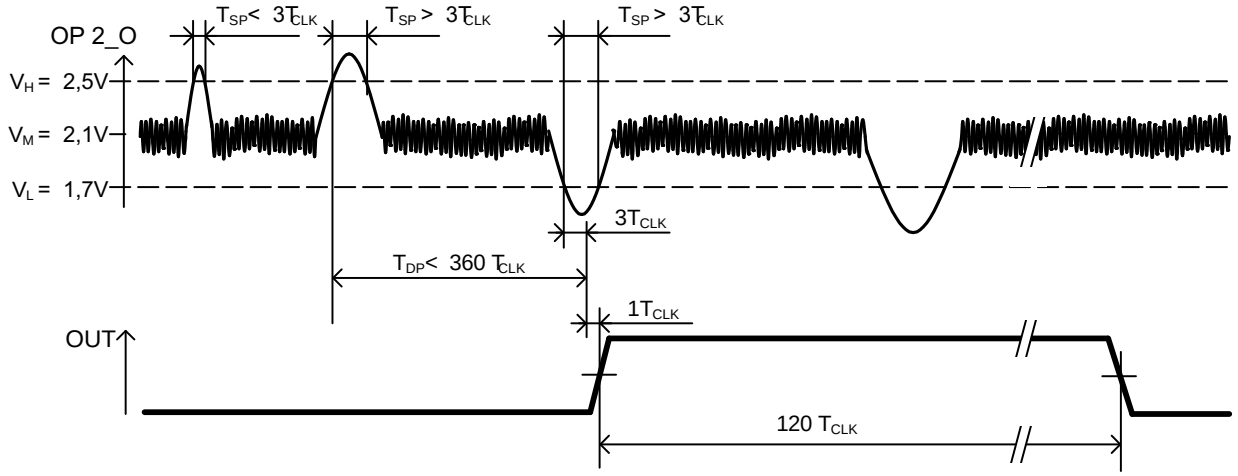


Figure 7. Timing Diagram for Dual−Pulse Mode Detection

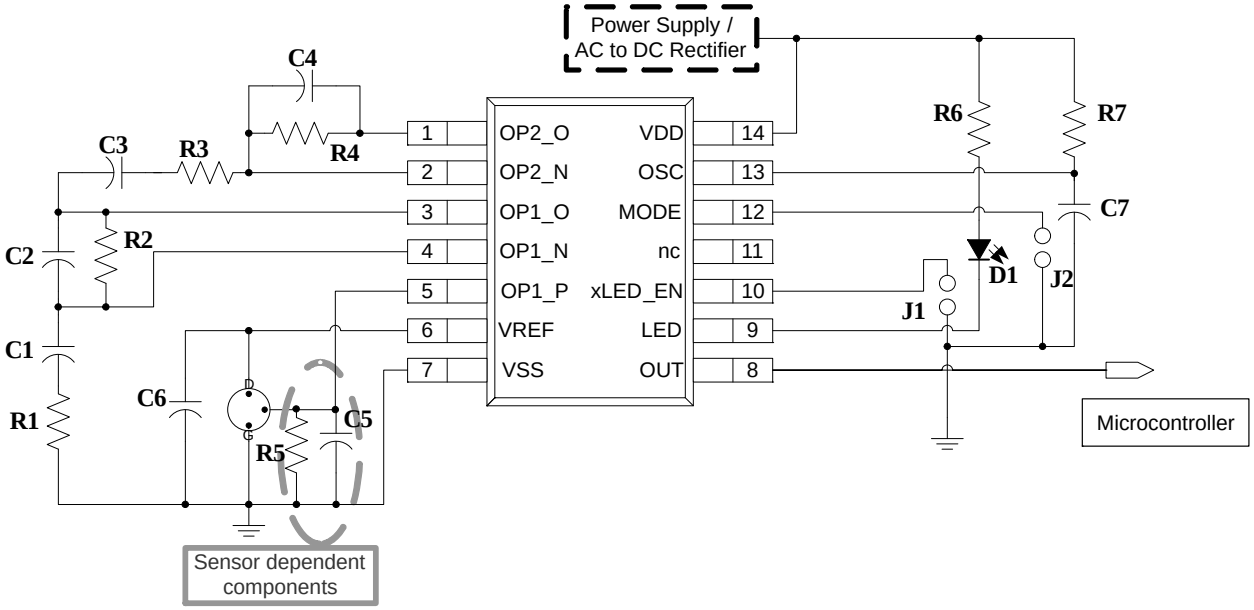


Figure 8. Typical Application Diagram Using NCS36000

R1 = 10 kΩ	C1 = 33 μF	J1 (Jumper for xLED_EN)
R2 = 560 kΩ	C2 = 10 nF	J2 (Jumper for Mode Select)
R3 = 10 kΩ	C3 = 33 μF	D1 (LED)
R4 = 560 kΩ	C4 = 10 nF	
R5 = 43 kΩ	C5 = 100 nF	
R6 = 1 kΩ	C6 = 100 nF	
R7 = 220 kΩ	C7 = 100 nF	

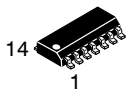
9. R1, C1, R2, C2, R3, C3, R4, C4 setup bandpass filter characteristics. With components as shown above the passband gain is approximately 70 dB with the 3 dB cutoff frequency of the filter at approximately 700 mHz and 20 Hz.
10. R4 can be replaced by a potentiometer to adjust sensitivity of system. Note dynamically changing R4 will also change the pole location for the second amplifier.
11. R5 and C5 are sensor dependant components and R6 may need to be adjusted to guarantee the AMP 1 IN parameter outlined within the Operating Ranges section of this document.
12. R7 and C7 may be adjusted to change the oscillator frequency. R7 may not be smaller than 50 kΩ.

ORDERING INFORMATION

Device	Package	Shipping†
NCS36000DG	SOIC−14 (Pb−Free)	55 Units / Rail
NCS36000DRG	SOIC−14 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

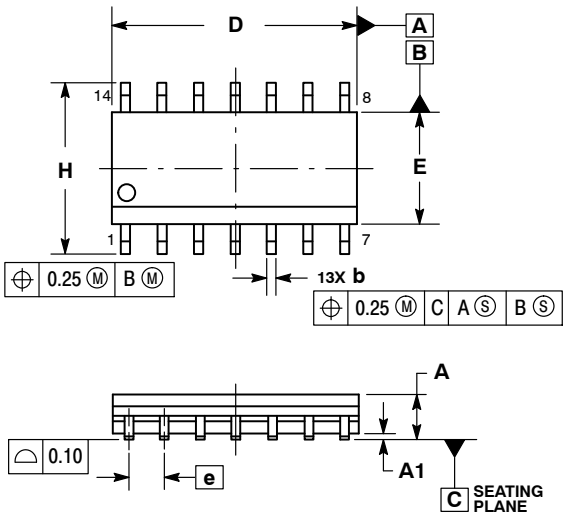
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

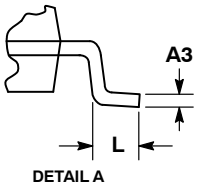


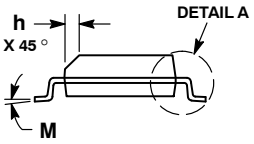
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



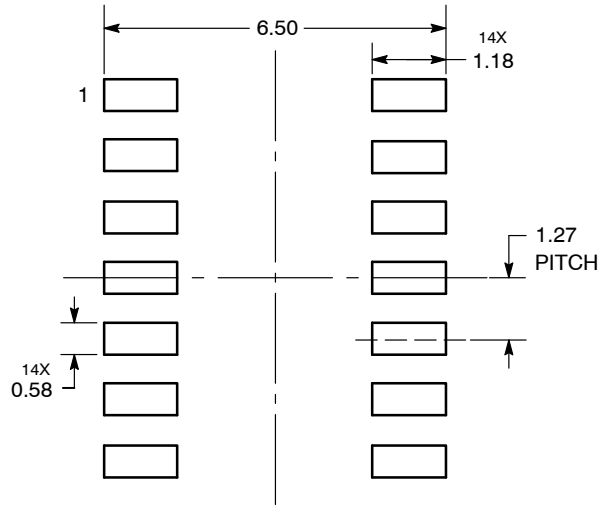




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

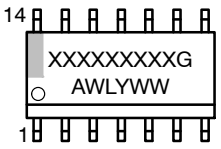
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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