NCP51199, NCV51199

DDR 2-Amp Source / Sink V_{TT} Termination Regulator

The NCP/NCV51199 is a linear regulator designed to supply a regulated V_{TT} termination voltage for DDR−2 and DDR−3 memory applications. The regulator is capable of actively sourcing and sinking ±2 A peak currents for DDR−2, and DDR−3 up to ±1.5 A while regulating the V_{TT} output voltage to within ±10 mV. The output termination voltage is regulated to track V_{DDQ} / 2 by two external voltage divider resistors connected to the PV_{CC}, GND, and V_{REF} pins.

The NCP/NCV51199 incorporates a high−speed differential amplifier to provide ultra−fast response to line and load transients. Other features include source/sink current limiting, soft−start and on−chip thermal shutdown protection.

Features

- Supports DDR−2 V_{TT} Termination to ±2 A, DDR−3 to ±1.5 A (peak)
- Stable with 10 μF Ceramic Capacitance on V_{TT} Output
- Integrated Power MOSFETs
- High Accuracy V_{TT} Output at Full−Load
- Fast Transient Response
- Built−in Soft−Start
- Shutdown for Standby or Suspend Mode
- Integrated Thermal and Current−Limit Protection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- SDRAM Termination Voltage for DDR−2 / DDR−3
- Motherboard, Notebook, and VGA Card Memory Termination
- Set Top Box, Digital TV, Printers

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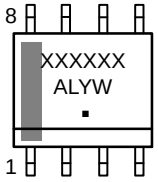
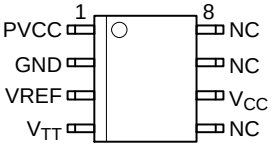
SOIC8−NB EP
PD SUFFIX
CASE 751BU

MARKING DIAGRAM



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

PIN CONNECTION



SOIC−8 EP

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

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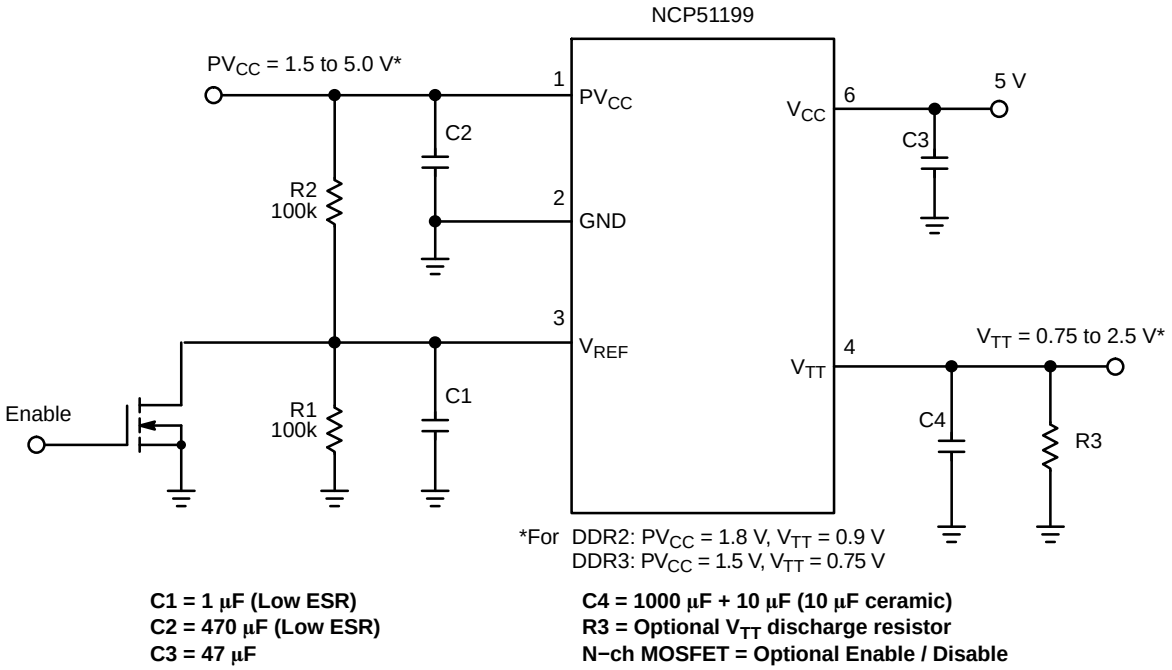

C1 = 1 μF (Low ESR)
C2 = 470 μF (Low ESR)
C3 = 47 μF
C4 = 1000 μF + 10 μF (10 μF ceramic)
R3 = Optional V_{TT} discharge resistor
N−ch MOSFET = Optional Enable / Disable

Figure 1. Application Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	PV_{CC}	Input voltage which supplies current to the output pin. C_{IN} = 470 μF with low ESR.
2	GND	Common Ground
3	V_{REF}	Buffered reference voltage input equal to ½ of V_{DDQ} and active low shutdown pin. An external resistor divider dividing down the PV_{CC} voltage creates the regulated output voltage. Pulling the pin to ground (0.15 V maximum) turns the device off.
4	V_{TT}	Regulator output voltage capable of sourcing and sinking current while regulating the output rail. C_{OUT} = 1000 μF + 10 μF ceramic with low ESR.
5	NC	True No Connect
6	V_{CC}	The V_{CC} pin is a 5 V input pin that provides internal bias to the controller. PV_{CC} should always be kept lower or equal to V_{CC}.
7	NC	True No Connect
8	NC	True No Connect
EP	Thermal Pad	Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Supply Voltage Range ($V_{cc} \geq PV_{CC}$) (Note 1)	PV_{CC}, V_{CC}	−0.3 to 6	V
Output Voltage Range	V_{TT}	−0.3 to 6	V
Reference Input Range	V_{REF}	−0.3 to 6	V
Maximum Junction Temperature	$T_{J(max)}$	125	°C
Storage Temperature Range	TSTG	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESDHBM	2	kV
ESD Capability, Machine Model (Note 2)	ESDMM	150	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SO8−EP (Note 4) Thermal Resistance, Junction−to−Air (Note 5) Power Rating at 25°C Ambient = 1.19 W, derate 12 mW/°C Thermal Reference, Junction−to−Lead2 (Note 5)	 $R_{\theta JA}$ $R_{\Psi JL}$	 84 20	°C/W

4. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 6)

Rating	Symbol	Min	Max	Unit
Input Voltage	PV_{CC}	1.5	5.5	V
Bias Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

ELECTRICAL CHARACTERISTICS

PV_{CC} = 1.8 V / 1.5 V; V_{CC} = 5 V; V_{REF} = 0.9 V / 0.75 V; C_{OUT} = 10 μF (Ceramic); T_A = +25°C, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Offset Voltage	I_{out} = 0 A	V_{OS}	−20	−	+20	mV
Load Regulation	V_{REF} = 900 mV, I_{out} = ±1.8 A, PV_{CC} = 1.8 V V_{REF} = 750 mV, I_{out} = ±1.4 A, PV_{CC} = 1.5 V	Reg_{load}	−10	−	+10	mV
INPUT AND STANDBY CURRENTS						
Bias Supply Current	I_{out} = 0 A	I_{BIAS}	−	0.8	2.5	mA
Standby Current	V_{REF} < 0.2 V (Shutdown), R_{LOAD} = 180Ω	I_{STB}	−	1	90	μA
CURRENT LIMIT PROTECTION						
Current Limit	PV_{CC} = 1.8 V, V_{REF} = 0.9 V	I_{LIM}	2.0	−	3.5	A
	PV_{CC} = 1.5 V, V_{REF} = 0.75 V		1.5	−	3.5	
SHUTDOWN THRESHOLDS						
Shutdown Threshold Voltage	Enable	V_{IH}	0.6	−	−	V
	Shutdown	V_{IL}	−	−	0.15	
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	V_{CC} = 5 V	T_{SD}	160	168	176	°C
Thermal Shutdown Hysteresis	V_{CC} = 5 V	T_{SH}	35	35	40	°C

TYPICAL CHARACTERISTICS

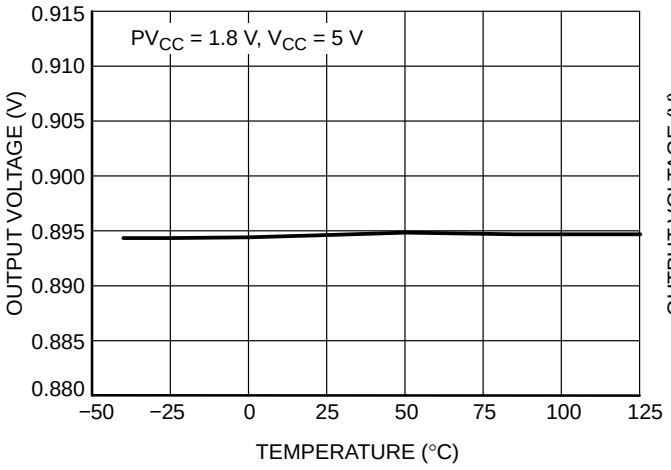

Figure 2. Output Voltage vs. Temperature

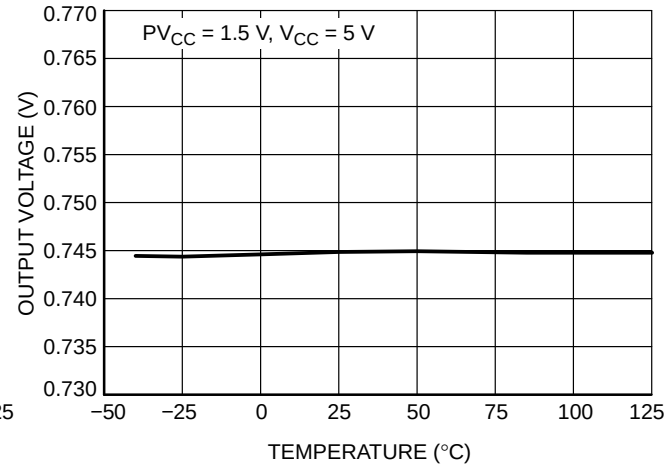

Figure 3. Output Voltage vs. Temperature

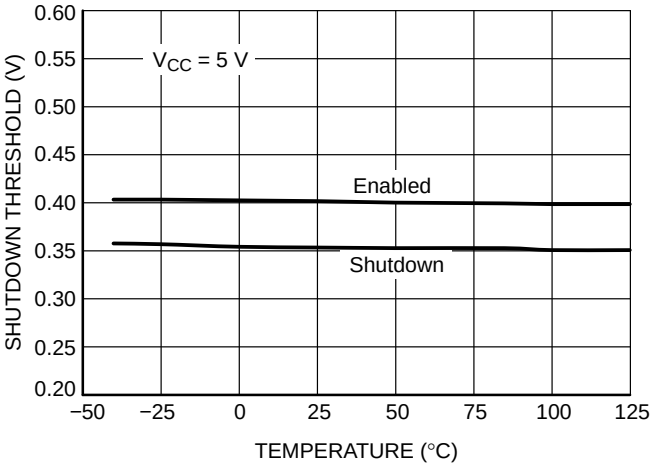

Figure 4. Shutdown Threshold vs. Temperature

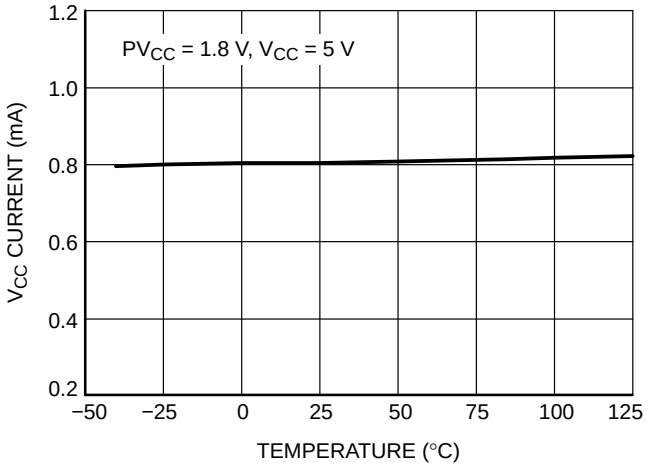

Figure 5. V_{CC} Current vs. Temperature

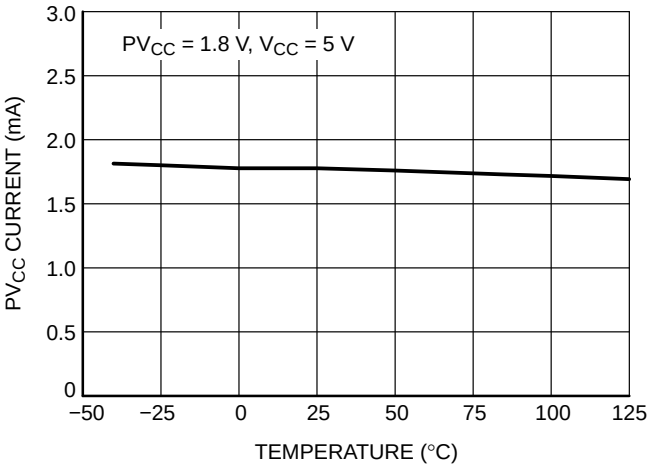

Figure 6. PV_{CC} Current vs. Temperature

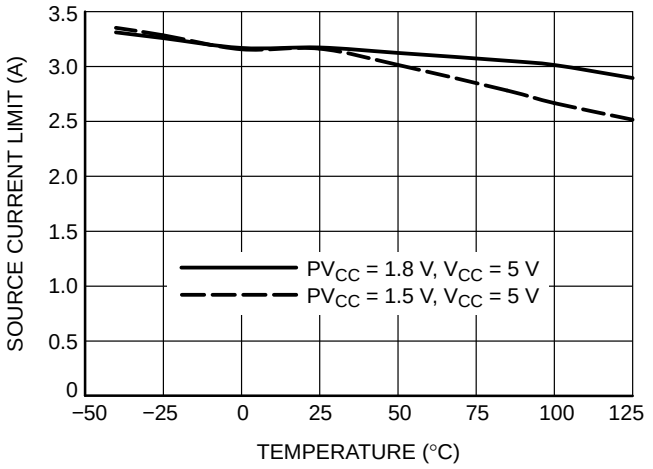

Figure 7. Source Current Limits vs. Temperature

TYPICAL CHARACTERISTICS

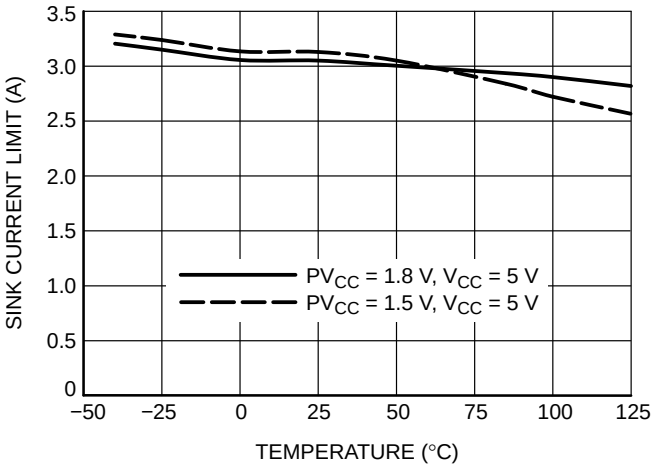

Figure 8. Sink Current Limits vs. Temperature

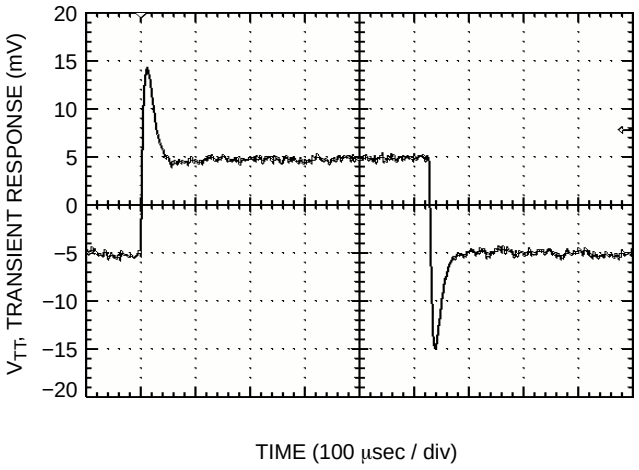

Figure 9. 1.25 V, ±1.6 A Transient Response

Table 1. ORDERING INFORMATION

Device	Marking	Package	Shipping †
NCP51199PDR2G	51199	SOIC−8 (Pb-Free)	2500 / Tape & Reel
NCV51199PDR2G*	V51199		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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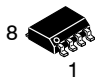
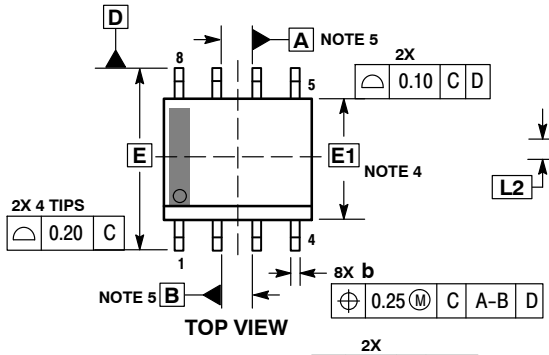


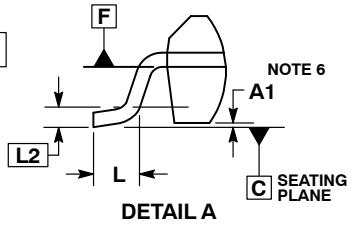
SCALE 1:1

SOIC8−NB EP
CASE 751BU
ISSUE E

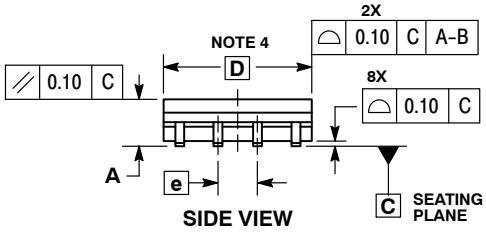
DATE 01 APR 2015



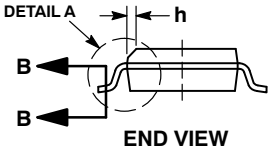
TOP VIEW



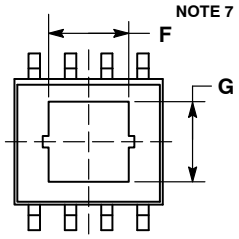
DETAIL A



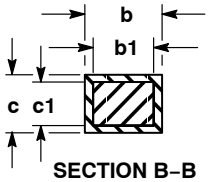
SIDE VIEW



END VIEW



BOTTOM VIEW

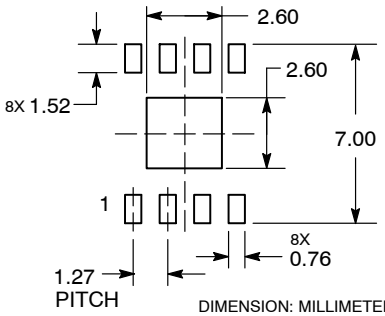


SECTION B−B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. TAB CONTOUR MAY VARY MINIMALLY TO INCLUDE TOOLING FEATURES.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
F	1.55	2.39
G	1.55	2.39
h	0.25	0.50
L	0.40	1.27
L2	0.25 BSC	

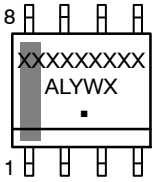
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	**SOIC8−NB EP**		**PAGE 1 OF 1**

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