10 Mb/s Industrial Ethernet MAC + PHY IC Controller

(802.3cg 10BASE−T1S Compliant)

NCN26010

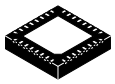
The NCN26010 device is an IEEE 802.3cg compliant Ethernet Transceiver including a Media Access Controller (MAC), a PLCA Reconciliation Sublayer (RS) and a 10BASE−T1S PHY designed for industrial multi−drop Ethernet. It provides all physical layer functions needed to transmit and receive data over a single unshielded twisted pair. NCN26010 communicates to host MCUs via the Open Alliance MACPHY SPI protocol.

Features

- 10BASE−T1S – IEEE 802.3cg Compliant
- 3.3 V Supply Voltage
- Two Configurable Digital Outputs that can Drive Low Current LEDs
- Low Profile 4 mm x 4 mm QFN 32 / TQFP32 (5 mm x 5 mm)
- Integrated MAC and 10BASE−T1S PHY
- Open Alliance Compatible SPI Interface for Exchanging Configuration and Data Frames to Host
- Supports IEEE802.3 CSMA/CD Collision Detection
- Physical Layer Collision Avoidance (PLCA) through Local Configuration for Collision−Free Operation on a Shared Medium (Multi Drop)
- Enhanced Noise Immunity Mode, Allowing Communication at Noise Levels Exceeding IEEE 802.3cg Specifications
- Supports >8 Nodes over >25 m UTP Cable
- Fast Startup: <100 ms
- Support for Bootstrap in Isolated Mode
- These are Pb−Free Devices

Typical Applications

- Industrial Automation
- Sensor Interfacing
- Home / Building Control
- Security and Field Instrumentation



QFN32 4x4, 0.4P
CASE 485GH

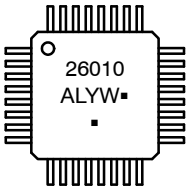


TQFP 32, 5x5
CASE 932AP−01

MARKING DIAGRAM



NCN26010XMNTXG

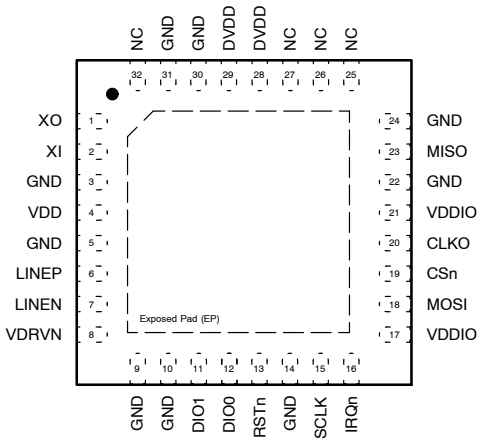


NCN26010XFBR2G

26010	= Specific Device Code
A	= Assembly Site
WL, L	= Wafer Lot Number
Y	= Year of Production
WW	= Work Week Number
YW	= Assembly Start Week
CCCCC	= Country of Origin Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION



4mm x 4mm QFN
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 53 of this data sheet.

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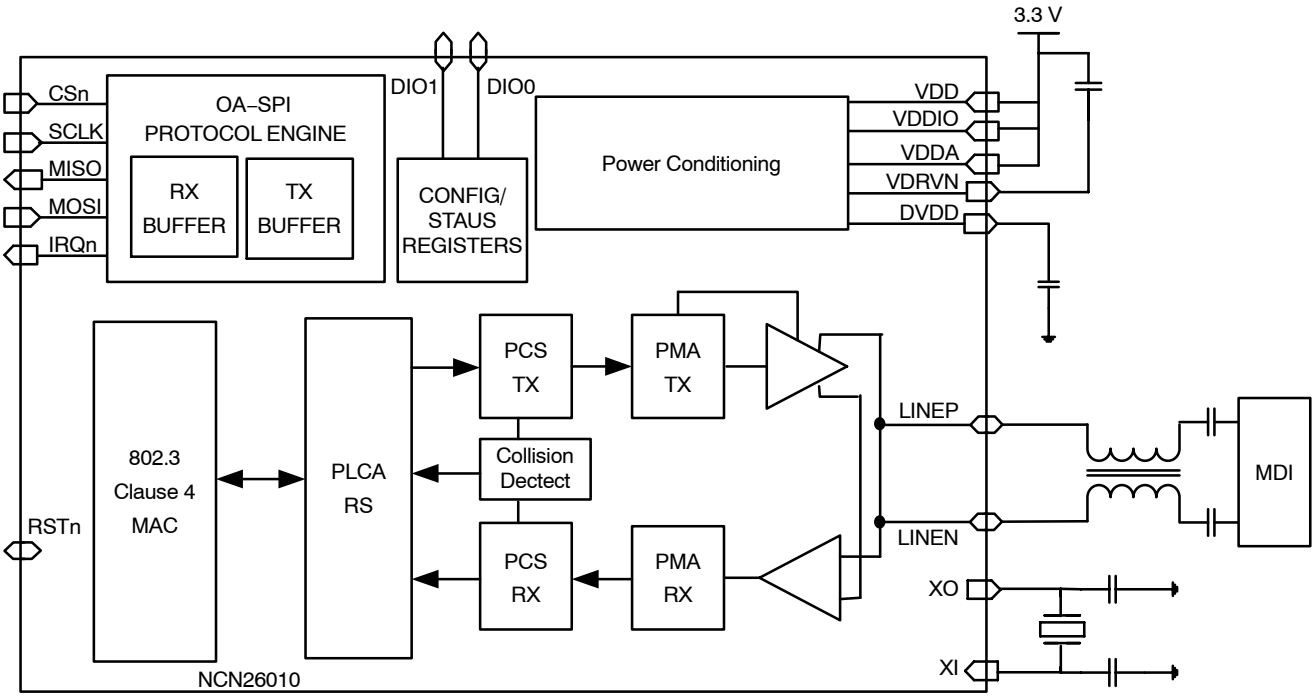


NOTE: Internal power distribution and GND lines from Power Supply block are not shown.

Figure 1. NCN26010 Block Diagram

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Type	Function
1	XO	Output	XTAL	Clock Crystal Connection. If a quartz crystal is used as a clock source, one pin of the crystal is connected to this pin. If an external clock source is used, XO shall be left floating (no connect.)
2	XI	Input	XTAL	System Clock / Crystal Connection. Optionally connected to an external crystal or a 3.3 V LVCMOS reference clock signal.
3	GND	Ground	GND	Analog Ground
4	VDD	Supply	PWR	3.3 V Supply
5	GND	Ground	GND	Ground
6	LINEP	Bi−Directional	Analog	MDI Data Line (Positive)
7	LINEN	Bi−Directional	Analog	MDI Data Line (Negative)
8	VDRVN	Bi−Directional	Analog	TX Driver regulator output Connect to an off−chip 2.2 μF decoupling capacitor
9	GND	Ground	GND	Ground
10	GND	Ground	GND	Ground
11	LED1/DIO1	Output	8X−LVCMOS	General Purpose IO with programmable pull−up/down. This pin can be configured to drive an external LED (through a proper bias resistor) or other circuitry.
12	LED0/DIO0	Output	8X−LVCMOS	General Purpose IO with programmable pull−up/down. This pin can be configured to drive an external LED (through a proper bias resistor) or other circuitry.
13	RSTn	Bi−Directional	8X−Open Drain / Schmitt−Trigger	Active−low asynchronous reset pin. This pin features an internal pull−up of 54 kΩ typical. For noise sensitive applications **onsemi** recommends the use of an external 10 kΩ pull−up resistor to VDDIO. To prevent permanent damage, when driving this from a MCU or any active driver, make sure that such driver is configured as open drain.
14	GND	Ground	GND	Ground
15	SCLK	Input	Schmitt−Trigger	SPI clock input
16	IRQn	Output	4X−Open Drain	Active low Interrupt request, can be configured to trigger on various events
17	VDDIO	Supply	PWR	3.3 V supply for Digital IO, can also be set to 2.5 V to support 2.5 V LVCMOS
18	MOSI	Input	Schmitt−trigger	SPI data input
19	CSn	Input	Schmitt−trigger	Active low Chip Select, selects the device for SPI communication
20	CLKO	Output	4X−LVCMOS	25 MHz clock output. Can provide a clock source for other devices like Micro Controllers or FPGAs on the same PCB. Note that this output is designed to drive a maximum of four LVCMOS input loads. When using this output to drive a 2.5 V I/O, it is recommended to add an external clock buffer.
21	VDDIO	Supply	PWR	3.3 V supply for Digital IO. Can also be set to 2.5 V to support 2.5 V LVCMOS
22	GND	Ground	GND	Ground
23	MISO	Output	8X−LVCMOS	SPI data output
24	GND	Ground	GND	Ground
25	NC			Do not connect
26	NC			Do not connect
27	NC			Do not connect
28	DVDD	Bi−Directional	Analog	Output of the LDO supplying the digital core. Connect to 2.2 μF decoupling capacitance.
29	DVDD	Bi−Directional	Analog	Always connect to pin 28 in the application
30	GND	Ground	GND	Ground

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Type	Function
31	GND	Ground	GND	Ground
32	NC			Reserved, do not connect in the application
EP	GND	Ground	GND	Exposed Pad, NCN26010XMNTXG only

ABSOLUTE MAXIMUM RATINGS

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Value	Unit
VDD	Chip Supply	−0.3 to 3.63	V
GND	Ground	−0.3 to 0	V
T_{STG}	Storage Temperature Range	−65 to 150	°C
T_{SLD}	Lead Temperature, Soldering (10 Sec.)	260	°C
LINEP	Line Voltage P	−30 to 30	V
LINEN	Line Voltage N	−30 to 30	V
ESD_{HBM}	ESD Capability, Human Body Model (Note 1)	2	kV
ESD_{HBM_LINE}	ESD Capability for LINEP and LINEN Pins, Human Body Model (Note 1)	8	kV
ESD_{CDM}	ESD Capability, Charged Device Model (Note 1)	0.5	kV
LU	Latch−up Current Immunity (Note 1)	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested using the following methods @ T_A = 25°C:
   ESD Human Body Model per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current per JESD78

RECOMMENDED OPERATING RANGES

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Min	Typ	Max	Unit
VDD	Chip Supply	2.97	3.3	3.63	V
VDDIO	I/O Supply for 3.3 V Operation	2.97	3.3	3.63	V
VDDIO	I/O Supply for 2.5 V Operation	2.25	2.5	2.75	V
GND	Ground	−	0	−	V
T_{AMB}	Ambient Operating Temperature	−40	−	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

Table 4. PACKAGE THERMAL CHARACTERISTICS

Symbol	Rating	Device	Value	Unit
Θ_{JA}	Junction−to−Ambient, Still Air	NCN26010XMNTXG	56.5	K/W
Θ_{JA}	Junction−to−Ambient, Still Air	NCN26010XFBR2G	67.0	K/W

ELECTRICAL CHARACTERISTICS

Table 5. ELECTRICAL CHARACTERISTICS (These specifications are over recommended supply voltage and operating free−air temperature unless otherwise noted.)

Symbol	Rating	Condition	Min	Typ	Max	Unit
SUPPLY POWER						
P_{ACTIVE}	Power Consumption (Transmitting and Receiving Ethernet Packets)	VDDIO = VDD = 3.3 V ±10%	–	150	215	mW
$P_{ACTIVERX}$	Receive only Power Consumption (Powered On, but not Transmitting Ethernet Packets)	VDDIO = VDD = 3.3 V ±10%	–	75	–	mW
P_{IDLE}	Idle Power Consumption (Clocked and Enabled, but not Transmitting or Actively Receiving, No Activity on SPI)	VDDIO = VDD = 3.3 V ±10%	–	55	–	mW
CLOCK						
F_{XTAL}	XTAL Clock Frequency	VDD = VDDIO = 3.3 V ±10%	−100 ppm	25	+ 100 ppm	MHz
F_{EXT}	External Clock Frequency	VDD = 3.3 V ±10%, VDDIO = 2.5 V ±10%	−100 ppm	25	+100 ppm	MHz
F_{SPI}	SPI Clock Frequency	VDD = VDDIO = 3.3 V ±10%	–	–	25	MHz
		VDD = 3.3 V ±10%, VDDIO = 2.5 V ±10%	–	–	20	
LINE TRANSMITTER CHARACTERISTICS						
BIT_f	Data Rate (10BASE−T1S)		–	–	10	Mb/s
V_{OUTpp}	Peak Differential Output (Peak−to−peak) (Note 2)	VDD = 3.3 V ±10% TX_GAIN = default	800	1000	1200	mV
J_{TX}	Cycle−to−Cycle Jitter		–	0.2	1	ns
t_{rise}	Rise Time	VDD = 3.3 V ±10%	–	10	–	ns
t_{fall}	Fall Time	VDD = 3.3 V ±10%	–	10	–	ns
R_{OUT}	Output Impedance	VDD = 3.3 V ±10%	40	50	60	Ω
LINE RECEIVER CHARACTERISTICS (at the MDI)						
V_{THRX}	Receiver Threshold		–	0	–	mV
V_{EDRX}	Energy Detection Threshold (Note 2)	VDD = 3.3 V ±10% RX_ED = default	–	250	–	mV
V_{acc}	Threshold Accuracy		−30	–	30	mV
V_{CM}	Common Mode Voltage Range		−20	–	20	V
R_{IN}	Differential Input Resistance	Driver is High−Z (Not Transmitting)	25	40	60	kΩ
C_{IN}	Differential Input Capacitance (at 20 MHz)		–	5.5	7.5	pF
DIGITAL IOs						
V_{IL}	LVCMOS Input Level Low	VDDIO = 2.5 V ±10%	−0.3	–	0.7	V
		VDDIO = 3.3 V ±10%	−0.3	–	0.8	V
V_{IH}	LVCMOS Input Level High	VDDIO = 2.5 V ±10%	1.7	–	VDDIO + 0.3	V
		VDDIO = 3.3 V ±10%	2.0	–	VDDIO + 0.3	V
$V_{t-}(V_{IL})$	Schmitt Trigger Input Level Low	VDDIO = 2.5 V ±10%	0.7	–	1.5	V
		VDDIO = 3.3 V ±10%	0.7	–	1.9	V
$V_{t+}(V_{IH})$	Schmitt Trigger Input Level High	VDDIO = 2.5 V ±10%	0.9	–	1.7	V
		VDDIO = 3.3 V ±10%	0.9	–	2.1	V

Table 5. ELECTRICAL CHARACTERISTICS (These specifications are over recommended supply voltage and operating free−air temperature unless otherwise noted.) (continued)

Symbol	Rating	Condition	Min	Typ	Max	Unit
V_{hyst} ($\|V_{t+}-V_{t-}\|$)	Schmitt Trigger Input Hysteresis	VDDIO = 2.5 V ±10%	0.2	–	1.0	V
		VDDIO = 3.3 V ±10%	0.2	–	1.4	V
V_{OL}	Output Level Low	VDDIO = 2.5 V – 10% 4X−Type (Note 3) IOL = 2.48 mA	0	–	0.45	V
		VDDIO = 2.5 V – 10% 8X−Type IOL = 4.83 mA				
		VDDIO = 3.3 V – 10% 4X−Type IOL = 2.93 mA	0	–	0.4	V
		VDDIO = 3.3 V – 10% 8X−Type IOL = 5.65 mA				
V_{OH}	Output Level High	VDDIO = 2.5 V −10% 4X−Type IOH = −2.63 mA	VDDIO − 0.45	–	VDDIO	V
		VDDIO = 2.5 V −10% 8X−Type IOH = −5.11 mA				
		VDDIO = 3.3 V – 10% 4X−Type IOH = 3.19 mA	VDDIO − 0.4	–	VDDIO	V
		VDDIO = 3.3 V – 10% 8X−Type IOH = −6.12 mA				
I_{IL}	Input Current Low	0.0 V ≤ Vin ≤ VDDIO, max supply = 3.63 V	−11	–	11	μA
I_{IH}	Input Current High	0.0 V ≤ Vin ≤ VDDIO, max supply = 3.63 V	−11	–	11	μA
R_{PU}	Pull−Up Resistance		33	54	103	kΩ
R_{PD}	Pull−Down Resistance		30	44	73	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Default Value, can be altered by device configuration.
3. 4X and 8X denote the number of std LVCMOS input loads the buffer is designed to drive.

SPI Interface Timing

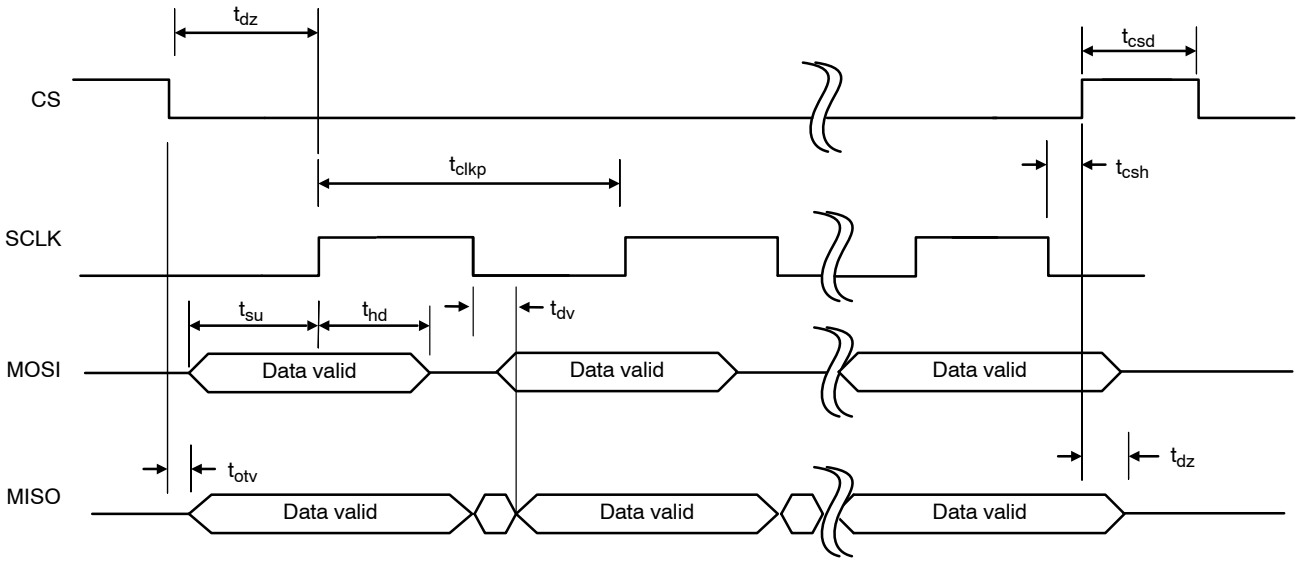


Figure 2. SPI Interface AC Timing Diagram

Table 6.

Symbol	Item	Condition	Min	Typ	Max	Unit
t_{clkp}	SPI Clock Period	VDDIO = 2.25 V – 3.63 V	40	–	–	ns
t_{su}	Data Input Setup Time	VDDIO = 2.25 V – 3.63 V	8	–	–	ns
t_{hd}	Data Input Hold Time	VDDIO = 2.25 V – 3.63 V	5	–	–	ns
t_{dv}	Output Data Valid	VDDIO = 3.3 V ±10%	–	–	12	ns
		VDDIO = 2.5 V ±10%	–	–	14.5	
t_{otv}	CS Low to MISO Out Valid	VDDIO = 3.3 V ±10%	–	–	12	ns
		VDDIO = 2.5 V ±10%	–	–	14.5	
t_{fc}	CS Low to Rising Edge of SCLK	VDDIO = 2.25 V – 3.63 V	20	–	–	ns
t_{csh}	SCLK Falling to CS De−assert	VDDIO = 2.25 V – 3.63 V	5	–	–	ns
		VDDIO = 2.5 V ±10%	5	–	14.5	
t_{dz}	CS De−assert to MISO HIGH−Z	VDDIO = 3.3 V ±10%	–	–	12	ns
		VDDIO = 2.5 V ±10%	–	–	14.5	

DETAILED DESCRIPTION

The NCN26010 is a 10BASE−T1S Physical Layer Transceiver as specified in IEEE 802.3cg with integrated Media Access Controller (MAC) and PLCA Reconciliation Sublayer.

It supports operation over a shared media (multi−drop) network segment with at least up to 25 m of a single twisted pair (UTP / STP) connection.

NCN26010 provides a Serial Peripheral Interface (SPI) in slave mode, allowing low pin count connection to standard, off−the−shelf Microcontrollers or other SPI host devices. The NCN26010 provides a shared bus speed of 10 Mb/s in Half−Duplex mode.

The MACPHY's SPI protocol is compliant to the specification issued by the Open Alliance[4].

The NCN26010 can be locally configured to run Physical Layer Collision Avoidance (PLCA), which supports at least 8 nodes on the shared medium, depending on environmental conditions.

PLCA improves data throughput under high network load and provides additional benefits:

- Nodes are granted transmit opportunities using a round robin arbitration scheme, enabling fair shared−access to the medium.
- By avoiding multiple back−off and retry events in the embedded MAC, maximum latencies are significantly reduced.
- Protects against the "babbling idiot" problem, as a single station can only transmit when granted an opportunity to do so.

The integration of the PLCA reconciliation sublayer (PLCA RS) in the device enables connected hosts to take full advantage of collision−free Ethernet communication on a single twisted pair, shared medium.

The integrated CSMA/CD 10 Mb/s MAC provides the following features:

- Multiple MAC address filtering
- Broadcast / Multicast filtering
- Promiscuous Mode (accept any frame regardless of type or destination address)
- FCS generation / checking
- Statistic / Diagnostic Counters
- Status reporting
- Factory−provided unique MAC address.

The SPI Protocol handler supports:

- 8 byte, 16 byte, 32 byte and 64 byte data chunks
- Both "Store & Forward" and "Cut−Through" operation
- Protected and Unprotected control transactions
- 4 kByte TX−Buffer
- 4 kByte RX−Buffer

Additional non−standard features are implemented into NCN26010:

- Enhanced Noise Immunity PMA operation (ENI)
- Collision detection masking
- PLCA Precedence Mode
- PLCA coordinator selection

The NCN26010 runs off a single 3.3 V supply.

The integrated crystal oscillator circuitry allows the use of an external CMOS oscillator, a quartz crystal, or any other external clock source, as long as its accuracy is in line with the specifications.

4. OPEN Alliance "TC6 – 10BASE−T1x MACPHY Serial interface Version 1.0", available from http://www.opensig.org

Boot Options

The NCN26010 offers two boot modes that can be selected using pin DIO0 as strapping pin during boot (hard reset or power up).

- NORMAL mode, DIO0 = 0: The NCN26010 works as a standard 10BASE−T1S MACPHY, connecting to the host via an SPI interface
- ISOLATED mode, DIO1 = 1: Same as NORMAL mode, except that all interface pins are kept in high impedance until the ISOLATED mode is disabled via SPI. Interrupt requests and SPI communication remain fully functional in this mode.

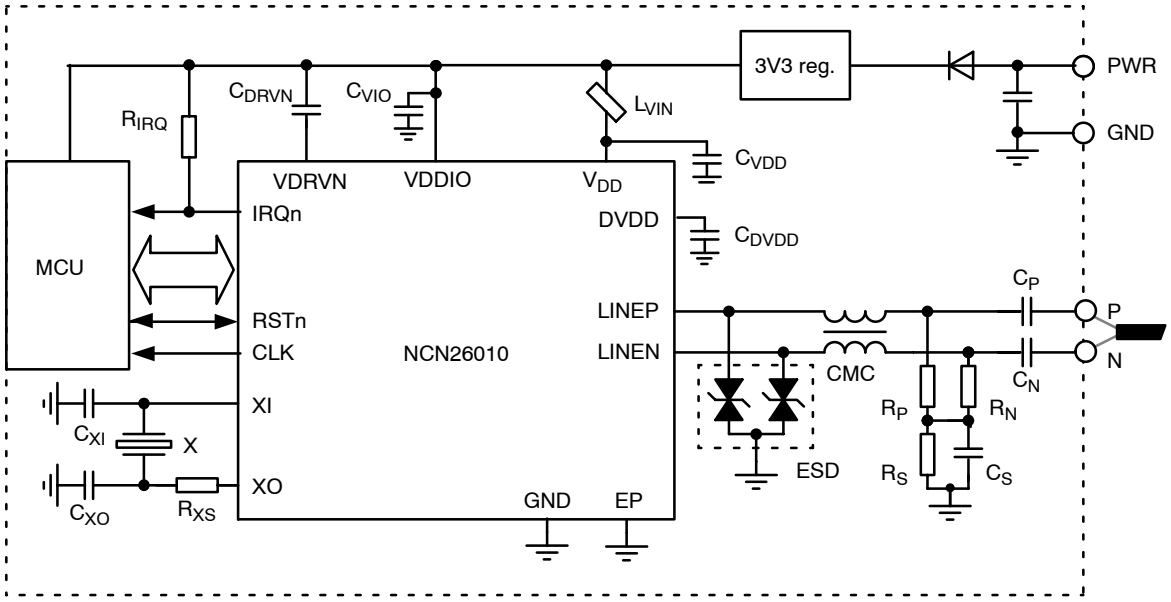


Figure 3. Basic Application Diagram

Table 7. RECOMMENDED EXTERNAL COMPONENTS FOR THE APPLICATION DIAGRAM

Component	Function	Value	Unit	Note
C_{VDD}	Filtering Capacitor, Ceramic	2.2	μF	±20%
C_{VIO}	Filtering Capacitor, Ceramic	100	nF	±10%
C_{DRVN}	Filtering Capacitor, Ceramic	2.2	μF	±20%
C_{DVDD}	Filtering Capacitor, Ceramic	2.2	μF	±20%
L_{VIN}	Noise Suppression Chip Ferrite Bead	1	kΩ	At 100 MHz
R_{IRQ}	IRQ Pull Up Resistor	10	kΩ	
X	Crystal	25	MHz	100 ppm or better, C_L = 12 pF
R_{XS}	Series Resistor	0	Ω	Depending on drive Level of the Crystal X
C_{XI}, C_{XO}	Load Capacitors	15	pF	<10%
CMC	Common Mode Choke (e.g. Murata DLW43MH201XK2L or TDK ACT45L−201−2P−TL−000)	200	μH	
C_P,C_N	DC−blocking Coupling Capacitors	100	nF	<10%, 50 V
R_P, R_N	Termination Resistor (Only for Head/Tail Nodes)	50	Ω	<1%, ≥0.4 W
C_S	Capacitor	4.7	nF	<10%, 50 V
R_S	Resistor	100	kΩ	<10%, ≥0.1 W
ESD	ESD Protection	ESD7241		optional

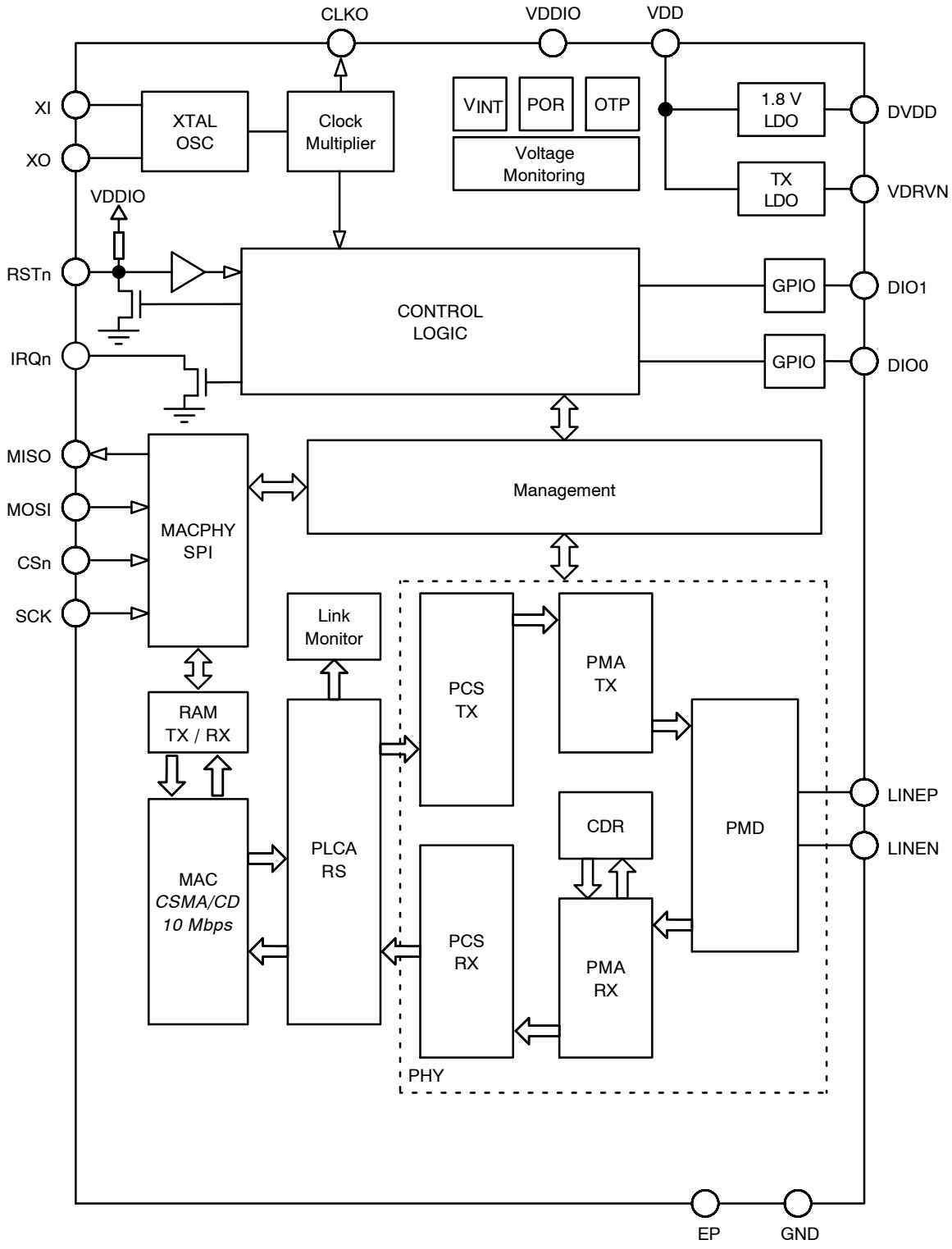


Figure 4. NCN26010 Simplified Block Diagram

Register Memory Map

The NCN26010 provides the registers in memory map selection groups. See the below table for details.

Table 8. MEMORY MAP SELECTION GROUPS

MMS	Width	Memory Map Description
0	32	Standard SPI Control and Status, PHY MIIM (Clause 22)
1	32	MAC registers
2	16	PHY– PCS Registers (IEEE802.3 MMD3)
3	16	PHY– PMA/PMD Registers (IEEE802.3 MMD 1)
4	16	PHY – PCLA and vendor specific Registers (MMD 31)
12	16	Vendor Specific Registers

The OA−SPI protocol always treats registers as 32 bit. Registers that are 16 bit wide have the two most significant bytes read as 0x00. For write commands to 16−bit registers, the two most significant bytes are ignored.

In this document, each register is defined by a table containing the following attributes:

- MMS: The target MMS (memory map selector) that together with ADDR uniquely identifies the register.
- ADDR: The 16−bit target address within the specified MMS at which the register can be accessed.
- DESCRIPTION: A brief description of the register and its purpose.

In the same table, each bit−field is further qualified by the following attributes:

- BIT: The bit position/range at which the field is located within the register.
- ACCESS: The allowed access type of the field, as specified in Table 9.
- SIGNAL: The name of the field.
- DEFAULT: The initial value of the register after a reset.

Table 9. DESCRIPTION OF REGISTER FIELD ACCESS TYPES USED IN THIS DOCUMENT

Access	Description
RW	The field can be read from and written to.
RW−x	Once the field is written to value “x”, it cannot be changed by a new write. Such field can only be cleared by a reset event.
RO	The field is read only. Writes to a RO field are ignored. If a DEFUALT value is present, then the field is a constant.
RO−SC	Read only field that self−clears on read.
RO−SCW	Read only field that clears on write. Writing to this field causes the field to be set to its reset state
RO−SCWx	Read only field with self−clear on writing value “x”. RO−SCW1 means the field clears to its reset value when writing a ‘1’. SCW0 clears the field by writing a 0.
RW−SCR	The field is a Read−Write, which self clears after a read access.
RW−SC	The field is a Read−Write field, whose content is cleared to its default value after the underlying operation completed.
RO−LH	Read−Only, Latch high on occurrence of the underlying event. Clears on read.
RO−LL	Read−Only, Latch low on occurrence of the underlying event. Clears on read.

Table 10. MEMORY MAP

MMS	Address	Name	Bit	7	6	5	4	3	2	1	0
0	0x0000	IDVER	31:24								
			23:16								
			15:8								
			7:0	MAJVER				MINVER			
	0x0001	PHYID	31:24	OUI[2:17]							
			23:16								
			15:8	OUI[18:23]						MODEL[5:4]	
			7:0	MODEL[3:0]				Rev			
	0x0002	STDCAP	31:24	RESERVED							
			23:16	RESERVED							
			15:8	RESERVED					TXFCSVC	IPRAC	DPRAC
			7:0	CTC	FTSC	AIDC	SEQC	RESERVED	MINCPS		
	0x0003	RESET	31:24								
			23:16								
			15:8								

Table 10. MEMORY MAP (continued)

MMS	Address	Name	Bit	7	6	5	4	3	2	1	0
			7:0								RESET
0	0x0004	CONFIG0	31:24								
			23:16								
			15:8	SYNC	TXFCSVE	CSARFE	ZARFE	TXCTHRESH		TXCTE	RXCTE
			7:0	FTSE	FTSS	PROTE	SEQE	RSVD	CPS		
	0x0005 – 0x0007	RESERVED	31:24	RESERVED							
			23:16								
			15:8								
			7:0								
	0x0008	STATUS0	31:24								
			23:16								
			15:8				CDPE	TXFCSE	RESERVED	RESERVED	RESERVED
			7:0	PHYINT	RESETC	HDRE	LOFE	RXBOE	TXBUE	TXBOE	TXPE
	0x0009 – 0x000A	RESERVED	31:24	RESERVED							
			23:16								
			15:8								
			7:0								
	0x000B	BUFSTS	31:24								
			23:16								
			15:8	TXC							
			7:0	RCA							
	0x000C	IMSK0	31:24								
			23:16								
			15:8				CDPEM	TXFCSEM	RESERVED		
			7:0	PHYINTM	RESETCM	HDREM	LOFEM	RXBOEM	TXBUEM	TXBOEM	TXPEM
	0x000D – 0xFEFF	RESERVED	31:24	RESERVED							
			23:16								
			15:8								
			7:0								
	0xFF00	PHYCTRL	31:24								
			23:16								
			15:8	RESET	LOOPBACK	SPEEDLSB	LNKCTRL		ISOLATE	LNKRST	DUPLEX
			7:0	COLTST	SPEEDMSB						
	0xFF01	PHYSTATUS	31:24								
			23:16								
			15:8					10MHALF			
			7:0	UNIDIR	SUPRPRE	LNKNEG	RMTFLT	AUTONEG	LNKSTS	JABDET	EXTCAP
	0xFF02	PHYID0	31:24								
			23:16								
			15:8	OUI[3:18]							
			7:0								
	0xFF03	PHYID1	31:24								
			23:16								
			15:8	OUI[19:24]						MODEL[5:4]	
			7:0	MODEL[3:0]				CHIPREV			
1	0x0000	MACCTRL0	31:24								
			23:16			IPGNF	BKOD	NFCSF	MCSF	BCSF	ADRF
			15:8								FCSA
			7:0							TXEN	RXEN
	0x0001 – 0x000F	RESERVED	31:24	RESERVED							
			23:16								
			15:8								

Table 10. MEMORY MAP (continued)

MMS	Address	Name	Bit	7	6	5	4	3	2	1	0
1			7:0								
	0x0010	ADDRFILT0L	31:24	ADDRFILT0[31:0]							
			23:16								
			15:8								
			7:0								
	0x0011	ADDRFILT0H	31:24	EN							
			23:16								
			15:8	ADDRFILT0[47:32]							
			7:0								
	0x0012	ADDRFILT1L	31:24	ADDRFILT1[31:0]							
			23:16								
			15:8								
			7:0								
	0x0013	ADDRFILT1H	31:24	EN							
			23:16								
			15:8	ADDRFILT1[47:32]							
			7:0								
	0x0014	ADDRFILT2L	31:24	ADDRFILT2[31:0]							
			23:16								
			15:8								
			7:0								
	0x0015	ADDRFILT2H	31:24	EN							
			23:16								
			15:8	ADDRFILT2[47:32]							
			7:0								
	0x0016	ADDRFILT3L	31:24	ADDRFILT3[31:0]							
			23:16								
			15:8								
			7:0								
	0x0017	ADDRFILT3H	31:24	EN							
			23:16								
			15:8	ADDRFILT3[47:32]							
			7:0								
	0x0018 – 0x001F	RESERVED	31:24	RESERVED							
			23:16								
			15:8								
			7:0								
	0x0020	ADDRMASK0L	31:24	ADDRMASK0[31:0]							
			23:16								
			15:8								
			7:0								
	0x0021	ADDRMASK0H	31:24								
			23:16								
			15:8	ADDRMASK0[47:32]							
			7:0								
	0x0022	ADDRMASK1L	31:24	ADDRMASK1[31:0]							
			23:16								
			15:8								
			7:0								
	0x0023	ADDRMASK1H	31:24								
			23:16								
			15:8	ADDRMASK1[47:32]							

Table 10. MEMORY MAP (continued)

MMS	Address	Name	Bit	7	6	5	4	3	2	1	0
			7:0								
1	0x0024	ADDRMASK2L	31:24	ADDRMASK2[31:0]							
			23:16								
			15:8								
			7:0								
	0x0025	ADDRMASK2H	31:24								
			23:16								
			15:8	ADDRMASK2[47:32]							
			7:0								
	0x0026	ADDRMASK3L	31:24	ADDRMASK3[31:0]							
			23:16								
			15:8								
			7:0								
	0x0027	ADDRMASK3H	31:24								
			23:16								
			15:8	ADDRMASK3[47:32]							
			7:0								
	0x0028 – 0x002F	RESERVED	31:24	RESERVED							
			23:16								
			15:8								
			7:0								
	0x0030	STOCTETSTXL	31:24	STOCTETSTX[31:0]							
			23:16								
			15:8								
			7:0								
	0x0031	STOCTETSTXH	31:24								
			23:16								
			15:8	STOCTETSTX[47:32]							
			7:0								
	0x0032	STFRAMESTXOK	31:24	STFRAMESTXOK[31:0]							
			23:16								
			15:8								
			7:0								
	0x0033	STBCASTTXOK	31:24	STBCASTTXOK[31:0]							
			23:16								
			15:8								
			7:0								
	0x0034	STMCASTTXOK	31:24	STMCASTTXOK[31:0]							
			23:16								
			15:8								
			7:0								
	0x0035	STFRAMESTX64	31:24	STFRAMESTX64[31:0]							
			23:16								
			15:8								
			7:0								
	0x0036	STFRAMESTX65	31:24	STFRAMESTX65[31:0]							
			23:16								
			15:8								
			7:0								
	0x0037	STFRAMESTX128	31:24	STFRAMESTX128[31:0]							
			23:16								
			15:8								

Table 10. MEMORY MAP (continued)

MMS	Address	Name	Bit	7	6	5	4	3	2	1	0
1			7:0								
	0x0038	STFRAMESTX256	31:24	STFRAMESTX256[31:0]							
			23:16								
			15:8								
			7:0								
	0x0039	STFRAMESTX512	31:24	STFRAMESTX512[31:0]							
			23:16								
			15:8								
			7:0								
	0x003A	STFRAMESTX1024	31:24	STFRAMESTX1024[31:0]							
			23:16								
			15:8								
			7:0								
	0x003B	STUNDERFLOW	31:24								
			23:16								
			15:8							STUNDERFLOW[9:8]	
			7:0	STUNDERFLOW[7:0]							
	0x003C	STSINGLECOL	31:24								
			23:16							STSINGLECOL[17:16]	
			15:8	STSINGLECOL[15:10]							
			7:0								
	0x003D	STMULTICOL	31:24								
			23:16							STMULTICOL[17:16]	
			15:8	STMULTICOL[15:10]							
			7:0								
	0x003E	STEXCESSCOL	31:24								
			23:16								
			15:8							STMULTICOL[9:8]	
			7:0	STMULTICOL[7:0]							
	0x003F	STDEFERREDTX	31:24								
			23:16							STDEFERREDTX[17:16]	
			15:8	STDEFERREDTX[15:10]							
			7:0								
	0x0040	STCRSERR	31:24								
			23:16								
			15:8							STCRSERR[9:8]	
			7:0	STCRSERR[7:0]							
	0x0041	STOCTETSRXL	31:24	STOCTETSRX[31:0]							
			23:16								
			15:8								
			7:0								
	0x0042	STOCTETSRXH	31:24								
			23:16								
			15:8	STOCTETSRX[47:32]							
			7:0								
	0x0043	STFRAMESRXOK	31:24	STFRAMESRXOK[31:0]							
			23:16								
			15:8								
			7:0								
	0x0044	STBCASTRXOK	31:24	STBCASTRXOK[31:0]							
			23:16								
			15:8								

Table 10. MEMORY MAP (continued)

MMS	Address	Name	Bit	7	6	5	4	3	2	1	0
			7:0								
1	0x0045	STMCASTRXOK	31:24	STMCASTRXOK[31:0]							
			23:16								
			15:8								
			7:0								
	0x0046	STFRAMESRX64	31:24	STFRAMESRX64[31:0]							
			23:16								
			15:8								
			7:0								
	0x0047	STFRAMESRX65	31:24	STFRAMESRX65[31:0]							
			23:16								
			15:8								
			7:0								
	0x0048	STFRAMESRX128	31:24	STFRAMESRX128[31:0]							
			23:16								
			15:8								
			7:0								
	0x0049	STFRAMESRX256	31:24	STFRAMESRX256[31:0]							
			23:16								
			15:8								
			7:0								
	0x004A	STFRAMESRX512	31:24	STFRAMESRX512[31:0]							
			23:16								
			15:8								
			7:0								
	0x004B	STFRAMESRX1024	31:24	STFRAMESRX1024[31:0]							
			23:16								
			15:8								
			7:0								
	0x004C	STRUNTSERR	31:24								
			23:16								
			15:8								STRUNTERR[9:8]
			7:0	STRUNTERR[7:0]							
	0x004D	STRXTOOLONG	31:24								
			23:16								
			15:8								STRXTOOLONG[9:8]
			7:0	STRXTOOLONG[7:0]							
	0x004E	STFCSERRS	31:24								
			23:16								
			15:8								STFCSERR[9:8]
			7:0	STFCSERR[7:0]							
	0x004F	STSYMBOLERRS	31:24								
			23:16								
			15:8								STSYMBOLERRS[9:8]
			7:0	STSYMBOLERRS[7:0]							
	0x0050	STALIGNERRS	31:24								
			23:16								
			15:8								STALIGNERRS[9:8]
			7:0	STALIGNERRS[7:0]							
	0x0051	STRXOVERFLOW	31:24								
			23:16								
			15:8								STRXOVERFLOW[9:8]

Table 10. MEMORY MAP (continued)

MMS	Address	Name	Bit	7	6	5	4	3	2	1	0
			7:0	STRXOVERFLOW[7:0]							
1	0x0052	STRXDROPPED	31:24	STRXDROPPED[31:0]							
			23:16								
			15:8								
			7:0								
2	0x0005	DEVINPKG1	15:8								
			7:0					PCSPRSNT		PMAPRSNT	C22PRSNT
	0x0006	DEVINPKG2	15:8								
			7:0								
	0x0007 – 0x08F2	RESERVED	15:8								
			7:0								
	0x08F3	T1SPCSCTRL	15:8	PCSRST	LOOPBACK						
			7:0								
	0x08F4	T1SPCSSTATUS	15:8								
			7:0	FAULT							
	0x08F5	T1SPCSRMTJAB	15:8	T1SPCSRMTJAB							
			7:0								
	0x08F6	T1SPCSPHYCOL	15:8	T1SPCSPHYCOL							
			7:0								
3	0x0005	DEVINPKG1	15:8								
			7:0					PCSPRSNT		PMAPRSNT	C22PRSNT
	0x0006	DEVINPKG2	15:8								
			7:0								
	0x0007 – 0x0011	RESERVED	15:8								
			7:0								
	0x0012	BASET1EXTABLTY	15:8								
			7:0					10BASE−T1S			
	0x0013 – 0x08F8	RESERVED	15:8								
			7:0								
	0x08F9	T1SPMACTRL	15:8	PMARST	PMATXDIS			LPM	MDE		
			7:0								LOOPBACK
	0x08FA	T1SPMASTS	15:8			LBA		LPA	MDA	RXFA	
			7:0							RXRJ	
	0x08FB	T1STMCTL	15:8	TMCTL							
			7:0								
4	0x0000 – 0x7FFF	RESERVED	15:8								
			7:0								
	0x8000	CHIPREV	15:8	MAJOREV				MINOREV			
			7:0	STAGE		PATCH					
	0x8001	PHYCFG1	15:8	RSVD							
			7:0	ENI	UTE				SCRDIS	NOCOLMSK	RXDLY
	0x8002	PLCAEXT	15:8	PRECEDENCE				RSVD			
			7:0							LDRMODE	LDRROLE
	0x8003	PMATUNE0	15:8			BEACONTHR					
			7:0						DRIFTCMP		
	0x8004	PMATUNE1	15:8			PREAMBLETHR					
			7:0			COMMITTHR					
	0x8005 – 0xC9FF	RESERVED	15:8								
			7:0								
	0xCA00	PLCAREGMAP	15:8	MAPID							
			7:0	MAPVER							
	0xCA01	PLCACTRL0	15:8	PLCAENABLE	PLCARESET						

Table 10. MEMORY MAP (continued)

MMS	Address	Name	Bit	7	6	5	4	3	2	1	0
4			7:0								
	0xCA02	PLCACTRL1	15:8	PLCANCNT							
			7:0	PLCAID							
	0xCA03	PLCASTS	15:8	PST							
			7:0								
	0xCA04	PLCATOTMR	15:8								
			7:0	TOTMR							
	0xCA05	PLCABURST	15:8	MAXBC							
			7:0	BTMR							
12	0x0000 – 0x000F	RESERVED	15:8								
			7:0								
	0x0010	MIIMIRQCTRL	15:8								
			7:0			PCOL	PLCARECOV	RMTJAB	LCLJAB	PLCACHNG	LNKCHNG
	0x0011	MIIMIRQSTS	15:8	RESETSTS							
			7:0			COL	RECOV	RJAB	LJAB	PLCASTS	LNKSTS
	0x0012	DIOCFG	15:8	SLEW1	PULLEN1	PULLTYPE1	FN1				VAL1
			7:0	SLEW0	PULLEN0	PULLTYPE0	FN0				VAL0
	0x0013 – 0x1000	RESERVED	15:8								
			7:0								
	0x1001	PHYTWEAK	15:8	TXGAIN		RXCDTHR				RXEDTHR[3:2]	
			7:0	RXEDTHR[1:0]		DIGSLEW	CMCCOMP		TXSLEW		CLKOUTEN
	0x1002	MACID0	15:8	MACID[15:0]							
			7:0								
	0x1003	MACID1	15:8								
			7:0	MACID[23:16]							
	0x1004	CHIPINFO	15:8		WAFERY						
			7:0		WAFERX						
	0x1005	NVMHEALTH	15:8	REDWARN	REDERR	YELWARN	YELERR	GRNWARN	GREENERR		
			7:0								

MMS0 Registers

SPI IDENTIFICATION REGISTER, IDVER (MMS0, ADDRESS 0x0000)

Bit(s)	Name	Description	Default Value	Type
31:8	Reserved	Always reads 0	0	RO
7:4	MAJVER	Major Version number	0001	RO
3:0	MINVER	Minor Version number	0001	RO

SPI IDENTIFICATION REGISTER, PHYID (MMS0, ADDRESS 0x0001)

Bit(s)	Name	Description	Default Value	Type
31:10	OUI	Organizational Unique Identifier Records the 22 MSB's of the OUI in reverse order. Bit 31 maps to bit 2 of the OUI, bit 0 maps to bit 23 of the OUI NOTE: **onsemi**'s OUI in its canonical form is: 60−C0−BF	0x0603FD	RO
9:4	MODEL	Model number	1010	RO
3:0	REV	Chip Revision number	0001	RO

SPI CAPABILITIES, SPICAP (MMS0, ADDRESS 0x0002)

Bit(s)	Name	Description	Default Value	Type
31:11	Reserved	Do not consider content	0x000000	RO
10	TXFCSVC	TX Frame Check Sequence Verification NCN26010 MAC supports checking the FCS on outgoing frames when not configured to compute and append the FCS to TX frames. When this feature is enabled and the MACPHY is operating in "store & forward" mode, frames from the SPI having an incorrect checksum are not forwarded to the line. If the MACPHY is operating in "cut−through" mode, incorrect frames are aborted in such a way the receiving nodes discard them.	1	RO
9	IPRAC	Indirect PHY register access Not supported by NCN26010.	0	RO
8	DPRAC	Direct PHY register access capability NCN26010's PHY registers are accessed using direct access through SPI control transactions.	1	RO
7	CTC	Cut−through Capability NCN26010 can operate in Cut−through−Mode.	1	RO
6	FTC	Frame Timestamp Capability NCN26010 does not provide Frame Timestamping functionality.	0	RO
5	AIDC	Address Increment Disable Capability The SPI protocol implemented into NCN26010 supports disabling the address auto−increment during control transactions, allowing the host to perform repeated read/write access to the same register	1	RO
4	SEQ	TX data chunk sequencing and retry. Not supported.	0	RO
3	N/A	Not used	0	RO
2:0	MINCPS	Minimum supported Chunk Payload Size NCN26010 supports 8 byte minimum payload size. See OPEN Alliance specification section 9.2.3.9 for details.	0x3	RO

RESET CONTROL AND STATUS, RESET (MMS0, ADDRESS 0x0003)

Bit(s)	Name	Description	Default Value	Type
31:1	N/A	Not used	0x000000	RO
0	RESET	Soft Reset Writing a 1 into this bit initiates a MAC and PHY reset to their initial state. Reset starts after CS pin is de−asserted.	0	RW−SC

SPI PROTOCOL CONFIGURATION REGISTER, CONFIG0 (MMS0, ADDRESS 0x0004)

Bit(s)	Name	Description	Default Value	Type
31:16	N/A	Bits contain no valid data	0x0000	RO
15	SYNC	Configuration Synchronization When set to 0, the NCN26010 does not accept TX or RX frames, as its configuration may not be complete. Once the host completes configuration of the NCN26010, it should set this bit to 1. Once set, the bit can only be cleared by a system reset.	0	RW−1
14	TXFCSVE	Transmit Frame CheckSequence Validation Enable. When set, the final 4 octets of all Ethernet frames conveyed via SPI are validated as an Ethernet FCS. When using this option, the FCSA bit in the MACCTRL0 shall be cleared.	0	RW
13	CSARFE	CS Align Receive Frame Enable When set, all received Ethernet frames start at the beginning of the receive chunk following the CSn assertion with a Start Word Offset of zero. When this bit is cleared, received frames may begin anywhere within the chunk payload.	0	RW
12	ZARFE	Zero Align Receive Frame Enable When set, all received Ethernet frames start at the beginning of the received chunk with a Start Word Offset of zero. When this bit is cleared, received frames may begin anywhere within the chunk payload.	0	RW
11:10	TXCTHRESH	Transmit Credit Threshold Configures the minimum number of transmit credits (TXC) that have to be available for asserting IRQn, after TXC went down to zero 00 ≥ 1 credit (the default) 01 ≥ 4 credits 10 ≥ 8 credits 11 ≥ 16 credits	00	RW
9	TXCTE	Transmit cut−through enable When set to one, this bit enables sending frames in cut−through mode to reduce the average TX latency.	0	RW
8	RXCTE	Receive cut−through enable When set to one, this bit enables receiving frames in cut−through mode to reduce the average RX latency.	0	RW
7	FTSE	Frame Timestamp enable This feature is not supported by NCN26010. This bit is read only	0	RO
6	FTSS	Receive Frame Timestamp Select This feature is not supported by NCN26010. This bit is read only	0	RO
5	PROTE	Enable Control Data Read/Write Protection Refer to OPEN Alliance specification section 7.4 for details.	0	RW
4:3	N/A	Not used	00	RO
2:0	CPS	Chunk Payload Size Configuration 0x3 Chunk Payload size is 8 bytes 0x4 Chunk Payload size is 16 bytes 0x5 Chunk Payload size is 32 bytes 0x6 Chunk Payload site is 64 bytes (default)	0x6	RW

SPI PROTOCOL STATUS REGISTER, STATUS0 (MMS0, ADDRESS 0x0008)

Bit(s)	Name	Description	Default Value	Type
31:13	N/A	Not used	0x0000	RO
12	CDPE	Control Data Protection Error When configured to control data read/write protection (set bit PORTE of CONFIG0 Register), this bit indicates that the MACPHY has detected an error in the last control transaction.	0	RC−SCW1
11	TXFCSE	When set, this bit indicates that the MACPHY has detected that the outgoing frame's FCS added by the host is invalid. To clear this bit, write a "1" to this field.	0	RC−SCW1
10	TTSCAC	Always 0. Time stamping is not supported by the NCN26010	0	RO
9	TTSCAB	Always 0. Time stamping is not supported by the NCN26010	0	RO
8	TTSCAA	Always 0. Time stamping is not supported by the NCN26010	0	RO
7	PHYINT	PHY interrupt When 1, the embedded PHY is generating an interrupt request. This bit can only be cleared when the interrupt event of the PHY is acknowledged	0	RO
6	RESETC	Reset complete This bit is set when the reset procedure is completed and the device is ready to be configured. When set, it will generate a non−maskable interrupt on IRQn to notify the SPI host that the reset has completed. In addition, when this bit is set, the EXST bit in the RX footer is also set. To clear this bit, the host shall write a 1 to it.	1	RC−SCW1
5	HDRE	Header Error. Indicates that a header error occurred since this bit was last cleared. When set, the MACPHY has detected an invalid header received from the SPI host due to a parity check error.	0	RC−SCW1
4	LOFE	Loss of Framing Error When 1, this bit indicates that the NCN26010 has detected a de−assertion of CS prior to the expected end of a data chunk or a command control transaction, resulting in loss of data.	0	RC−SCW1
3	RXBOE	Receive buffer Overflow Error When 1, this bit indicates that a frame coming from the network was discarded due to the receive buffer being full	0	RC−SCW1
2	TXBUE	Transmit Buffer Underflow Error When 1, this bit indicates that the transmit buffer experienced an underflow condition and the transmitted frame was lost. This situation can only happen when the NCN26010 is configured to operate in TX cut−through mode.	0	RC−SCW1
1	TXBOE	Transmit Buffer Overflow Error When 1, this bit indicates that the transmit buffer overflowed and that the transmit frame data was lost.	0	RC−SCW1
0	TXPE	Transmit Protocol Error When set, this bit indicates that a TX Data Chunk error occurred. This error gets flagged under any of following error conditions: • Data chunk with DV=1 but without a prior or concurent SV=1 • Data chunk with SV=1 but with no EV=1 (repeated SV=1). • Data chunk with EV=1 without a prior SV=1 • The values of the SWO and/or EBO fields in the header exceed the CPS setting on the SPICONFIG0 register. (e.g. CPS set to 32 bit chunk size and SWO points to bit 40) See OPEN Alliance protocol specification for details.	0	RC−SCW1

BUFFER STATUS REGISTER, BUFSTS (MMS0, ADDRESS 0x000B)

Bit(s)	Name	Description	Default Value	Type
31:16	N/A	Not used	0x000000	RO
15:8	TXC	Transmit Credits Available Reports the number of data chunks available in the transmit buffer. Writing chunks when TXC is 0, results in a transmit buffer overflow. The lower five bits of the TXC are also contained in the TXC field of the SPI protocol's footer (the last 4 bytes of a received data chunk). The NCN26010 provides a 4 kByte buffer for TX data.	0x3C	RO
7:0	RCA	Receive Chunks Available Number of data chunks currently available for the SPI host to read. Reading this field allows the SPI host, for example, to queue that number of receive chunks available into a single DMA transfer. The lower 5 bits of this field are also reported in the RCA field of every RX data footer. The NCN26010 provides a 4 kByte buffer for RX data.	0000	RO

INTERRUPT MASK REGISTER, IMASK (MMS0, ADDRESS 0x000C)

Bit(s)	Name	Description	Default Value	Type
31:13	N/A	Not used	0x0000	RO
12	CDPEM	Control Data Protection Error Mask When set to 1, the Control Data Protection status bit in SPI STATUS0 register does not set the EXST bit in the data footer, and prevents IRQn from being asserted.	1	RW
11	TXFCSEM	TX frame check sequence error mask When set to 1, the Transmit FCS Error (TXFCSE) status bit in STATUS0 register deos not set the EXST bit in the data footer, and prevents IRQn from being asserted.	1	RW
10	Reserved		1	RO
9	Reserved		1	RO
8	Reserved		1	RO
7	PHYINTM	PHY interrupt Mask When set to 1, physical layer interrupt (PHYINT) status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
6	RESETCM	Reset complete Mask When set to 1, reset complete (RESERTC) status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	0	RW
5	HDREM	Header Error Mask When set to 1, a SPI Header Error (HDRE) does not assert IRQn or EXST in the data chunk footer.	1	RO
4	LOFEM	Loss of Frame Error Mask When set to 1, the LOFE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
3	RXDOEM	Receive Buffer Overflow Error Mask When set to 1, the RXDOE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
2	TXBUEM	Transmit Buffer Underflow Error Mask When set to 1, the TXBUE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
1	TXBOEM	Transmit Buffer Overflow Error Mask When set to 1, the TXBOE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
0	TXPEM	Transmit Protocol Error Mask When set to 1, the TXPE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW

PHY CONTROL REGISTER (MMS0, ADDRESS 0xFF00)

Bit(s)	Name	Description	Default Value	Type
31:16	N/A	Not used	0x0000	RO
15	Reset	1 = PHY reset 0 = normal operation When set, a soft reset is initiated. The soft reset does not cause bootstrapping, ignoring changes in strap−pin configuration. All registers revert to their default values and any communication is interrupted. After the soft reset procedure is completed, this bit is automatically reset to 0 (default).	0	RW SC
14	Loopback	1 = loopback mode enabled 0 = loopback mode disabled When set to 1, frames are looped back to the MAC rather than being sent over the line. In this mode, the transceiver is isolated from the line.	0	RW
13	Speed (LSB)	See bit 6 below	0	RO
12	Link Control	1 = PHY transmit/receive enabled 0 = PHY transmit/receive disabled The implementation of this bit differs from IEEE 802.3cg Clause 22.2.4.1.4 (Auto negotiation Enable).	0	RW
11	N/A		0	RO
10	Isolate	1 = Isolation enabled 0 = Normal Operation When set to 1, all pins are set to tristate except for the SPI interface and the IRQn pin. The default state depends on the bootstrap configuration.	−	RW
9	Link Reset	1 = Reset Link 0 = Normal Operation When set to 1, the link is reset, then normal operation resumes. This behavior differs from IEEE802.3 Clause 22.2.4.1.7, but allows the device to be managed by standard software drivers.	0	RW−SC
8	Duplex Mode	0 = Half−Duplex This is a read only flag. Zero indicates that the NCN26010 only supports half−duplex operation.	0	RO
7	Collision Test	1 = Collision Test enabled 0 = Normal Operation For a description of collision test mode, see IEEE802.3 Clause 22.2.4.1.9.	0	RW
6	Speed (MSB)	Link speed capability Together with bit 13, this bit indicates that the PHY only supports 10 Mb/s. Both bit 6 and bit 13 reads as zero.	0	RO
5:0	−	Not used	0000	RO

PHY STATUS REGISTER (MMS0, ADDRESS 0xFF01)

Bit(s)	Name	Description	Default Value	Type
31:12	–	Always reads 0	0	RO
11	10 Mb/s Half Duplex	Always reads 1 Indicates the PHY is a 10 Mb/s half−duplex device.	1	RO
10:8	–	Always reads 0	000	RO
7	Unidirectional Ability	Always reads 0 10BASE−T1S does not support unidirectional links.	0	RO
6	MF Preamble Suppression	Always reads 0 The PHY does not accept MDIO frames with suppressed preamble. NOTE: this is not relevant for the NCN26010 as the devices has no MDIO interface	0	RO
5	Link Negotiation Complete	1 = link negotiation complete 0 = link negotiation in progress The PHY sets this bit when PHY Control register bit 12 = 1 and bit 9 = 0. This bit is further masked by PLCA status when PLCA is enabled. This prevents standard drivers from sending a packet while PLCA is starting. The implementation is different from IEEE 802.3 Clause 22.2.4.2.10 (Auto negotiation Enable), but allows the NCN26010 to be managed by standard software drivers.	–	RO
4	Remote Fault	1 = remote jabber detected 0 = no remote jabber detected The fault condition is latched until this field is read or the integrated PHY is reset.	–	R−LH SC
3	Auto−Negotiation Ability	Always reads 1 The device does not support auto negotiation, but this bit is set to 1 to allow the NCN26010 to be managed by standard software drivers.	1	RO
2	Link Status	1 = link is up 0 = link is down	–	RO
1	Jabber Detect	1 = local jabber detected 0 = no local jabber detected The fault condition is latched until this field is read, or the integrated PHY is reset. See also 802.3cg Clause 147.3.2.9	–	R−LH SC
0	Extended Capability	Always reads 1 Indicates that the integrated PHY contains registers that are normally found in Clause 45 of the IEEE802.3 specification.	1	RO

PHY IDENTIFIER REGISTERS (MMS0, ADDRESS 0xFF02 AND 0xFF03)

Bit(s)	Name	Description	Default Value	Type
0xFF02[31:16]	–	Not used	0x0000	RO
0xFF02[15:0]	PHY Identifier MSB	OUI [3:18] Note that the bit order is reversed. Bit 15 corresponds to bit 3 of the OUI; bit 0 corresponds to bit 18 of the OUI.	0x180F	RO
0xFF03[31:16]	–	Not used	0x0000	RO
0xFF03[15:10]	PHY Identifier LSB	OUI[19:24] NOTE: Bit order is reversed. Bit 15 corresponds to bit 19 of the OUI, bit 10 corresponds to bit 24 of the OUI.	0x35	RO
0xFF03[9:4]	PHY Identifier LSB	IC Model Number	0x1A	RO
0xFF03[3:0]	PHY Identifier LSB	Chip Revision Number	0x1	RO

MMS1 Registers

Memory Map Selection 1 contains all registers related to the Media Access Controller (MAC) of the NCN26010 device

MAC CONTROL0 REGISTER (MMS1, ADDRESS 0x0000)

Bit(s)	Name	Description	Default Value	Type
31:22	–	Not used	0x000	RO
21	IPGNF (Inter Packet Gap No Filter)	1 = Inter−Packet Gap Filter disabled 0 = Inter−Packet Gap Filter enabled When enabled, the MAC does not restart the Inter Packet Gap counter if a glitch on carrier sense is detected within 2/3 of the nominal IPG period. Enabling IPGNF may help improve performance in high impulse noise environments. NOTE: Depending on the network design and noise environment, enabling this bit may actually degrade performance. If unsure, leave IPGNF disabled.	0	RW
20	BKOD (Back−off Disable)	1 = back−off disabled 0 = back−off enabled When set, the MAC does not perform back−off after a collision has been detected. This feature may be useful in conjunction with the PLCA RS in high impulse noise environments, as it makes the MAC automatically retransmit disrupted packets. NOTE: Setting BKOD to 1 enables a non−standard feature that can affect interoperability and performance in plain (non−PLCA) CSMA/CD networks. When in doubt, leave this option to its default state.	0	RW
19	NFCSF (FCS Filter Disable)	1 = FCS filtering disabled 0 = FCS filtering enabled No FCS Filter: when enabled, RX frames are forwarded to the host even if their FCS (CRC) is invalid. The host will still be able to determine if an FCS error occurred by checking the FD bit in the SPI Protocol footer. See OPEN Alliance documentation for details on the RX footer.	0	RW
18	MCSF (Multicast Filter Enable)	1 = multicast filter enabled 0 = multicast filter disabled When enabled, the MAC discards RX frames with a multi cast destination address (first bit of the destination address set to 1). See IEEE802.3 clause 3.2.3 for details. When set, discarded frames are counted in the STRXDROPPED statistics counter (MMS 1 address 0x0052). Note that the MAC address is typically represented in little−endian bit order. The first address bit (I/G) defined in the IEEE Standard is the least significant bit of the first byte. Example: 01:54:09:AA:4C:02 is a multicast address, 84:2D:FC:65:98:07 is a unicast address. Broadcast frames are still forwarded, depending on the setting of bit 17, even if this filter is active.	0	RW
17	BCSF (Broadcast Filter Enable)	1 = broadcast filter enabled 0 = broadcast filter disabled When enabled, the MAC discards frames with broadcast destination address (FF:FF:FF:FF:FF:FF). If a frame is discarded as a consequence of enabling this filter, it will be counted in the STRXDROPPED statistic register (MMS1 address 0x0052).	0	RW
16	ADRF (Address Filter Enable)	1 = destination Address Filter enabled 0 = destination Address Filter disabled When enabled, the MAC checks the destination address of the incoming frame against the ADDRFILTx/ADDRMASKx registers to decide if the frame has to be accepted or rejected. When disabled, the MAC will enter promiscuous mode, accepting every frame regardless of its destination address. The promiscuous mode is helpful for monitoring network traffic or for implementing bridging in multi−port hosts.	0	RW
15:9	–	Not used	0x00	RO

MAC CONTROL0 REGISTER (MMS1, ADDRESS 0x0000) (continued)

Bit(s)	Name	Description	Default Value	Type
8	FCSA (FCS Append)	1 = calculate & append FCS 0 = do not add FCS When enabled, the MAC inside NCN26010 computes and auto−appends the FCS (fame check sequence) to outgoing TX Frames, off−loading the host controller from having to calculate the FCS. When cleared, the MAC expects the FCS to be included in the frame data offered by the host controller. In safety critical application and in application in which SPI transmission errors could occur, this feature should not be used. In such situation the host should calculate and append the FCS prior to passing the frame data to the MACPHY over SPI (FCSA=0). When enabled, frames shorter than 64 bytes will be padded up by the MAC. When disabled, the host *shall* perform padding, otherwise frames will be corrupted.	1	RW
7:2	−	Not used	0x00	RO
1	TXEN (Transmit Enable)	1= TX enabled 0 = TX disabled When set, the MAC transmit functions are enabled, and packets conveyed by the host are forwarded to the embedded PHY. When this bit is cleared, frames coming from the host interface are kept in RAM but no data is passed to the internal PHY. When TXEN is cleared during an active frame transmission, the MAC defers entering TX disabled state until the frame is sent in full. Clearing TXEN also resets all statistics registers that count TX events (MMS 1, addresses 0x0030 to 0x0040)	0	RW
0	RXEN (Receive Enable)	1 = RX enable 0 = RX disable When set, the MAC receive functions are enabled and packets from the embedded PHY are forwarded to the host. When cleared, frames coming from the PHY functions of the NCN26010 are silently discarded, and no data is conveyed to the host. Clearing RXEN also resets all statistics registers that count RX events (MMS 1, addresses 0x0041 to 0x0052) If RXEN is cleared while a reception is ongoing, the transfer is not interrupted. Hence, this bit can be used to perform a graceful shutdown of the MAC's RX function. If RXEN is enabled while the integrated PHY is already conveying data to the MAC, the current reception is skipped, preventing the MAC form transferring corrupted or incomplete data to the host.	0	RW

ADDRESS FILTER LOW 0, ADDRFILT0L (MMS1, ADDRESS 0x0010)

Bit(s)	Name	Description	Default Value	Type
31:0	ADDFILT0[31:0]	Holds the 32 lower order bits of the Address Filter that is spilt into ADDRFILT0L and ADDRFILT0H.	0x00000000	RW

ADDRESS FILTER HIGH 0, ADDRFILT0H (MMS1, ADDRESS 0x0011)

Bit(s)	Name	Description	Default Value	Type
31	EN	1 = Filter enabled 0 = Filter disabled When set, enables the corresponding Address Filter. ADRF in the MAC Control register (MMS 1, 0x0000 bit 16) shall also be enabled for address filtering to work.	0	RW
30:16	−	Not used	0x0000	RO
15:0	ADDRFILT0[47:32]	Higher order bits of the Filter Address.	0x0000	RW

ADDRESS FILTER LOW 1, ADDRFILT1L (MMS1, ADDRESS 0x0012)

Bit(s)	Name	Description	Default Value	Type
31:0	ADDFILT1[31:0]	Holds the 32 lower order bits of the Address Filter that is spilt into ADDRFILT1L and ADDRFILT1H.	0x00000000	RW

ADDRESS FILTER HIGH 1, ADDRFILT1H (MMS1, ADDRESS 0x0013)

Bit(s)	Name	Description	Default Value	Type
31	EN	1 = Filter enabled 0 = Filter disabled When set, enables the corresponding Address Filter. ADRF in the MAC Control register (MMS1, 0x0000 bit 16) shall also be enabled for address filtering to work.	0	RW
30:16	–	Not used	0x0000	RO
15:0	ADDRFILT1[47:32]	Higher order bits of the Filter Address.	0x0000	RW

ADDRESS FILTER LOW 2, ADDRFILT2L (MMS1, ADDRESS 0x0014)

Bit(s)	Name	Description	Default Value	Type
31:0	ADDFILTL2[31:0]	Holds the 32 lower order bits of the Address Filter that is spilt into ADDRFILT2L and ADDRFILT2H.	0x00000000	RW

ADDRESS FILTER HIGH 2, ADDRFILT2H (MMS1, ADDRESS 0x0015)

Bit(s)	Name	Description	Default Value	Type
31	EN	1 = Filter enabled 0 = Filter disabled When set, enables the corresponding Address. ADRF in the MAC Control register (MMS1, 0x0000 bit 16) shall also be enabled for address filtering to work.	0	RW
30:16	–	Not used	0x0000	RO
15:0	ADDRFILT2[47:32]	Higher order bits of the Filter Address.	0x0000	RW

ADDRESS FILTER LOW 3, ADDRFILT3L (MMS1, ADDRESS 0x0016)

Bit(s)	Name	Description	Default Value	Type
31:0	ADDFILT3[31:0]	Holds the 32 lower order bits of the Address Filter that is spilt into ADDRFILT3L and ADDRFILT3H.	0x00000000	RW

ADDRESS FILTER HIGH 3, ADDRFILT3H (MMS1, ADDRESS 0x0017)

Bit(s)	Name	Description	Default Value	Type
31	EN	1 = Filter enabled 0 = Filter disabled When set, enables the corresponding Address Filter. ADRF in the MAC Control register (MMS1, 0x0000 bit 16) shall also be enabled for address filtering to work.	0	RW
30:16	–	Not used	0x0000	RO
15:0	ADDRFILT3[47:32]	Higher order bits of the Filter Address.	0x0000	RW

ADDRESS MASK LOW 0, ADDRMASK0L (MMS1, ADDRESS 0x0020)

Bit(s)	Name	Description	Default Value	Type
31:0	ADDRMASK0[31:0]	Holds the 32 lower order bits of the Address Filter mask that is spilt into ADDRMASK0L and ADDRMASK0H.	0xFFFFFFFF	RW

ADDRESS MASK HIGH 0, ADDRMASK0H (MMS1, ADDRESS 0x0021)

Bit(s)	Name	Description	Default Value	Type
31:16	–	Not used	0x0000	RO
15:0	ADDRMASK0[47:0]	Higher order bits of the Filter Address Mask.	0xFFFF	RW

ADDRESS MASK LOW 1, ADDRMASK1L (MMS1, ADDRESS 0x0022)

Bit(s)	Name	Description	Default Value	Type
31:0	ADDRMASK1[31:0]	Holds the 32 lower order bits of the Address Filter mask that is spilt into ADDRMASK1L and ADDRMASK1H.	0xFFFFFFFF	RW

ADDRESS MASK HIGH 1, ADDRMASK1H (MMS1, ADDRESS 0x0023)

Bit(s)	Name	Description	Default Value	Type
31:16	–	Not used	0x0000	RO
15:0	ADDRMASK1[47:0]	Higher order bits of the Filter Address Mask.	0xFFFF	RW

ADDRESS MASK LOW 2, ADDRMASK2L (MMS1, ADDRESS 0x0024)

Bit(s)	Name	Description	Default Value	Type
31:0	ADDRMASK2[31:0]	Holds the 32 lower order bits of the Address Filter mask that is spilt into ADDRMASK2L and ADDRMASK2H.	0xFFFFFFFF	RW

ADDRESS MASK HIGH 2, ADDRMASK2H (MMS1, ADDRESS 0x0025)

Bit(s)	Name	Description	Default Value	Type
31:16	–	Not used	0x0000	RO
15:0	ADDRMASK2[47:0]	Higher order bits of the Filter Address Mask.	0xFFFF	RW

ADDRESS MASK LOW 3, ADDRMASK3L (MMS1, ADDRESS 0x0026)

Bit(s)	Name	Description	Default Value	Type
31:0	ADDRMASK3[31:0]	Holds the 32 lower order bits of the Address Filter mask that splits into ADDRMASK3L and ADDRMASK3H.	0xFFFFFFFF	RW

ADDRESS MASK HIGH 3, ADDRMASK3H (MMS1, ADDRESS 0x0027)

Bit(s)	Name	Description	Default Value	Type
31:16	–	Not used	0x0000	RO
15:0	ADDRMASK3[47:0]	Higher order bits of the Filter Address Mask.	0xFFFF	RW

STATISTIC SENT BYTES COUNTER LOW, STOCTETSTXL (MMS1, ADDRESS 0x0030)

Bit(s)	Name	Description	Default Value	Type
31:0	STOCTETSTXL[31:0]	MAC statistic register. STOCTETSXTL holds the 32 low order bits of the cumulative sum of all data bytes sent since the register was last read. Together with the STOCTETSTXH, this register represents the number of transmitted bytes. The bytes comprise the whole frame, from the first byte of the destination address up to (and including) the FCS. Any padding added by the MAC is also counted. If the counter reaches its maximum value of 0xFFFFFFFFFFFF, it wraps to zero. The counter clears when both STOCTETSTXL and STOCTETSTXH are read. NOTE: Internal logic samples the high order bits of the 48−bit counter into the STOCTETSTXH register, every time the STOCTETSTXL register is read. For reading the correct number of bytes transmitted, the host shall read the STOCTETSTXL register first, followed by the STOCTETSTXH register, in that order exactly.	0x00000000	RO−SCR

STATISTIC SENT BYTES COUNTER HIGH, STOCTETSTXH (MMS1, ADDRESS 0x0031)

Bit(s)	Name	Description	Default Value	Type
31:16	–	Not used	0x0000	RO
15:0	STOCTETSTX[47:32]	MAC statistic register. STOCTETSXTH holds the 16 high order bits of the cumulative sum of all data bytes sent since the last read.	0x0000	RO−SCR

STATISTIC FRAMES SENT OK, STFRAMESTXOK (MMS1, ADDRESS 0x0032)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESTXOK	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF and resets to 0 after a read access.	0x0000	RO−SCR

STATISTIC, BROADCAST FRAMES SENT OK, STBCASTTXOK (MMS1, ADDRESS 0x0033)

Bit(s)	Name	Description	Default Value	Type
31:0	STBCASTTXOK	MAC statistic register. Holds the number of broadcast frames (destination address FF:FF:FF:FF:FF:FF) transmitted successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF and resets to 0 after a read access.	0x0000	RO−SCR

STATISTIC, MULTICAST FRAMES SENT OK, STMCASTTXOK (MMS1, ADDRESS 0x0034)

Bit(s)	Name	Description	Default Value	Type
31:0	STMCASTTXOK	MAC statistic register. Holds the number of multicast frames (first bit of destination address set to 1) transmitted successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF and resets to 0 after a read access.	0x0000	RO−SCR

STATISTIC, 64−BYTE FRAMES SENT OK, STFRAMESTX64 (MMS1, ADDRESS 0x0035)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESTX64	MAC statistic register. Holds the number of 64−byte frames transmitted successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 65−BYTE TO 127−BYTE FRAMES SENT OK, STFRAMESTX65 (MMS1, ADDRESS 0x0036)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESTX65	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register, with a size between 65 bytes and 127 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 128−BYTE TO 255−BYTE FRAMES SENT OK, STFRAMESTX128 (MMS1, ADDRESS 0x0037)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESTX128	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register, with a size between 128 bytes and 255 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 256−BYTE TO 511−BYTE FRAMES SENT OK, STFRAMESTX256 (MMS1, ADDRESS 0x0038)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESTX256	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register, with a size between 256 bytes and 511 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 512−BYTE TO 1023−BYTE FRAMES SENT OK, STFRAMESTX512 (MMS1, ADDRESS 0x0039)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESTX512	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register, with a size between 512 bytes and 1023 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

Statistic, 1024−byte to or more frames sent ok, STFRAMESTX1024 (MMS1, Address 0x003A)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESTX1024	MAC statistic register. Holds the number of frames transmitted successfully since the last read of this register, with a size of 1024 bytes or more. This counter does not overflow from its maximum value of 0xFFFFFFFF and is cleared after a read access.	0x0000	RO−SCR

STATISTIC, ABORTED FRAMES DUE TO TX−BUFFER UNDERFLOW, STUNDERFLOW (MMS1, ADDRESS 0x003B)

Bit(s)	Name	Description	Default Value	Type
31:10	−	Not used	0x000000	RO
9:0	STUNDERFLOW	MAC statistic register. Holds the number of frames aborted due to a TX buffer underflow. This can only happen in cut−through mode, if the host does not send frame data fast enough. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x0000	RO−SCR

STATISTIC, FRAMES TRANSMITTED AFTER SINGLE COLLISION, STSINGLECOL (MMS1, ADDRESS 0x003C)

Bit(s)	Name	Description	Default Value	Type
31:18	−	Not used	0x0000	RO
17:0	STSINGLECOL	MAC statistic register. Holds the number of frames transmitted after a single collision event. When PLCA is enabled, the register counts the logical collisions reported by the RS, rather than the actual physical collisions happening on the line. In this case, a non−zero value in SINGLECOL indicates that the PLCA RS is actively arbitrating the line. It does not indicate a problem or degradation of the network performance. To read the actual number of physical collisions on a PLCA enabled network, read the T1SPCSDIAG2 register. This counter does not overflow from its maximum value of 0x0003FFFF. It is cleared after a read access.	0x00000	RO−SCR

STATISTIC, FRAMES TRANSMITTED AFTER MULTIPLE COLLISIONS, STMULITCOL (MMS1, ADDRESS 0x003D)

Bit(s)	Name	Description	Default Value	Type
31:18	–	Not used	0x0000	RO
17:0	STMULTICOL	MAC statistic register. Holds the number of frames transmitted after multiple collision events. When PLCA is enabled, the register should not count any event. Multiple collisions happening on a PLCA enabled network may indicate a misconfiguration of the fundamental parameters (e.g. TO_TIMER), the presence of non−PLCA nodes on the same medium or a defective node on the network. This counter does not overflow from its maximum value of 0x0003FFFF. It is cleared after a read access.	0x00000	RO−SCR

STATISTIC, FRAMES TRANSMITTED AFTER EXCESSIVE COLLISIONS, STEXCESSCOL (MMS1, ADDRESS 0x003E)

Bit(s)	Name	Description	Default Value	Type
31:10	–	Not used	0x000000	RO
9:0	STEXCESSCOL	MAC statistic register. Holds the number of outgoing frames that were aborted because too many collisions happened. When PLCA is enabled, the register should not count any event. Excessive collisions happening on a PLCA enabled network may indicate wrong configuration of fundamental parameters (e.g. TO_TIMER), the presence of non−PLCA nodes on the network or a defective node. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

STATISTIC, FRAMES TRANSMITTED AFTER DEFERRAL, STDEFEEREDTX (MMS1, ADDRESS 0x003F)

Bit(s)	Name	Description	Default Value	Type
31:18	–	Not used	0x0000	RO
17:0	STDEFERREDTX	MAC statistic register. Holds the number of frames transmitted after being deferred. Refer to IEEE802.3 clause 5.2.2 for details. In PLCA enabled networks, deferral is part of the arbitration mechanism. Therefore, a non−zero value in this counter does not indicate degradation of network performance. This counter does not overflow from its maximum value of 0x0003FFFF. It is cleared after a read access.	0x00000	RO−SCR

STATISTIC, COUNTER OF CRS DE−ASSERTION DURING FRAME TRANSMISSION, STCRSERR (MMS1, ADDRESS 0x0040)

Bit(s)	Name	Description	Default Value	Type
31:10	–	Not used	0x0000	RO
9:0	STCRSERR	MAC statistic register. Counts events where carrier indication is de−asserted or not asserted by the PHY during transmission of a frame. A non−zero value in this register may indicate a too high level of noise on the line This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x00000	RO−SCR

STATISTIC RECEIVED BYTES COUNTER LOW, STOCTETSRXL (MMS1, ADDRESS 0x0041)

Bit(s)	Name	Description	Default Value	Type
31:0	STOCTETSRX[31:0]	MAC statistic register. STOCTETSRXL holds the 32 low order bits of the cumulative sum of all data bytes received since the register was last read. Together with the STOCTETSRXH, this register represents the number of received bytes. The bytes comprise the whole frame, from the first byte of the destination address up to (and including) the FCS. If the counter reaches its maximum value of 0xFFFFFFFFFFFF, it wraps to zero. The counter clears when both STOCTETSRXL and STOCTETSRXH have been read. NOTE: internal logic samples the high order bits of the 48−bit counter into the STOCTETSRXH register, every time the STOCTETSRXL register is read. For reading the correct number of bytes received, the host shall read the STOCTETSRXL register first, followed by the STOCTETSRXH register, in that order exactly.	0x00000000	RO−SCR

STATISTIC RECEIVED BYTES COUNTER HIGH, STOCTETSRXH (MMS1, ADDRESS 0x0042)

Bit(s)	Name	Description	Default Value	Type
31:16	−	Not used	0x0000	RO
15:0	STOCTETSRX[47:32]	MAC statistic register. STOCTETSRXH holds the 16 high order bits of the cumulative sum of all data bytes received since the last read.	0x0000	RO−SCR

STATISTIC FRAMES RECEIVED OK, STFRAMESRXOK (MMS1, ADDRESS 0x0043)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESRXOK	MAC statistic register. Holds the number of frames received successfully since last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF, and it is reset after a read access.	0x0000	RO−SCR

STATISTIC, BROADCAST FRAMES RECEIVED OK, STBCASTRXOK (MMS1, ADDRESS 0x0044)

Bit(s)	Name	Description	Default Value	Type
31:0	STBCASTRXOK	MAC statistic register. Holds the number of broadcast frames (destination address FF:FF:FF:FF:FF:FF) received successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF. It resets to 0 after a read access.	0x0000	RO−SCR

STATISTIC, MULTICAST FRAMES RECEIVED OK, STMCASTRXOK (MMS1, ADDRESS 0x0045)

Bit(s)	Name	Description	Default Value	Type
31:0	STMCASTRXOK	MAC statistic register. Holds the number of multicast frames (first bit of destination address set to 1) received successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF. It resets to 0 after a read access.	0x0000	RO−SCR

STATISTIC, 64−BYTE FRAMES RECEIVED OK, STFRAMESRX64 (MMS1, ADDRESS 0x0046)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESRX64	MAC statistic register. Holds the number of 64−byte frames received successfully since the last read of this register. This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 65−BYTE TO 127−BYTE FRAMES RECEIVED OK, STFRAMESTX65 (MMS1, ADDRESS 0x0047)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESRX65	MAC statistic register. Holds the number of frames received successfully since the last read of this register, with a size between 65 bytes and 127 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 128−BYTE TO 255−BYTE FRAMES RECEIVED OK, STFRAMESTX128 (MMS1, ADDRESS 0x0048)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESRX128	MAC statistic register. Holds the number of frames received successfully since the last read of this register, with a size between 128 bytes and 255 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 256−BYTE TO 511−BYTE FRAMES RECEIVED OK, STFRAMESTX256 (MMS1, ADDRESS 0x0049)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESRX256	MAC statistic register. Holds the number of frames received successfully since the last read of this register, with a size between 256 bytes and 511 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 512−BYTE TO 1023−BYTE FRAMES RECEIVED OK, STFRAMESTX512 (MMS1, ADDRESS 0x004A)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESRX512	MAC statistic register. Holds the number of frames received successfully since the last read of this register, with a size between 512 bytes and 1023 bytes. This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x0000	RO−SCR

STATISTIC, 1024−BYTE TO OR MORE FRAMES RECEIVED OK, STFRAMESTX1024 (MMS1, ADDRESS 0x004B)

Bit(s)	Name	Description	Default Value	Type
31:0	STFRAMESRX1024	MAC statistic register. Holds the number of frames received successfully since the last read of this register, with a size of 1024 bytes or more. This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x0000	RO−SCR

STATISTIC, DROPPED TOO SHORT FRAMES STRUNTERR(MMS1, ADDRESS 0x004C)

Bit(s)	Name	Description	Default Value	Type
31:10	−	Not used	0x000000	RO
9:0	STRUNTERR	MAC statistic register. Fragments counter. Holds the number of received frames that were dropped due to their length being shorter than 64 bytes (runt frames). See Clause 4A.4.2 in the IEEE 802.3 specification. Runts are typically triggered by fragments resulting from collisions on CSMA/CD networks but might also indicate poor SNR at the physical layer. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

STATISTIC, DROPPED TOO LONG FRAMES STRXTOOLONG (MMS1, ADDRESS 0x004D)

Bit(s)	Name	Description	Default Value	Type
31:10	–	Not used	0x000000	RO
9:0	STRXTOOLONG	MAC statistic register. Holds the number of received frames that were dropped due to their length being longer than 2000 bytes. This counter does not overflow from its maximum value of 0x000003FF and it is cleared after a read access.	0x000	RO−SCR

STATISTIC, DROPPED FCS ERROR FRAMES STFCSERRS (MMS1, ADDRESS 0x004E)

Bit(s)	Name	Description	Default Value	Type
31:10	–	Not used	0x000000	RO
9:0	STFCSERRS	MAC statistic register. Frame Check Sequence (FCS) error counter. Holds the number of received frames that were dropped due a frame check sequence mismatch. This counter does not overflow from its maximum value of 0x000003FF, and it is cleared after a read access.	0x000	RO−SCR

STATISTIC, SYMBOL ERRORS DURING FRAME RECEPTION, STSYMBOLERRS (MMS1, ADDRESS 0x004F)

Bit(s)	Name	Description	Default Value	Type
31:10	–	Not used	0x000000	RO
9:0	STSYMBOLERRS	MAC statistic register. Holds the number of received frames that were dropped due to the PHY reporting a symbol decoding error. This may be caused by excessive differential noise on the line and may also happen if the remote peer aborted the frame. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

STATISTIC, ALIGN ERRORS DURING FRAME RECEPTION, STALIGNERRS (MMS1, ADDRESS 0x0050)

Bit(s)	Name	Description	Default Value	Type
31:10	–	Not used	0x000000	RO
9:0	STALIGNERRS	MAC statistic register. Holds the number of received frames that were dropped because their size was not byte−aligned. This may be caused by excessive differential noise on the line or collisions when PLCA is not enabled. This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

STATISTIC, RX BUFFER OVERFLOW ERRORS, STRXOVERFLOW (MMS1, ADDRESS 0x0051)

Bit(s)	Name	Description	Default Value	Type
31:10	–	Not used	0x000000	RO
9:0	STRXOVERFLOW	MAC statistic register. Holds the number of received frames that were aborted because the host failed to retrieve data at a sufficient rate, causing the RX buffer to overflow. Note that such aborted frames are still counted as “received successfully” at the MAC layer (and other statistic registers). This counter does not overflow from its maximum value of 0x000003FF. It is cleared after a read access.	0x000	RO−SCR

STATISTIC, RX DROPPED FRAME COUNT, STRXDROPPED (MMS1, ADDRESS 0x0052)

Bit(s)	Name	Description	Default Value	Type
31:0	STRXDROPPED	MAC statistic register. Holds the number of received frames that were successfully received, but dropped because of address filtering. Dropped frames include frames that did not pass the checks against ADDRFILTx/ADDRMASKx, broadcast frames filtered by the BCSF bit stetting and multicast frames filtered by the MCSF bit setting in the MAC control register (MMS 1, 0x0000). Note that such frames are still counted as ”received successfully” at the MAC layer (and other statistic registers). This counter does not overflow from its maximum value of 0xFFFFFFFF. It is cleared after a read access.	0x00000000	RO−SCR

MMS2 Registers

Memory Map Selection 2 contains a direct mapping of Clause 45 MMD 3 PHY−PCS registers implemented in the NCN26010 device.

While register access though the SPI interface is always 32 bit, all MMS2 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes.

DEVICES IN PACKAGE 1 REGISTER (MMS2, ADDRESS 0x0005)

Bit(s)	Name	Description	Default Value	Type
15:4	−	Always reads 0	0x000	RO
3	PCS Present	Always reads 1 Indicating that the device contains the PCS.	1	RO
2	−	Always reads 0	0	RO
1	PMA Present	Always reads 1 Indicating that the device contains the PMA.	1	RO
0	Clause 22 Registers Present	Always reads 1 Indicating that the device contains Clause 22 standard registers.	1	RO

DEVICES IN PACKAGE 2 REGISTER (MMS2, ADDRESS 0x0006)

Bit(s)	Name	Description	Default Value	Type
15:0	−	Always reads 0	0x0000	RO

10BASE−T1S PCS CONTROL REGISTER (MMS2, ADDRESS 0x08F3)

Bit(s)	Name	Description	Default Value	Type
15	PCS Reset	1 = PCS reset 0 = normal operation Setting this bit to 1 sets all 10BASE−T1S PCS registers to their default state. This may change the internal state of the PHY's PCS and the state of the physical link. Setting this bit causes the PCS and the PMA PHY layers to reset.	0	RW SC
14	Loopback	1 = Loopback enabled 0 = Loopback disabled When enabled, data sent by the MAC is looped back, traversing PCS TX and PCS RX. This allows testing of the 4B/5B encoder/decoder and the PCS TX/RX state machines / scrambler.	0	RW
13:0	−	Always reads 0	0	RO

10BASE−T1S PCS STATUS REGISTER (MMS2, ADDRESS 0x08F4)

Bit(s)	Name	Description	Default Value	Type
15:8	−	Always reads 0	0	RO
7	Fault	1 = Fault condition detected 0 = No fault condition detected If this bit reads 1, the PCS inside the NCN26010 has detected a jabber fault condition. This can either be a local or a remote fault condition. Fault is latched until read. Self−clears on read.	−	RO−LH
6:0	−	Always reads 0	0	RO

10BASE−T1S PCS DIAGNOSTICS REGISTER 1 (MMS2, ADDRESS 0x08F5)

Bit(s)	Name	Description	Default Value	Type
15:0	PCS Remote Jabber Count	Counts the number of detected remote jabber events since this register was last read. For details, see IEEE802.3 Clause 45 MMD3 address 2293. If the count reaches 0xFFFF, no more errors are counted to prevent the counter from overflowing.	0	RO−SC

10BASE−T1S PCS DIAGNOSTICS REGISTER 2 (MMS2, ADDRESS 0x08F6)

Bit(s)	Name	Description	Default Value	Type
15:0	PCS Physical Collisions Count	Counts the number of physical collision events detected by the PHY since this register was last read. If the count reaches 0xFFFF, no more errors are counted to prevent the counter from overflowing. NOTE: Physical collisions are caused by the superposition of signals transmitted simultaneously by more than one station on the same medium. In contrast to physical collisions, logical collisions in PLCA mode are triggered by the PCLA RS arbitration algorithm.	0	RO−SC

MMS3 Registers

Memory Map Selection 3 contains a direct mapping of Clause 45 MMD 3 PHY−PCS registers implemented in the NCN26010 device.

All MMS3 registers ar16−bit registers.

DEVICES IN PACKAGE 1 REGISTER (MMS3, ADDRESS 0x0005)

Bit(s)	Name	Description	Default Value	Type
15:4	−	Always reads 0	0	RO
3	PCS Present	Always returns 1 Indicating that the device contains the PCS.	1	RO
2	−	Always returns 0	0	RO
1	PMA Present	Always returns 1 Indicating that the device contains the PMA.	1	RO
0	Clause 22 Registers Present	Always returns 1 Indicating that the device contains Clause 22 standard registers.	1	RO

DEVICES IN PACKAGE 2 REGISTER (MMS3, ADDRESS 0x0006)

Bit(s)	Name	Description	Default Value	Type
15:0	−	Always reads 0	0x0000	RO

BASE−T1 EXTENDED ABILITY REGISTER (MMS3, ADDRESS 0x0012)

Bit(s)	Name	Description	Default Value	Type
15:4	−	Always reads 0	0	RO
3	10BASE−T1S	Always reads 1 This is a 10BASE−T1S only device.	1	RO
2:0	−	Always reads 0	0	RO

10BASE−T1S PMA CONTROL REGISTER (MMS3, ADDRESS 0x08F9)

Bit(s)	Name	Description	Default Value	Type
15	PMA Reset	Alias of Clause 22 bit 0.15 and MII Control Register bit 15 Soft Reset Setting this bit to one triggers a soft reset of the NCN26010. This bit self−clears when the reset finishes.	0	RW−SC
14	Transmit Disable	1 = disable Transmit 0 = enable Transmit When set, the embedded PHY transmitter is shut down and TX requests from the MAC (SPI) are ignored.	0	RW
13:12	−	Always reads 0	0	RO
11	Low Power Mode	Not implemented	0	RO
10	Multi−Drop Enable	Always reads 1 This NCN26010 is a multi−drop only device.	1	RO
9:1	−	Always reads 0	0	RO
0	Loopback Mode	Same as Clause 22 bit 0.14 and MIIM control register MMS1, address 0xFF00, bit 14.	0	RW

10BASE−T1S PMA STATUS REGISTER (MMS3, ADDRESS 0x08FA)

Bit(s)	Name	Description	Default Value	Type
15:14	−	Always reads 0	0	RO
13	Loopback Ability	Always reads 1, indicating the PHY supports loopback.	1	RO
12	−	Always reads 0	0	RO
11	Low Power Ability	Always reads 0 The PHY does not support Low Power Mode.	0	RO
10	Multi−Drop Ability	Always reads 1 This NCN26010 supports half duplex multi−drop operation.	1	RO
9	Receive Fault Ability	Always reads 1 The PHY supports receive fault detection.	1	RO
8:2	−	Always reads 0	0	RO
1	Remote Jabber	Copy of Clause 22 Register 1.4 and MIIM Status register, MMS1, Address 0xFF01, bit 4. Auto clear to zero on read. See the MIIM Status register for description.	0	RO−LH
0	−	Always reads 0	0	RO

10BASE−T1S TEST MODE CONTROL REGISTER (MMS3, ADDRESS 0x08FB)

Bit(s)	Name	Description		Default Value	Type
15:13	Test Mode	Test mode in accordance with IEEE802.3cg. Default is normal operation		000	RW
		Pattern	**Test Mode**		
		000	Normal Operation		
		001	Transmitter Output Voltage test		
		010	Transmitter Output Droop test		
		011	Transmitter PSD mask test		
		100	Transmitter high Impedance test		
		101	Reserved		
		110	Reserved		
		111	Reserved		
12:0	−	Always reads 0		0	R

MMS4 Registers

Memory Map Selection 4 contains a direct mapping of Clause 45 MMD 31 PLCA and vendor specific PHY registers implemented in the NCN26010 device.

All MMS4 registers are 16−bit registers.

CHIP REVISION REGISTER (MMS4, ADDRESS 0x8000)

Bit(s)	Name	Description	Default Value	Type
15:12	Major Revision	Major release number	0b00001	R
11:8	Minor Revision	Minor release number	0b0000	R
7:6	Stage	Maturity level − Stable	0b11	R
5:0	Patch	Patch level build number	0b000001	R

PHY CONFIGURATION 1 REGISTER (MMS4, ADDRESS 0x8001)

The PHY configuration 1 register allows using non−IEEE802.3 compliant operation modes that can help with debugging and increased performance in noisy environments. Note that these setting should be used with care as they might result in a network configuration that prohibits successful communication.

Bit(s)	Name	Description	Default Value	Type
15	Reserved	Reserved	0	R/W
14:8	Not Used	−	0x00	R
7	Enhanced Noise Immunity	1 = Enhanced noise immunity enabled 0 = Enhanced noise immunity disabled Enhanced Noise Immunity (ENI) mode allows extending the PHY noise immunity to values above the IEEE 802.3cg defined noise levels, allowing the device to withstand industry standard immunity tests. ENI mode changes the way the PHY detects a carrier to overcome false carrier detection when noise on the line roughly exceeds 220 mV_{pp}. Instead of relying solely on energy detection, the PMA further qualifies carrier detection by detecting a valid manchester coding, thus rejecting in−band noise. While this is a non standard feature, ENI is interoperable with full PLCA−enabled networks. In this case, immunity can can be further improved by disabling physical collision detection.	0	R/W
6	Unjab Timer Enable	1 = Unjab Timer enabled 0 = Unjab Timer disabled Setting this bit enables automatic recovery from PCS TX jabbers after the Unjab timer expired and the jabber condition is over. See Clause 147.3.2 of the IEEE802.3cg specification for more details.	0	R/W
5:3	Not used	−	0x0	R
2	Scrambler Disable	1 = PCS scrambling disabled 0 = PCS scrambling enabled When set, the PCS scrambling function is disabled and the 4B data is sent unaltered to the 4B/5B and DME encoders. In addition, data received from the line is not de−scrambled after the 5B/4B conversion. This is a debug feature not intended for normal operation.	0	R/W
1	No Collision Masking	1 = ENI collision detection masking disabled 0 = ENI collision detection masking enabled If set, this bit prevents masking of physical collision detection when Enhanced Noise Immunity (ENI) mode is enabled	1	R/W
0	RX Delay	1 = enable additional delay in the RX data path 0 = additional RX delay disabled Setting this bit enables an additional RX data path delay of 14 MII clock cycles. For NCN26010, this should always be set to 0 for improving performance. NOTE: Although the default is 1, this bit can be set to 0 to decrease the RX latency by approximately 5.6 μs.	1	R/W

PLCA EXTENSIONS REGISTER (MMS4, ADDRESS 0x8002)

Bit(s)	Name	Description	Default Value	Type
15	PLCA Precedence	1 = Precedence Mode enabled 0 = Precedence Mode disabled While in Precedence Mode, the PLCA Reconciliation Sublayer implicitly terminates a cycle at each transmitted or received packet, causing the network to behave more like a CAN network where nodes with lower local node IDs get strict precedence over nodes with higher PLCA IDs. With strict precedence, a node could transmit for indefinite time without being interrupted. Depending on how the network is engineered, nodes with higher PLCA IDs are subject to starvation (as they might never get permission to transmit). Note that all nodes shall support precedence mode for this feature to work, and that precedence mode is not interoperable with standard PLCA.	0	R/W
14:12	Not Used	–	0x0	R
11	Reserved	Read / Write accesses to this bit have no effect on the NCN61010.	1	R/W
10:2	Not Used	–	0x00	R
1	Coordinator Mode	1 = Coordinator Mode enabled 0 = Coordinator Mode disabled When enabled the NCN26010 Coordinator role is determined by the Coordinator bit setting in this register. When disabled, the NCN26010 takes the PLCA coordinator role if its PLCA ID is set to 0 in the PLCA Control 1 register.	0	R/W
0	Coordinator Role	1 = PHY is PLCA coordinator 0 = PHY is PLCA node When the Coordinator Mode bit in this register is set to 1, and the Coordinator Role is also set to 1, the PLCA RS takes the coordinator role, regardless of the configured PLCA ID.	0	R/W

PMA TUNE 0 REGISTER (MMS4, ADDRESS0x8003)

This register allows fine−tuning of the NCN26010 line receiver when ENI mode is enabled.

WARNING: Changing the setting from their default should only be considered by experienced users at their own risk. Invalid settings may lead to unexpected link down and corrupted Ethernet frames.

<table>
<tr><th>Bit(s)</th><th>Name</th><th colspan="2">Description</th><th>Default Value</th><th>Type</th></tr>
<tr><td>15:14</td><td>Not Used</td><td colspan="2">–</td><td>0x0</td><td>R</td></tr>
<tr><td>13:8</td><td>PLCA Beacon Detection Threshold</td><td colspan="2">This field selects the threshold level for the PLCA Beacon (NN*) detection in the PMA when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduces the noise tolerance. Lower values achieve the opposite effect.</td><td>0x20</td><td>R/W</td></tr>
<tr><td>7:3</td><td>Not Used</td><td colspan="2">–</td><td>0x0</td><td>R</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">Drift Compensation Window Selection</td><td colspan="2">Selects the size of the integration window for the clock drift compensator inside the RX PMA when ENI mode is enabled. A lower value allows for compensation of higher clock drifts at the expense of jitter rejection. Higher values achieve the opposite effect.</td><td rowspan="10">0x5</td><td rowspan="10">R/W</td></tr>
<tr><td>Window Selection Value</td><td>Integration Window Size</td></tr>
<tr><td>0</td><td>reserved</td></tr>
<tr><td>1</td><td>reserved</td></tr>
<tr><td>2</td><td>31 bit times</td></tr>
<tr><td>3</td><td>63 bit times</td></tr>
<tr><td>4</td><td>127 bit times</td></tr>
<tr><td>5</td><td>optimized default</td></tr>
<tr><td>6</td><td>reserved</td></tr>
<tr><td>7</td><td>reserved</td></tr>
</table>

PMA TUNE 1 REGISTER (MMS4, ADDRESS 0x8004)

This register allows fine−tuning of the NCN26010 line receiver.

WARNING: Changing the setting from their default should only be considered by experienced users at their own risk. Invalid setting may lead to unexpected link down and dropped or corrupted Ethernet frames.

Bit(s)	Name	Description	Default Value	Type
15:14	Not Used	–	0x0	R
13:8	Packet Preamble Detection Threshold	Sets the threshold level for the packet preamble (JJHH) detection in the PMA RX when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduce the noise tolerance. Lower values achieve the opposite effect.	0x35	R/W
7:6	Not Used	–	0x0	R
5:0	Commit Detection Threshold	Sets the threshold for the Commit (JJ) detection of the PMA RX when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduce the noise tolerance. Lower values achieve the opposite effect.	0x20	R/W

PLCA REGISTER MAP AND IDENTIFICATION REGISTER, PLCIDVER (MMS4, ADDRESS 0xCA00)

Bit(s)	Name	Description	Default Value	Type
15:8	PLCA Memory Map Identifier MAPID	Indicates compatibility with the OPEN Alliance PLCA memory map definition.	0x0A	RO
7:0	PLCA Memory Map Version MAPVER	Indicates the version of the OPEN Alliance memory map definition the NCN26010 device adheres to.	0x10	R0

PLCA CONTROL 0 REGISTER, PLCACTRL0 (MMS4, ADDRESS 0xCA01)

Bit(s)	Name	Description	Default Value	Type
15	PCLA Enable	1 = PCLA enabled 0 = PCLA disabled When enabled, the PCLA RS functions are switched on. Otherwise, the PHY operates in CSMA/CD half−duplex mode.	0	R/W
14	PLCA Reset	1 = PLCA reset 0 = normal operation When set, the PLCA RS is reset to its initial state. This will also reset the PCS and PMA layers. The NCN26010 registers are not altered by this reset. Upon PCLA reset, this bit is cleared	0	R/W SC
13:0	–	Always reads 0	All 0	R

PLCA CONTROL 1 REGISTER, PLCACTRL1 (MMS4, ADDRESS 0xCA02)

Bit(s)	Name	Description	Default Value	Type
15:8	PCLA Node Count NCNT	Configures the number of transmit opportunities generated in a PLCA cycle. This parameter is only meaningful when the embedded PHY is operating as the coordinator node in a PLCA enabled network.	0x08	RW
7:0	PLCA Local Node ID ID	Set the PHY's local node ID in a PLCA enabled network. This number shall be less than or equal to the PLCA node count (see bits 15:8) of the PLCA coordinator node. When set to 0x0, the PHY acts as PLCA coordinator unless coordinator mode is enabled. Note that the default value of 0xFF disables the PLCA function.	0xFF	RW

PLCA STATUS REGISTER, PLCASTATUS (MMS4, ADDRESS 0xCA03)

Bit(s)	Name	Description	Default Value	Type
15	Beacon TX / RX Status PST	When one, this bit indicates that the PLCA RS is receiving / transmitting the BEACON. Note that only the coordinator node transmits the BEACON. When this bit reads 0, the PHY is not ready to send or receive data in PLCA mode. This could also be interpreted as an indicator of PLCA activity on the line.	–	RO
14:0	–	Always reads 0	0x0000	RO

PLCA TRANSMIT OPPORTUNITY TIMER REGISTER, PLCATOTMR (MMS4, ADDRESS 0xCA04)

Bit(s)	Name	Description	Default Value	Type
15:8	–	Always reads 0	0x00	RO
7:0	Transmit Opportunity Timer TOTMR	Defines the minimum duration, in bit time, of the PLCA transmit opportunity timer as described in the OPEN Alliance PLCA registers specification. The default value is 24BT (2.4 μs). Larger values allow for extending the maximum reach of the mixing segment, while lower values improve performance by reducing the overall unused TO time. See IEEE802.3cg Clause 30 and Clause 147 for a detailed description. This parameter shall be set to the same value across all nodes sharing the same media.	0x18	RW

PLCA BURST MODE REGISTER, PLCABURST (MMS4, ADDRESS 0xCA05)

Bit(s)	Name	Description	Default Value	Type
15:8	Maximum Burst Count MAXBC	Sets the number of **additional** Ethernet frames that may be transmitted during a single transmit opportunity. The default value allows only one frame to be sent per transmit opportunity. See IEEE802.3cg Clause 148.4.4.2 for more details	0x00	R/W
7:0	Inter Frame Gap Compensation Timer BTMR	Sets the number of bit times that the PLCA RS waits for the MAC to send a frame, after CRS is de−asserted. The default of 128 includes the minimum inter−frame gap of 96 bits as defined in IEEE802.3 Clause 4.4.2, plus additional margin. Can be used to fine tune the burst performance	0x80	R/W

MMS12 Registers

Memory Map Selection 12 contains a direct mapping of Clause 45 MMD 30 vendor specific registers implemented in the NCN26010 device.

All MMS12 registers are 16−bit registers.

MIIM IRQ CONTROL REGISTER (MMS12, ADDRESS 0x0010)

Bit(s)	Name	Description	Default Value	Type
15:6	No Used	Not used	0x000	R
5	Physical Collision Report	1 = PHYINT on Physical Collision enabled 0 = PHYINT on Physical Collision disabled If enabled, a PHYINT event is issued every time a physical collision is detected.	0	R/W
4	PLCA Recovery Report	1 = PHYINT on PLCA Recovery enabled 0 = PHYINT on PLCA Recovery disabled When enabled, a PHYINT is issued on every PLCA Recovery event. PLCA recovery is flagged when a false carrier event (e.g. impulse noise) occurs on the line. When a CRS event is not followed by the reception of a packet within a certain amount of time the embedded PHY goes to either of two states, depending on its PLCA settings: When configured as coordinator node, the PHY waits for the line to be quiet for a certain amount of time and then sends a new BEACON. When not configured as a coordinator node, the PHY will wait for a BEACON before getting a new transmit opportunity.	0	R/W
3	Remote Jabber Report	1 = PHYINT on Remote Jabber enabled 0 = PHYINT on Remote Jabber disabled When enabled, a PHYINT is issued every time the embedded PHY detects a remote jabber condition. A remote jabber condition occurs if a station transmits for longer than a maximum length Ethernet frame transmit duration (2000 bytes, including FCS).	0	R/W
2	Local Jabber Report	1 = PHYINT on Local Jabber enabled 0 = PHYINT on Local Jabber disabled When enabled, a PHYINT event is asserted when the NCN26010 detects a local jabber condition.	0	R/W
1	PLCA Status Change Report	1 = PHYINT on change of PLCA Status 0 = no PHYINT on change of PLCA Status When enabled, the device issues a PHYINT every time the PLCA Status changes. To determine the actual PLCA status, the host interrupt service routine would have to read the PLCA Status Register, PLCASTATUS (MMS4, Address 0xCA03).	0	R/W
0	Link Stats Change Report	1 = PHYINT on change of Link Status enabled 0 = PHYINT on change of Link Status disabled When enabled, a PHYINT event is issued every time the link status changed. The actual link status can be read from the Link Status bit (0.2) in the PHY Status register MMS 0, Address 0xFF01.	0	R/W

5. Note in this table PHYINT is refered to as an interrup request internal to the NCN26010 device and not the IRQn pin on the device. The difference is that the PHYINT can be masked and shall be acknowledged separately.

MIIM IRQ STATUS REGISTER (MMS12, ADDRESS 0x0011)

Whenever an IRQ occurs, the user should read this register to determine the source of the interrupt. All the bits latch high and self−clear on read of this register.

Bit(s)	Name	Description	Default Value	Type
15	Reset Status	This bit is set at Power−On−Reset or any other form of hardware reset. Its purpose is to notify the host of a possibly unsolicited system reset. When set, it does not generate an interrupt. Once cleared, it cannot be set. The bit can be cleared by writing a “1” to it.	0	RC−SCW1
14:6	No Used	Not used	0x000	
5	Physical Collision	A one indicates that the last IRQ was issued due to a Physical collision on the line.	0	R LH−SC
4	PLCA Recovery	A one indicates that the last IRQ was issued by the PHY due to a PLCA Recovery condition.	0	R LH−SC
3	Remote Jabber	A one indicates that the last IRQ was issued by the PHY due to detecting a remote jabber fault	0	R LH−SC
2	Local Jabber	A one indicates that the last IRQ was issued by the PHY due to detecting a remote jabber fault	0	R LH−SC
1	PLCA Status Change	A one indicates that the last IRQ was issued due to a change in PLCA status. To determine the actual PLCA status the hosts interrupt service routine would have to read the PLCA Status Register, PLCASTATUS (MMS4, Address 0xCA03) at MMS 4, Address 51715 (0xCA03).	0	R LH−SC
0	Link Stats Change	A one indicates that the last IRQ was issued due to a change in the Link Status. The actual link status can be read from the Link Status bit (0.2) in the PHY Status register MMS 0, Address 0xFF01.	0	R LH−SC

DIO CONFIGURATION REGISTER (MMS12, ADDRESS 0x0012)

The DIO configuration register sets the function of the General Purpose I/O pins DIO1 and DIO0.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Default Value</th><th>Type</th></tr>
<tr><td>15</td><td>Slew Rate 1</td><td>1 = slow
0 = fast
Sets the slew rate of the DIO1 output.</td><td>0</td><td>R/W</td></tr>
<tr><td>14</td><td>Pull Enable 1</td><td>1= enabled
0 = disabled
When enabled, DIO1 is programed to provide an internal pull−up or pull−down resistor, depending on bit 13 of this register.</td><td>1</td><td>R/W</td></tr>
<tr><td>13</td><td>Pull Resistor Type 1</td><td>1 = Pull Down
0 = Pull Up
Sets the type of the internal pull when bit 14 is set.</td><td>0</td><td>R/W</td></tr>
<tr><td>12:9</td><td>FN1[3:0]</td><td>Selects the function of the DIO 1 pin. See table for FNx below.</td><td>0</td><td>R/W</td></tr>
<tr><td>8</td><td>VAL1</td><td>Sets the output value of DIO1 when FN1[3:0] is set to GPIO function.
It sets the polarity (1 = active high, 0 = active low) for all other modes.</td><td>0</td><td>R/W</td></tr>
<tr><td>7</td><td>Slew Rate 0</td><td>1 = slow
0 = fast
Sets the slew rate of the DIO0 output.</td><td>0</td><td>R/W</td></tr>
<tr><td>6</td><td>Pull Enable 0</td><td>1 = enabled
0 = disabled
When enabled, DIO0 is programed to provide an internal pull−up or pull−down resistor, depending on bit 5.</td><td>1</td><td>R/W</td></tr>
<tr><td>5</td><td>Pull Resistor Type 0</td><td>1 = Pull Down
0 = Pull Up
Sets the type of the internal pull when bit 6 is enabled.</td><td>1</td><td>R/W</td></tr>
<tr><td>4:1</td><td>FN0[3:0]</td><td>Selects the function of the DIO0 pin. See table for FNx
<table>
<tr><th>FNx[3:0]</th><th>Function</th><th>Description</th></tr>
<tr><td>0x0</td><td>Disable</td><td>DIOx is set to high−impedance (default)</td></tr>
<tr><td>0x1</td><td>GPIO (output)</td><td>Output value is set after VALx</td></tr>
<tr><td>0x2</td><td>SFD−TX</td><td>Generates a pulse at SFD transmission. VALx sets the pulse polarity.</td></tr>
<tr><td>0x3</td><td>SFD−RX</td><td>Generates a pulse when SFD is detected during RX. VALx sets the pulse polarity. (Note 6)</td></tr>
<tr><td>0x4</td><td>LED Link Control</td><td>Pin drives a LED when port is enabled and link status is up</td></tr>
<tr><td>0x5</td><td>LED PLCA Status</td><td>Pin drives a LED when PLCA status is up</td></tr>
<tr><td>0x6</td><td>LED TX</td><td>LED indicating TX activity</td></tr>
<tr><td>0x7</td><td>LED RX</td><td>LED indicating RX activity. (Note 6)</td></tr>
<tr><td>0x8</td><td>CLK25M</td><td>Output 25 MHz clock</td></tr>
<tr><td>0x9 − 0xA</td><td>Reserved</td><td>Don’t use</td></tr>
<tr><td>0xB</td><td>SFD− RX&TX</td><td>Pulse on DIOx at SFD (RX or TX), VALx sets the polarity of the pulse</td></tr>
<tr><td>0xC − 0xE</td><td>Reserved</td><td>Don’t use</td></tr>
<tr><td>0xF</td><td>LED TX&RX</td><td>LED indicating TX and RX activity</td></tr>
</table></td><td>0x0</td><td>R/W</td></tr>
<tr><td>0</td><td>VAL0</td><td>Sets the output value of DIO0 when FN0[3:0] is set to GPIO function.
It sets the polarity (1 = active high, 0 = active low) for all other modes.</td><td>0</td><td>R/W</td></tr>
</table>

6. Also triggers on TX.

PHY TWEAKS REGISTER (MMS12, ADDRESS 0x1001)

The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected and do not need modification under normal conditions.

Bit(s)	Name	Description	Default Value	Type
15:14	TX Gain	Specifies the Transmitter Amplitude gain.	0b00	R/W

TX Gain	TX Amplitude (mV_{pp})
0b00	1000
0b01	1100
0b10	900
0b11	800

NOTE: This is an advanced configuration register. It is recommended to consult with **onsemi** before changing the value from its default settings.

Bit(s)	Name	Description	Default Value	Type
13:10	RX CD Threshold	Specifies the RX Collision Detection threshold level. R $RX_{CD_Treshold} = 150\ mV + 50\ mV_{pp} * RX_CD$	0xB	R/W

RX CD	Threshold Level [mV_{pp}]
0	150
1	200
2	250
3	300
4	350
5	400
6	450
7	500
8	550
9	600
10	650
11	700 (default)
12	750
13	800
14	850
15	900

NOTE: This is an advanced configuration register. It is recommended to consult with **onsemi** before changing the value from its default settings.

Bit(s)	Name	Description	Default Value	Type
9:6	RX_ED Threshold	Specifies the RX energy detection threshold level following this equation $RX_{ED_Treshold} = 150\ mV + 50\ mV_{pp} * RX_ED$	0x2	R/W

RX_ED	ED Threshold Level (mV_{pp})
0	150
1	200
2	250 (default)
3	300
4	350
5	400
6	450
7	500

PHY TWEAKS REGISTER (MMS12, ADDRESS 0x1001) (continued)
The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected and do not need modification under normal conditions.

Bit(s)	Name	Description		Default Value	Type
		8	550		
		9	600		
		10	650		
		11	700		
		12	750		
		13	800		
		14	850		
		15	900		
		NOTE: This is an advanced configuration register. It is recommended to consult with **onsemi** before changing the value from its default settings.			
5	Digital Slew Rate	0 = slow 1 = fast (default) Sets the output slew rate of the all digital I/Os, excluding DIO0 and DIO1. Setting the slew rate to “fast” might improve signal integrity when driving higher capacitive loads, but yields the opposite effect in low capacitive load scenarios.		1	R/W
4:3	CMC Compensation	In case a common mode choke is used on the line, these bits can be set to compensate for the added common−mode choke resistance:		0	R/W
		CMC	**CMC Typical Series Resistance (Ω)**		
		0b00	0 – 0.5 (default)		
		0b01	0.5 – 2−25		
		0b10	2.25 – 3.75		
		0b11	3.75 – 5		
2	TX Slew	0 = slow 1 = fast This sets the slew rate of the TX line driver output. Setting this to “slow” can help improve EMC performance but may have a negative effect on return loss.		0	RW
1	Not Used	–		0	R
0	CLK Out Enable	1 = enabled (default) 0 = disabled When enabled, the PHY’s internal 25 MHz clock is output at CLKO. When disabled, the CLKO pin drives a logic low level.		1	R/W

MACID0 (MMS12, ADDRESS 0x1002)

Bit(s)	Name	Description	Default Value	Type
15:0	MACID [15:0]	Lower 16 bit of the unique MAC address. Together with the upper 8 bits in the MACID1 register, and the OUI from IDVER (MMS0, address 0x0000, bits 31:10), it forms a unique MAC address for the NCN26010 device. Note that no Address Filter is pre−initialized with that MAC address. The user should read MACID0, MACID1 and OUI (from IDVER) to initialize the address filters. The host may also need to use the MAC address as the source address in Ethernet frames sent to the NCN26010.	–	RO

MACID1 (MMS12, ADDRESS 0x1003)

Bit(s)	Name	Description	Default Value	Type
15:8	–	Not used	–	RO
7:0	MACID[23:16]	Upper 8 bits of the MAC address. See description in MACID0 for details.	–	RW

CHIP INFO REGISTER (MMS12, ADDRESS 0x1004)

Bit(s)	Name	Description	Default Value	Type
15	Not Used		0	R
14:8	Wafer_Y	Y position on the Wafer from where the part was picked.	–	R
7	Not Used		0	R
6:0	Wafer_X	X position on the Wafer from where the part was picked.	–	R

NVM HEALTH REGISTER (MMS12, ADDRESS 0x1005)

This register reports if there are errors in the factory configuration data set by **onsemi** during manufacturing of the NCN26010.
There are three different zones for the configuration data stored inside the devices non−volatile memory:

Zone	Description
Green	Manufacturing related data Errors in this zone do not cause any failure or misbehavior in the application.
Yellow	Functional Data: MAC and OUI Corrupted data in this area does not cause the part to malfunction, but a host relying on the information stored herein might not initialize its drivers correctly. However, countermeasures taken in the host's software could be used to fall back to a state where operation is still possible.
Red	Configuration data Data corruption in this area could render the part unusable. With factory configuration not being correct, it cannot be guaranteed that the part will operate within the limits required by specifications.

Note that the configuration memory cannot be written by the user, so corrupted data cannot be recovered.
The configuration memory is protected by an ECC scheme that allows the correction of single bit error and the detection of double bit errors. With this feature, a single bit error (SBERR) can be considered a warning, while a reported double bit error shall be interpreted as an error impairing the function of the part (partially or entirely), depending on the zone in which it appears.

Bit(s)	Name	Description	Default Value	Type
15	Red Zone NVM Warning	When this bit reads as one, the ECC controller for the configuration memory has detected a single bit error in the red zone. As single bit errors are corrected by the ECC controller, this is just a warning. The NCN26010 remains fully functional	0	R
14	Red Zone NVM Error	When 1, the ECC controller detected at least two unrecoverable bit errors in the red zone of the configuration memory. This shall be treated as an error, therefore correct functionality is not guaranteed. The part might still operate with degraded performance.	0	R
13	Yellow Zone NVM Warning	When 1, the ECC controller detected and corrected a single bit error in the yellow zone of the configuration memory. Full functionality is still granted.	0	R
12	Yellow Zone NVM Error	When 1, the ECC controller detected at least two unrecoverable bit errors in the yellow zone of the configuration memory. While this is an error invalidating the content of the OUI and the MAC ID, the NCN26010 still functions as an Ethernet MACPHY in accordance to specifications.	0	R
11	Green Zone NVM Warning	When 1, the ECC controller detected and corrected a single bit error in the green zone of the trim and configuration memory. Full functionality is still granted.	0	R
10	Green Zone NVM Error	When 1, the ECC controller detected at least two unrecoverable bit errors in the green zone of the configuration memory. As the green zone contains manufacturing and tracing information, the NCN26010 functionality is not affected. However, a part with this error loses its manufacturing traceability.	0	R
9:0	Reserved	Reserved for manufacturing purposes.	–	R

Applications Information

Clock Source

The NCN26010 requires a precise and robust 25 MHz clock source for correct operation.

The clock can either be fed from an external 25 MHz clock source, or be generated using a quartz crystal connected to the XTAL Oscillator circuit of the NCN26010.

Crystal Oscillator

The oscillator circuit is designed to drive a 25 MHz parallel resonance AT cut quartz crystal. The external crystal shall be connected between the XI pin and the XO pin. XI is the input pin and XO is the output pin of the internal crystal oscillator circuit.

A typical crystal connection circuit is shown in Figure 5.

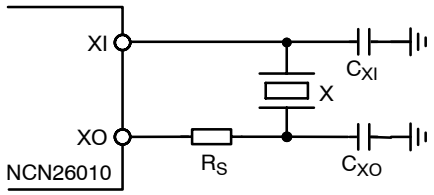


Figure 5. Crystal Connection Diagram

External Clock Source

In situations where a 25 MHz (±100 ppm) clock signal is already available in the system, the NCN26010 can be clocked using that signal, removing the need of adding a crystal and load capacitors. In this case, the external clock signal shall be connected to the XI pin of the NCN26010, while the XO pin shall be left floating.

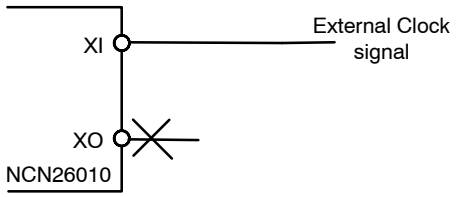


Figure 6. Connecting an External Clock Source

Clock Output

The NCN26010 also offers a dedicated output pin that can provide a stable 25 MHz clock to other components (like MCUs) on the same PCB. The CLKO pin offers that function at 3.3 V or 2.5 V LVCMOS levels depending on VDDIO.

Device Configuration Examples

To configure the NCN26010, configuration registers (see memory map) can be set using SPI commands following the OPEN Alliance TC6 10BASE−T1x (see OPEN specs) serial communication protocol.

Please see the “OPEN Alliance 10BASE−T1x MACPHY Serial Interface” specification section 7.4, available at https://www.opensig.com, for details.

Basic Configuration for CSMA/CD Operation

To connect the NCN26010 device to a 10BASE−T1S multi drop network in CSMA/CD mode of operation, a few writes to control registers are required. This requires configuring the MAC and the PHY functions inside the device and finally set the SPI protocol to enable the exchange of Ethernet frames between the MACPHY and the connected SPI master.

Minimal configuration example:

1. Issue a device reset by writing 0x00000001 into Reset Control and Status, RESET (MMS0, Address 0x0003)
2. In the MAC CONFIG0 register at MMS1, Address 0x0000, set the following bits:
   - Bit 8: configures the MAC for calculating and appending the FCS. This relieves the host from calculating the FCS and the padding.
   - Bit 1: enable TX functionality, allowing the MAC to send Ethernet frames to the internal PHY
   - Bit0: enable RX functionality, allowing the MAC to receive Ethernet frames from the internal PHY.

   Please refer to the register description of the MAC CONFIG0 register for more options, as the above represent only the minimum required settings.
3. Enable the physical link by setting bit 12 of the “PHY Control Register” at MMS0, Address 0xFF00
4. Configure the SPI protocol engine, according to the application’s needs, by setting the appropriate bits in the SPI CONFIG0 Register at MMS0, address 0x0004.

   NOTE: A good starting point is writing 0x0000BC06, but that is dependent on the implementation and capabilities of the software running on the host.

   Note that as a last action, the SYNC bit needs to be set to one to allow data to flow between the host and the MACPHY.

The above four steps set the NCN26010 in CSMA/CD mode, accepting all valid Ethernet frames (“promiscuous” mode). This mode is useful when implementing traffic monitors, bridges or interface converters.

Basic Configuration for PLCA Operation

The NCN26010 offers the IEEE802.3cg specified feature of Physical Layer Collision Avoidance.

When PLCA is enabled, the coordinator node (PLCA ID = 0) starts a PLCA cycle by putting a BEACON on the line that is seen by all stations configured to operate in PLCA mode. PLCA only operates properly when all stations on the multi−drop segment have a valid PLCA configuration. Minimum requirements are:

- Every station needs to have a unique PLCA ID in the range of 0 to 254

- There shall be one and only one coordinator node.
- On the coordinator node, PLCA node count shall be configured to be greater or equal to the highest ID assigned to the stations in the mixing segment.
- It is recommended not to set the node count to values lower than 8.

In addition to the basic setup for CSMA/CD, users need to set for the coordinator node:

1. The local PLCA ID to 0 and the appropriate PLCA node count to allow all station to participate in the PLCA enabled segment.
   This is done by setting the correct numbers in the PLCACTRL1 register at MMS4, Address 0xCA02.
2. Enable PLCA by writing a one to PLCACTRL0 (MMS4, Address 0xCA01), bit 15.

For all other nodes in the PLCA enabled network, there is no need to specify the PLCA node count. This can be left at default or can be set to any other valid number.

Address Filtering

Running the NCN26010 in promiscuous mode will generate a lot of traffic on the SPI interface. This might not be desired in stations that are limited in performance (like low cost/low power MCUs) and could not cope with constant traffic of 10 Mb/s.

In a typical application, it is desired to have the MACPHY only forwarding Ethernet frames that match certain destination MAC addresses.

The NCN26010 offers a flexible scheme of up to four address match registers and filter masks allowing to forward frames that match dedicated destination address or groups of destination addresses.

These can be Broadcasts, Multicast and Unicast addresses.

For accepting broadcast frames, the MAC CONTROL0 register (MMS1, address 0x0000) needs to clear its BCSF.

To allow the MACPHY to forward multicast packets to the host, clear the MCSF bits in the MAC CONTROL0 register.

In the canonical case of a station being assigned a single dedicated MAC address to respond at, the ADDRFLTH, ADDRFLTL, ADDRMASKL and ADDRMASKH registers have to be set accordingly.

These filters can also be used to limit the multicast frames to dedicated multicast IDs or a larger group of IDs or unicast addresses. For example, when ADRF = 1, a frame is accepted if any of the ADDRFLT/MASK register pairs accept the frame. A pair accepts the frame if the logical bitwise AND between the frame's destination MAC address and the ADDMASK value matches exactly the ADDRFLT value.

Example A:

A NCN26010 device should be setup to forward all broadcast frames and frames with the destination address 60:C0:BF:01:01:01

Solution:

- Set ADDRFLT0L to 0xBF010101
- Set ADDRFLT0H to 0x800060C0
  note that bit 31 of ADDRFLTxH activates that filter
- Set ADDRMSK0L to 0xFFFFFFFF
- Set ADDRMSK0H to 0x0000FFFF
- Set bit ADRF and clear bit BCSF in the MAC CONTROLL0 register to one.

Example B:

In addition to Example A, the MACPHY should also accept all multicast frames of the group 31:6E:17:XX:XX:XX

Solution:

ADDRFLT1L = 0x17000000
ADDRFLT1H = 0x8000316E
ADDRMASK1L = 0xFF000000
ADDRMASK1H = 0x0000FFFF

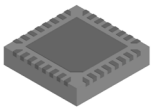
ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Shipping†
NCN26010XMNTXG	26010	QFN32 4x4, 0.4P (Pb−Free)	4000 / Tape & Reel
NCN26010XFBR2G	26010	TQFP 32, 5x5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



QFN32 4x4, 0.4P
CASE 485GH
ISSUE O

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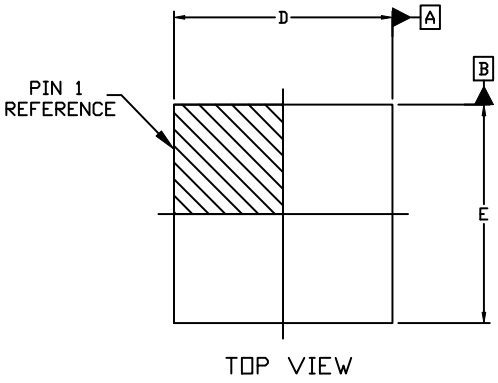
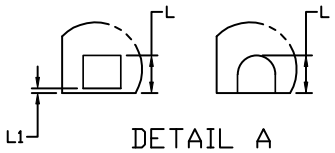
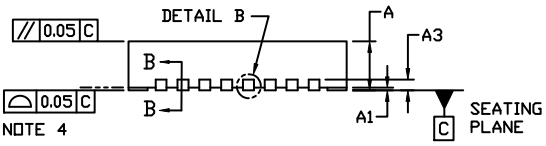
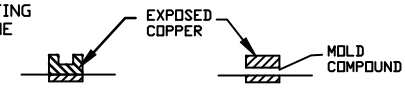


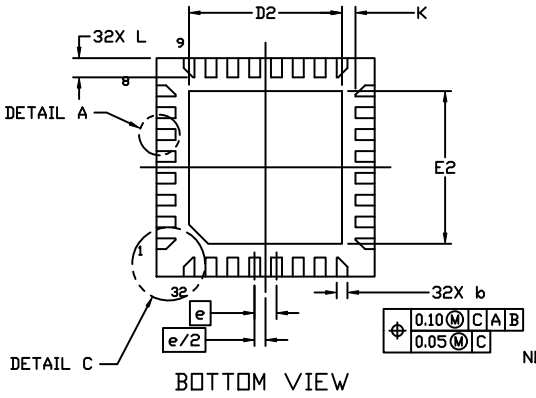
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



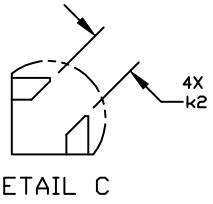
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.95	4.00	4.05
D2	2.70	2.80	2.90
E	3.95	4.00	4.05
E2	2.70	2.80	2.90
e		0.40 BSC	
K		0.25 REF	
k2		0.45 REF	
L	0.25	0.35	0.45
L1	---	---	0.15

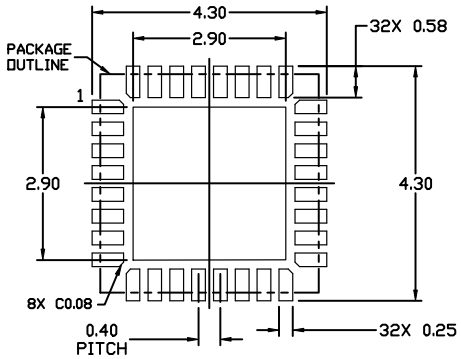






NOTE 3





RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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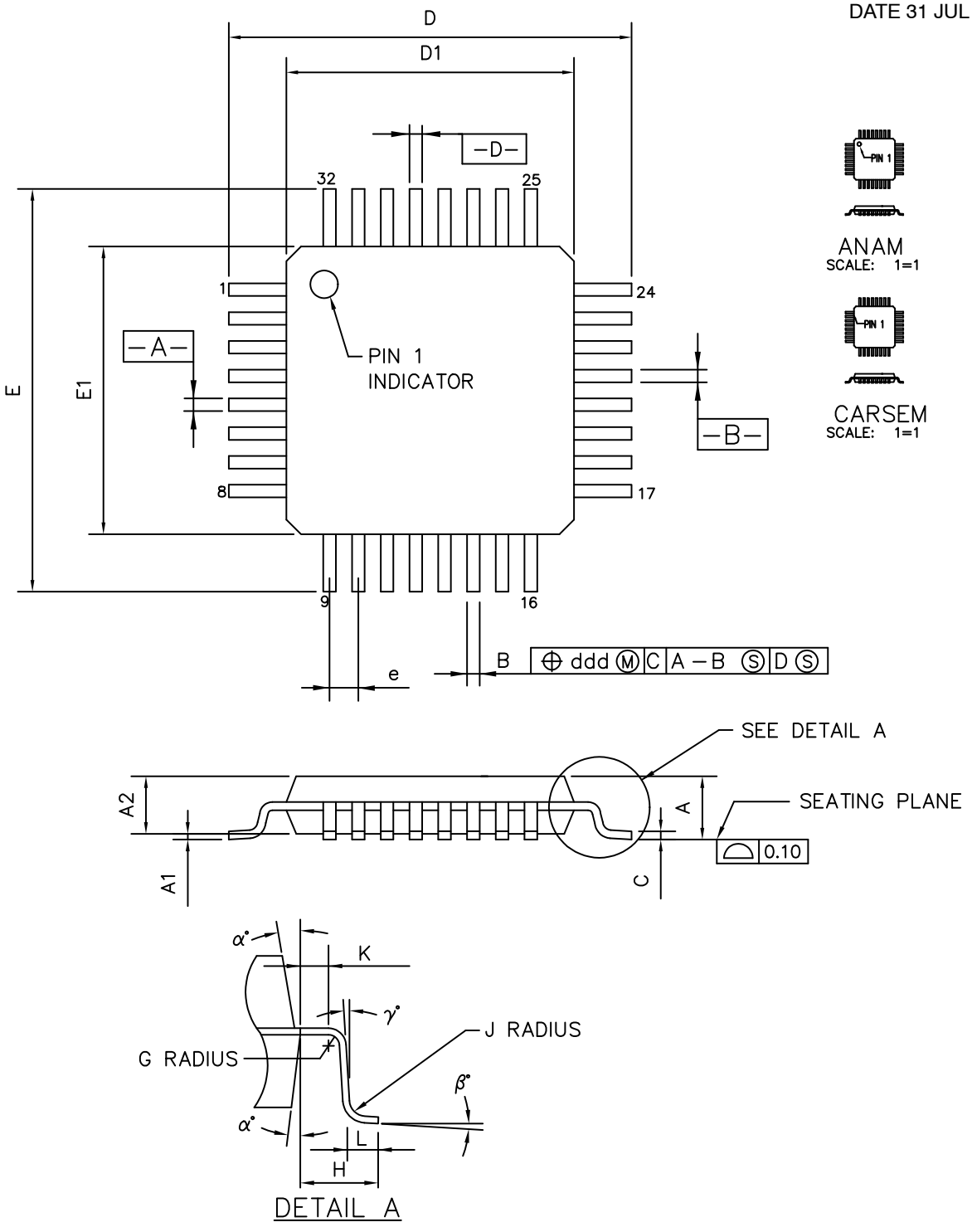

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TQFP 32, 5x5
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DATE 31 JUL 2008

1.0 mm
THICK

ANAM P/N 40579 ⚠12			
SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.95	1.00	1.05
D	7.00 BSC		
D1	5.00 BSC		
E	7.00 BSC		
E1	5.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
B	0.17	0.22	0.27
c	0.09	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–
G	0.08	–	–
H	1.00 REF.		
J	0.08	–	0.20
K	0.20	–	–
ccc	–	–	0.08
ddd	–	–	0.08

CARSEM PKGTQ0001 ⚠12			
SYMBOL	MIN	NOM	MAX
A	1.00	1.10	1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
D	7.00 BSC		
D1	5.00 BSC		
E	7.00 BSC		
E1	5.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
B	0.17	0.22	0.27
c	0.09	–	0.20
α°	11	12	13
β°	0	3.5	7
γ°	0	–	–
G	0.08	–	–
H	1.00 REF.		
J	0.08	–	0.20
K	0.20	–	–
ccc	–	–	0.08
ddd	–	–	0.08

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−1994.
2. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A−B AND D TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE H.
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.30 MILLIMETERS.
12. ⚠12 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS−026, VARIATION AAA AND AAB.
13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
14. DIMENSION D2 AND E2 REPRESENT THE SIZE OF THE EXPOSED PAD. THE ACTUAL DIMENSIONS ARE SPECIFIED ON THE BONDING DIAGRAM, AND IS DEPENDENT ON THE DIE SIZE.
15. EXPOSED PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05.
16. CORNER CHAMFER OF EXPOSED DIE PAD SHALL BE WITHIN 0.30 MM.

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