

## 3.3 V Automotive Grade M-LVDS Driver Receiver

### NBA3N201S

#### Description

The NBA3N201S is a 3.3 V supply differential Multipoint Low Voltage (M-LVDS) line Driver and Receiver for automotive applications. NBA3N201S offers the Type-1 receiver threshold at 0.0 V.

The NBA3N201S has Type-1 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of -1 V to 3.4 V. Type-1 receivers have near zero thresholds ( $\pm 50$  mV) and exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input.

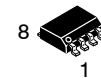
NBA3N201S supports Simplex or Half Duplex bus configurations.

#### Features

- Low-Voltage Differential 30  $\Omega$  to 55  $\Omega$  Line Drivers and Receivers for Signaling Rates Up to 200 Mbps
- Type-1 Receivers Incorporate 25 mV of Hysteresis
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- -1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With up to 2 V of Ground Noise
- Bus Pins High Impedance When Disabled or  $V_{CC} \leq 1.5$  V
- M-LVDS Bus Power Up/Down Glitch Free
- Operating range:  $V_{CC} = 3.3 \pm 10\%$  V (3.0 to 3.6 V)
- Operation from -40°C to 125°C.
- AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

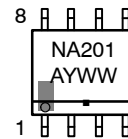
#### Applications

- Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Cellular Base Stations
- Central-Office Switches
- Network Switches and Routers
- Automotive



SOIC-8  
D SUFFIX  
CASE 751

#### MARKING DIAGRAM

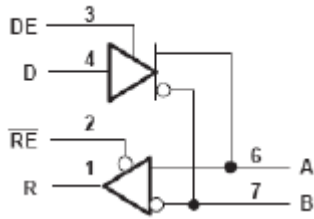


|       |                        |
|-------|------------------------|
| NA201 | = Specific Device Code |
| A     | = Assembly Location    |
| Y     | = Year                 |
| WW    | = Work Week            |
| ▪     | = Pb-Free Package      |

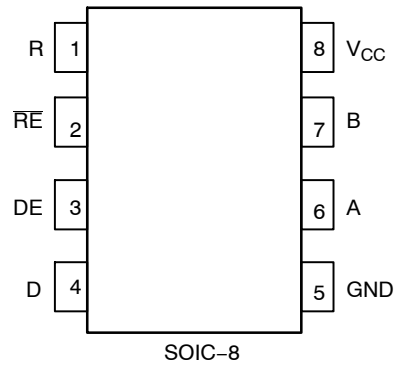
#### ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

# NBA3N201S



**Figure 1. Logic Diagram**



**Figure 2. Pinout Diagram**  
(Top View)

**Table 1. PIN DESCRIPTION**

| Number | Name | I/O Type             | Open Default | Description                                                                             |
|--------|------|----------------------|--------------|-----------------------------------------------------------------------------------------|
| 1      | R    | LVC MOS Output       |              | Receiver Output Pin                                                                     |
| 2      | RE   | LVC MOS Input        | High         | Receiver Enable Input Pin (LOW = Active, HIGH = High Z Output)                          |
| 3      | DE   | LVC MOS Input        | Low          | Driver Enable Input Pin (LOW = High Z Output, HIGH=Active)                              |
| 4      | D    | LVC MOS Input        |              | Driver Input Pin                                                                        |
| 5      | GND  |                      |              | Ground Supply pin. Pin must be connected to power supply to guarantee proper operation. |
| 6      | A    | M-LVDS Input /Output |              | Transceiver True Input/Output Pin                                                       |
| 7      | B    | M-LVDS Input /Output |              | Transceiver Invert Input/Output Pin                                                     |
| 8      | VCC  |                      |              | Power Supply pin. Pin must be connected to power supply to guarantee proper operation.  |

# NBA3N201S

Table 2. DEVICE FUNCTION TABLE

| TYPE 1 Receiver | Inputs                                    |                 | Output |       |
|-----------------|-------------------------------------------|-----------------|--------|-------|
|                 | $V_{ID} = V_A - V_B$                      | $\overline{RE}$ | R      |       |
|                 | $V_{ID} \geq 50 \text{ mV}$               | L               | H      |       |
|                 | $-50 \text{ mV} < V_{ID} < 50 \text{ mV}$ | L               | ?      |       |
|                 | $V_{ID} \leq -50 \text{ mV}$              | L               | L      |       |
|                 | X                                         | H               | Z      |       |
|                 | X                                         | Open            | Z      |       |
|                 | Open                                      | L               | ?      |       |
|                 | Input                                     |                 | Enable |       |
| DRIVER          | D                                         | DE              | A / Y  | B / Z |
|                 | L                                         | H               | L      | H     |
|                 | H                                         | H               | H      | L     |
|                 | Open                                      | H               | L      | H     |
|                 | X                                         | Open            | Z      | Z     |
|                 | X                                         | L               | Z      | Z     |
|                 | X                                         | L               | Z      | Z     |

H = High, L = Low, Z = High Impedance, X = Don't Care, ? = Indeterminate

# NBA3N201S

**Table 3. ATTRIBUTES** (Note 1)

| Characteristics                                               |                                                        |                  | Value                             |
|---------------------------------------------------------------|--------------------------------------------------------|------------------|-----------------------------------|
| ESD Protection                                                | Human Body Model (JEDEC Standard 22, Method A114-A)    | A, B<br>All Pins | ±6 kV<br>±2 kV                    |
|                                                               | Machine Model                                          | All Pins         | ±200 V                            |
|                                                               | Charged –Device Model (JEDEC Standard 22, Method C101) | All Pins         | ±1500 V                           |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) |                                                        |                  | Level 1                           |
| Flammability Rating<br>Oxygen Index                           |                                                        |                  | UL-94 code V-0 A 1/8"<br>28 to 34 |
| Transistor Count                                              |                                                        |                  | 917 Devices                       |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |                                                        |                  |                                   |

1. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS** (Note 2)

| Symbol           | Parameter                                | Condition 1        | Condition 2                                                                      | Rating                                                         | Unit              |
|------------------|------------------------------------------|--------------------|----------------------------------------------------------------------------------|----------------------------------------------------------------|-------------------|
| V <sub>CC</sub>  | Supply Voltage                           |                    |                                                                                  | -0.5 ≤ V <sub>CC</sub> ≤ 4.0                                   | V                 |
| V <sub>IN</sub>  | Input Voltage                            | D, DE, RE          |                                                                                  | -0.5 ≤ V <sub>IN</sub> ≤ 4.0                                   | V                 |
|                  |                                          | A, B               |                                                                                  | -1.8 ≤ V <sub>IN</sub> ≤ 4.0                                   |                   |
| I <sub>OUT</sub> | Output Voltage                           | R<br>A, B          |                                                                                  | -0.3 ≤ I <sub>OUT</sub> ≤ 4.0<br>-1.8 ≤ I <sub>OUT</sub> ≤ 4.0 | V                 |
| T <sub>A</sub>   | Operating Temperature Range, Industrial  |                    |                                                                                  | -40 to ≤ +125                                                  | °C                |
| T <sub>stg</sub> | Storage Temperature Range                |                    |                                                                                  | -65 to +150                                                    | °C                |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | SOIC-8                                                                           | 190<br>130                                                     | °C/W<br>°C/W      |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | (Note 3)           | SOIC-8                                                                           | 41 to 44                                                       | °C/W              |
| T <sub>sol</sub> | Wave Solder                              |                    |                                                                                  | 265                                                            | °C                |
| P <sub>D</sub>   | Power Dissipation (Continuous)           |                    | T <sub>A</sub> = 25°C<br>25°C < T <sub>A</sub> < 125°C<br>T <sub>A</sub> = 125°C | 725<br>5.8<br>377                                              | mW<br>mW/°C<br>mW |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously.

If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

# NBA3N201S

**Table 5. DC CHARACTERISTICS** VCC = 3.3 ±10% V( 3.0 to 3.6 V), GND = 0 V, TA = -40°C to +125°C (See Notes 4, 5)

| Symbol | Characteristic                                                                                                                                                                                                                                                                                                                                                 | Min  | Typ           | Max                 | Unit |
|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|---------------|---------------------|------|
| ICC    | Power Supply Current<br>Receiver Disabled Driver Enabled RE and DE at VCC, RL = 50 Ω, All others open<br>Driver and Receiver Disabled RE at VCC, DE at 0 V, RL = No Load, All others open<br>Driver and Receiver Enabled RE at 0 V, DE at VCC, RL = 50 Ω, All others open<br>Receiver Enabled Driver Disabled RE at 0 V, DE at 0 V, RL = 50 Ω, All others open |      | 13<br>1<br>16 | 22<br>4<br>24<br>13 | mA   |
| VIH    | Input HIGH Voltage                                                                                                                                                                                                                                                                                                                                             | 2    |               | VCC                 | V    |
| VIL    | Input LOW Voltage                                                                                                                                                                                                                                                                                                                                              | GND  |               | 0.8                 | V    |
| VBUS   | Voltage at any bus terminal VA, VB, VY or VZ                                                                                                                                                                                                                                                                                                                   | -1.4 |               | 3.8                 | V    |
| VID    | Magnitude of differential input voltage                                                                                                                                                                                                                                                                                                                        | 0.05 |               | VCC                 |      |

## DRIVER

|          |                                                                                                         |          |  |         |    |
|----------|---------------------------------------------------------------------------------------------------------|----------|--|---------|----|
| VAB      | Differential output voltage magnitude (see Figure 4)                                                    | 440      |  | 690     | mV |
| Δ VAB    | Change in Differential output voltage magnitude between logic states (see Figure 4)                     | -50      |  | 50      | mV |
| VOS(SS)  | Steady state common mode output voltage (see Figure 5)                                                  | 0.8      |  | 1.2     | V  |
| ΔVOS(SS) | Change in Steady state common mode output voltage between logic states (see Figure 5)                   | -50      |  | 50      | mV |
| VOS(PP)  | Peak-to-peak common-mode output voltage (see Figure 5)                                                  |          |  | 150     | mV |
| VAOC     | Maximum steady-state open-circuit output voltage (see Figure 9)                                         | 0        |  | 2.4     | V  |
| VBOC     | Maximum steady-state open-circuit output voltage (see Figure 9)                                         | 0        |  | 2.4     | V  |
| VP(H)    | Voltage overshoot, low-to-high level output (see Figure 7)                                              |          |  | 1.2 VSS | V  |
| VP(L)    | Voltage overshoot, high-to-low level output (see Figure 7)                                              | -0.2 VSS |  |         | V  |
| IIH      | High-level input current (D, DE) VIH = 2 V                                                              | 0        |  | 10      | uA |
| IIL      | Low-level input current (D, DE) VIL = 0.8 V                                                             | 0        |  | 10      | uA |
| JIOSJ    | Differential short-circuit output current magnitude (see Figure 6)                                      |          |  | 24      | mA |
| IOZ      | High-impedance state output current (driver only)<br>-1.4 V ≤ (VA or VB) ≤ 3.8 V, other output at 1.2 V | -15      |  | 10      | uA |
| IO(OFF)  | Power-off output current (0 V ≤ VCC ≤ 1.5 V)<br>-1.4 V ≤ (VA or VB) ≤ 3.8 V, other output at 1.2 V      | -10      |  | 10      | uA |

## RECEIVER

|         |                                                                                                                                 |     |    |     |    |
|---------|---------------------------------------------------------------------------------------------------------------------------------|-----|----|-----|----|
| VIT+    | Positive-going Differential Input voltage Threshold (See Figure 11 & Table 8)<br>Type 1                                         |     |    | 50  | mV |
| VIT-    | Negative-going Differential Input voltage Threshold (See Figure 11 & Table 8)<br>Type 1                                         | -50 |    |     | mV |
| VHYS    | Differential Input Voltage Hysteresis (See Figure 11 and Table 2)<br>Type 1                                                     |     | 25 |     | mV |
| VOH     | High-level output voltage (IOH = -8 mA)                                                                                         | 2.4 |    |     | V  |
| VOL     | Low-level output voltage (IOL = 8 mA)                                                                                           |     |    | 0.4 | V  |
| IIH     | RE High-level input current (VIH = 2 V)                                                                                         | -10 |    | 0   | uA |
| IIL     | RE Low-level input current (VIL = 0.8 V)                                                                                        | -10 |    | 0   | uA |
| IOZ     | High-impedance state output current (VO = 0 V of 3.6 V)                                                                         | -10 |    | 15  | uA |
| CA / CB | Input Capacitance VI = 0.4 sin(30E6πt) + 0.5 V, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent)         |     | 3  |     | pF |
| CAB     | Differential Input Capacitance VAB = 0.4 sin(30E6πt) V, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent) |     |    | 2.5 | pF |
| CA/B    | Input Capacitance Balance, (CA/CB)                                                                                              | 99  |    | 101 | %  |

# NBA3N201S

**Table 5. DC CHARACTERISTICS** VCC = 3.3 ±10% V( 3.0 to 3.6 V), GND = 0 V, TA = -40°C to +125°C (See Notes 4, 5)

| Symbol                      | Characteristic                                                                                                                                              | Min             | Typ<br>(Note<br>5) | Max           | Unit |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--------------------|---------------|------|
| <b>BUS INPUT AND OUTPUT</b> |                                                                                                                                                             |                 |                    |               |      |
| IA                          | Input Current Receiver or Transceiver with Driver Disabled<br>VA = 3.8 V, VB = 1.2 V<br>VA = 0.0 V or 2.4 V, VB = 1.2 V<br>VA = -1.4 V, VB = 1.2 V          | 0<br>-20<br>-32 |                    | 32<br>20<br>0 | uA   |
| IB                          | Input Current Receiver or Transceiver with Driver Disabled<br>VB = 3.8 V, VA = 1.2 V<br>VB = 0.0 V or 2.4 V, VA = 1.2 V<br>VB = -1.4 V, VA = 1.2 V          | 0<br>-20<br>-32 |                    | 32<br>20<br>0 | uA   |
| IAB                         | Differential Input Current Receiver or Transceiver with driver disabled (IA-IB)<br>VA = VB, -1.4 ≤ VA ≤ 3.8 V                                               | -4              |                    | 4             | uA   |
| IA(OFF)                     | Input Current Receiver or Transceiver Power Off 0V ≤ VCC ≤ 1.5 and:<br>VA = 3.8 V, VB = 1.2 V<br>VA = 0.0 V or 2.4 V, VB = 1.2 V<br>VA = -1.4 V, VB = 1.2 V | 0<br>-20<br>-32 |                    | 32<br>20<br>0 | uA   |
| IB(OFF)                     | Input Current Receiver or Transceiver Power Off 0V ≤ VCC ≤ 1.5 and:<br>VB = 3.8 V, VA = 1.2 V<br>VB = 0.0 V or 2.4 V, VA = 1.2 V<br>VB = -1.4 V, VA = 1.2 V | 0<br>-20<br>-32 |                    | 32<br>20<br>0 | uA   |
| IAB(OFF)                    | Receiver Input or Transceiver Input/Output Power Off Differential Input Current; (IA-IB)<br>VA = VB, 0 ≤ VCC ≤ 1.5 V, -1.4 ≤ VA ≤ 3.8 V                     | -4              |                    | 4             | uA   |
| CA                          | Transceiver Input Capacitance with Driver Disabled VA = 0.4 sin(30E6πt) + 0.5 V using HP4194A impedance analyzer (or equivalent); VB = 1.2 V                |                 | 5                  |               | pF   |
| CB                          | Transceiver Input Capacitance with Driver Disabled VB = 0.4 sin(30E6πt) + 0.5 V using HP4194A impedance analyzer (or equivalent); VA = 1.2 V                |                 | 5                  |               | pF   |
| CAB                         | Transceiver Differential Input Capacitance with Driver Disabled VA = 0.4 sin(30E6πt) + 0.5 V using HP4194A impedance analyzer (or equivalent); VB = 1.2 V   |                 |                    | 3.0           | pF   |
| CA/B                        | Transceiver Input Capacitance Balance with Driver Disabled, (CA/CB)                                                                                         | 99              |                    | 101           | %    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. See Figure 3. DC Measurements reference.

5. Typ value at 25°C and 3.3 VCC supply voltage.

**Table 6. DRIVER AC CHARACTERISTICS** VCC = 3.3 ±10% V( 3.0 to 3.6 V), GND = 0 V, TA = -40°C to +125°C (Note 6)

| Symbol      | Characteristic                                                                                                                                                             | Min | Typ | Max | Unit |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| tPLH / tPHL | Propagation Delay (See Figure 7)                                                                                                                                           | 1.0 | 1.5 | 2.4 | ns   |
| tPHZ / tPLZ | Disable Time HIGH or LOW state to High Impedance (See Figure 8)                                                                                                            |     |     | 7   | ns   |
| tPZH / tPZL | Enable Time High Impedance to HIGH or LOW state (See Figure 8)                                                                                                             |     |     | 7   | ns   |
| tSK(P)      | Pulse Skew ( tPLH - tPHL ) (See Figure 7)                                                                                                                                  |     | 0   | 150 | ps   |
| tSK(PP)     | Device to Device Skew similar path and conditions (See Figure 7)                                                                                                           |     |     | 1   | ns   |
| tJIT(PER)   | Period Jitter RMS, 100 MHz (Source tr/tf 0.5 ns, 10 and 90 % points, 30k samples. Source jitter de-embedded from Output values ) (See Figure 10)                           |     | 2   | 3.5 | ps   |
| tJIT(PP)    | Peak-to-peak Jitter, 200 Mbps 2 <sup>15</sup> -1 PRBS (Source tr/tf 0.5 ns, 10 and 90% points, 100k samples. Source jitter de-embedded from Output values) (See Figure 10) |     | 30  | 160 | ps   |
| tr / tf     | Differential Output rise and fall times (See Figure 7)                                                                                                                     | 0.9 |     | 1.6 | ns   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

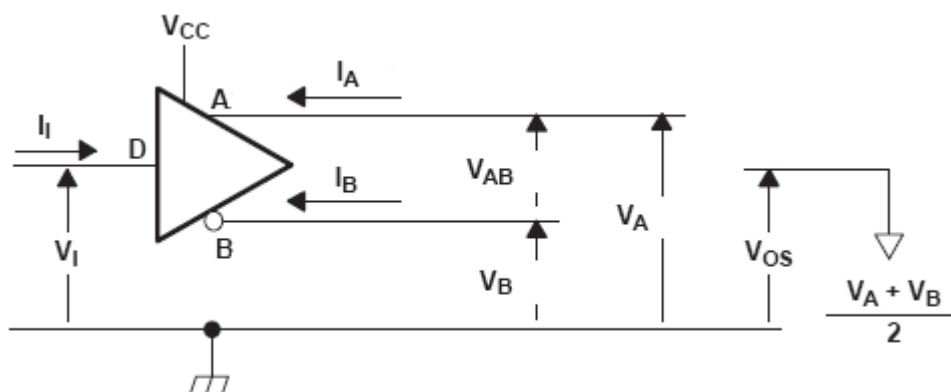
6. Typ value at 25°C and 3.3 VCC supply voltage.

**Table 7. RECEIVER AC CHARACTERISTICS** VCC = 3.3 ±10% V( 3.0 to 3.6 V), GND = 0 V, TA = -40°C to +125°C (Note 7)

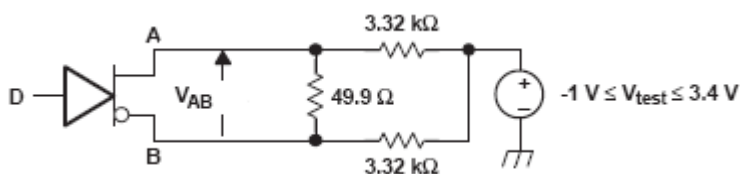
| Symbol                              | Characteristic                                                                                                                                                                                      | Min | Typ | Max | Unit |
|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| t <sub>PLH</sub> / t <sub>PHL</sub> | Propagation Delay (See Figure 12)                                                                                                                                                                   | 2   | 4   | 6   | ns   |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | Disable Time HIGH or LOW state to High Impedance (See Figure 13)                                                                                                                                    |     |     | 10  | ns   |
| t <sub>PZH</sub> / t <sub>PZL</sub> | Enable Time High Impedance to HIGH or LOW state (See Figure 13)                                                                                                                                     |     |     | 18  | ns   |
| t <sub>SK(P)</sub>                  | Pulse Skew ( t <sub>PLH</sub> - t <sub>PHL</sub>  ) (See Figure 14) C <sub>L</sub> = 5 pF<br>Type 1                                                                                                 |     | 100 | 400 | ps   |
| t <sub>SK(PP)</sub>                 | Device to Device Skew similar path and conditions (See Figure 12) C <sub>L</sub> = 5 pF                                                                                                             |     |     | 1   | ns   |
| t <sub>JIT(PER)</sub>               | Period Jitter RMS, 100 MHz (Source: VID = 200 mV <sub>pp</sub> V <sub>CM</sub> = 1 V, tr/tf 0.5 ns, 10 and 90 % points, 30k samples. Source jitter de-embedded from Output values ) (See Figure 14) |     | 4   | 8   | ps   |
| t <sub>JIT(PP)</sub>                | Peak-to-peak Jitter, 200 Mbps 2 <sup>15</sup> -1 PRBS (Source tr/tf 0.5 ns, 10% and 90% points, 100k samples. Source jitter de-embedded from Output values) (See Figure 14)<br>Type 1               |     | 300 | 800 | ps   |
| tr / tf                             | Differential Output rise and fall times (See Figure 14) C <sub>L</sub> = 15 pF                                                                                                                      | 1   |     | 2.3 | ns   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Typ value at 25°C and 3.3 VCC supply voltage. .

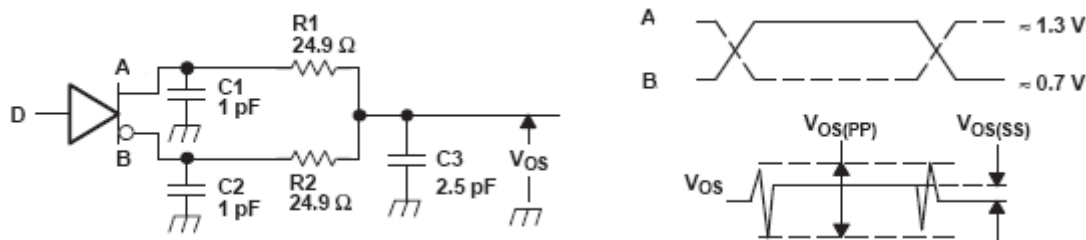


**Figure 3. Driver Voltage and Current Definitions**



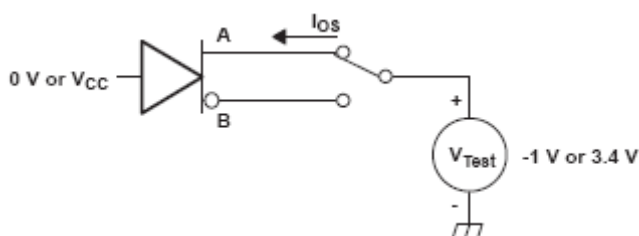
A. All resistors are 1% tolerance.

**Figure 4. Differential Output Voltage Test Circuit**

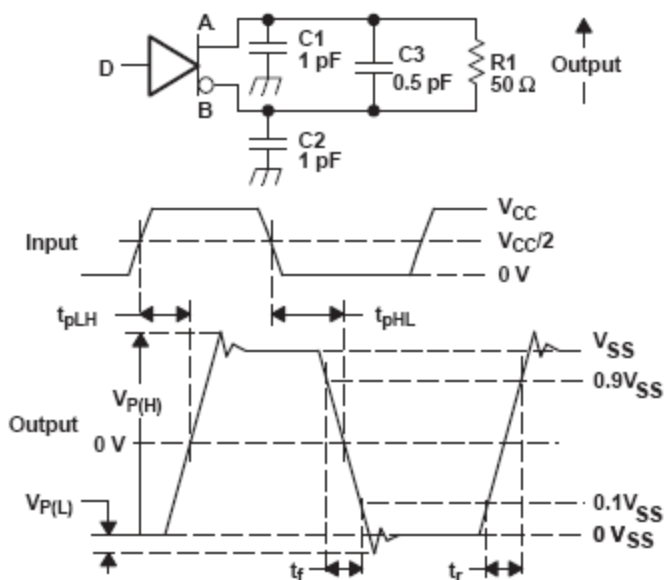


- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse frequency = 500 kHz, duty cycle =  $50 \pm 5\%$ .  
 B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20% tolerance.  
 C. R1 and R2 are metal film, surface mount, 1% tolerance, and located within 2 cm of the D.U.T.  
 D. The measurement of  $V_{OS(PP)}$  is made on test equipment with a  $-3$  dB bandwidth of at least 1 GHz.

**Figure 5. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**

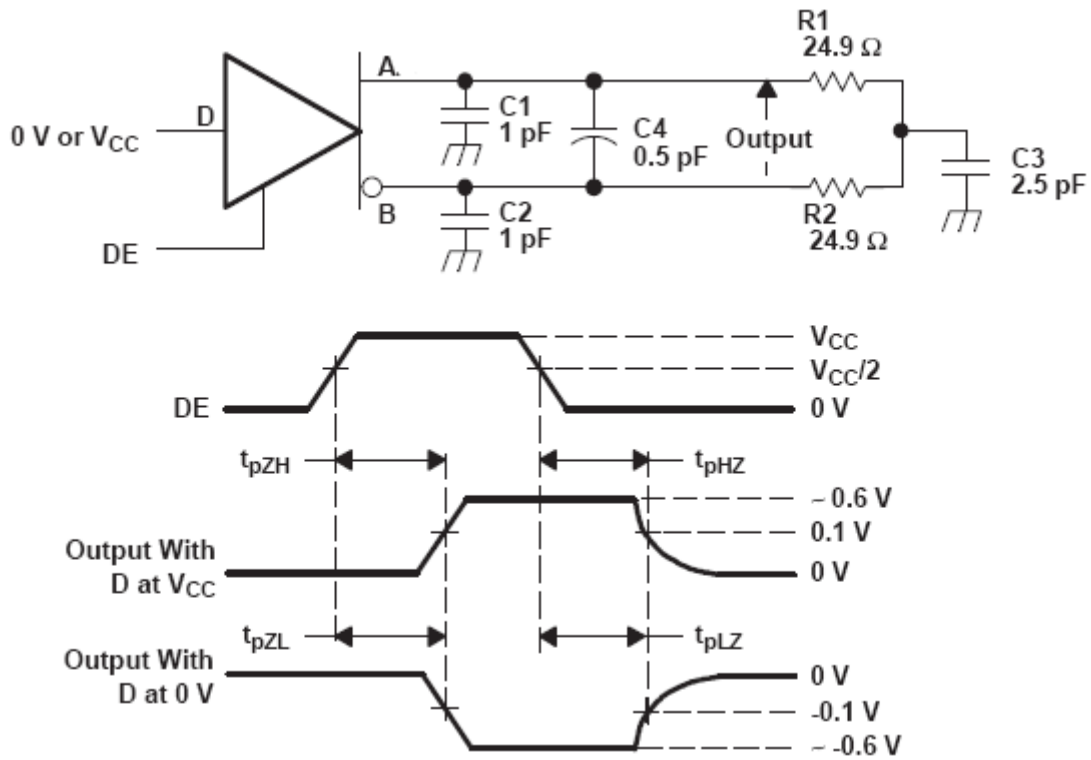


**Figure 6. Driver Short-Circuit Test Circuit**



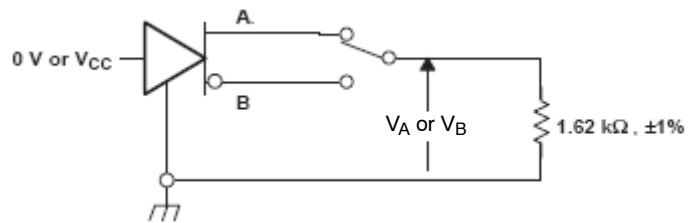
- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 500 kHz, duty cycle =  $50 \pm 5\%$ .  
 B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.  
 C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.  
 D. The measurement is made on test equipment with a  $-3$  dB bandwidth of at least 1 GHz.

**Figure 7. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**

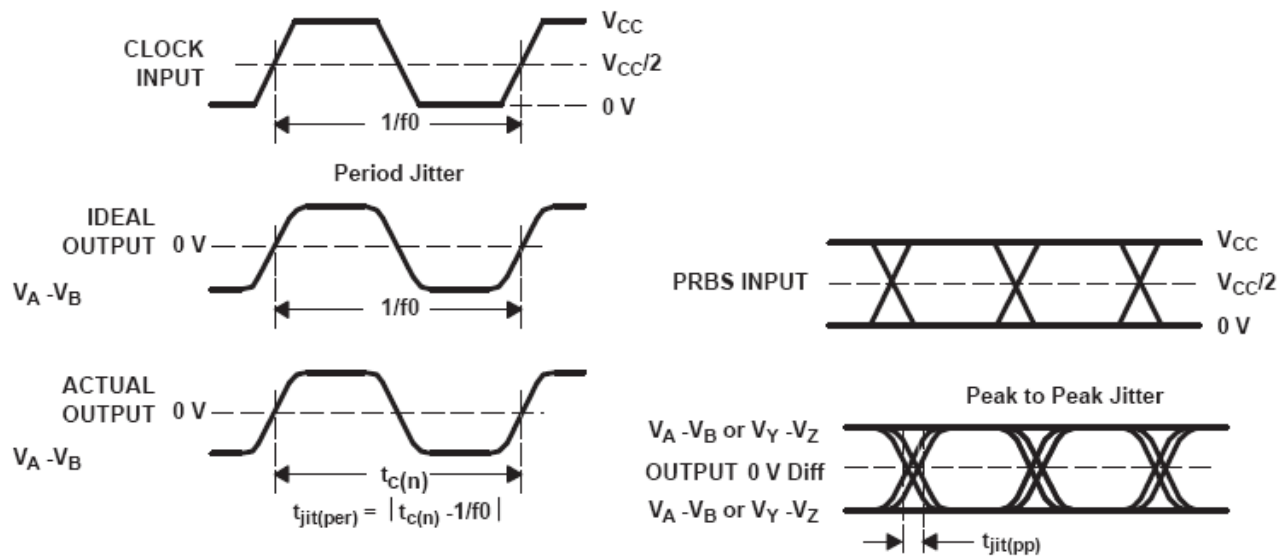


- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 500 kHz, duty cycle =  $50 \pm 5\%$ .
- B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
- C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

**Figure 8. Driver Enable and Disable Time Circuit and Definitions**



**Figure 9. Maximum Steady State Output Voltage**



- A. All input pulses are supplied by an Agilent 8304A Stimulus System.  
 B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software  
 C. Period jitter is measured using a 100 MHz 50  $\pm$ 1% duty cycle clock input.  
 D. Peak-to-peak jitter is measured using a 200 Mbps 2<sub>15</sub>-1 PRBS input.

Figure 10. Driver Jitter Measurement Waveforms

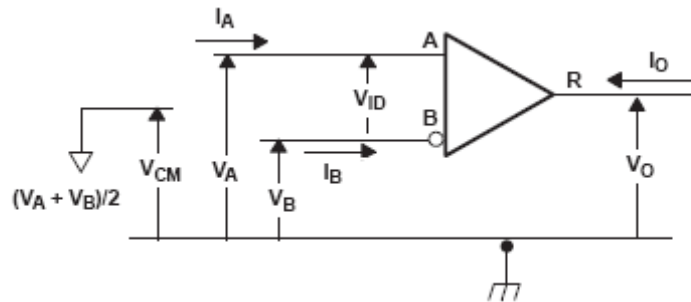
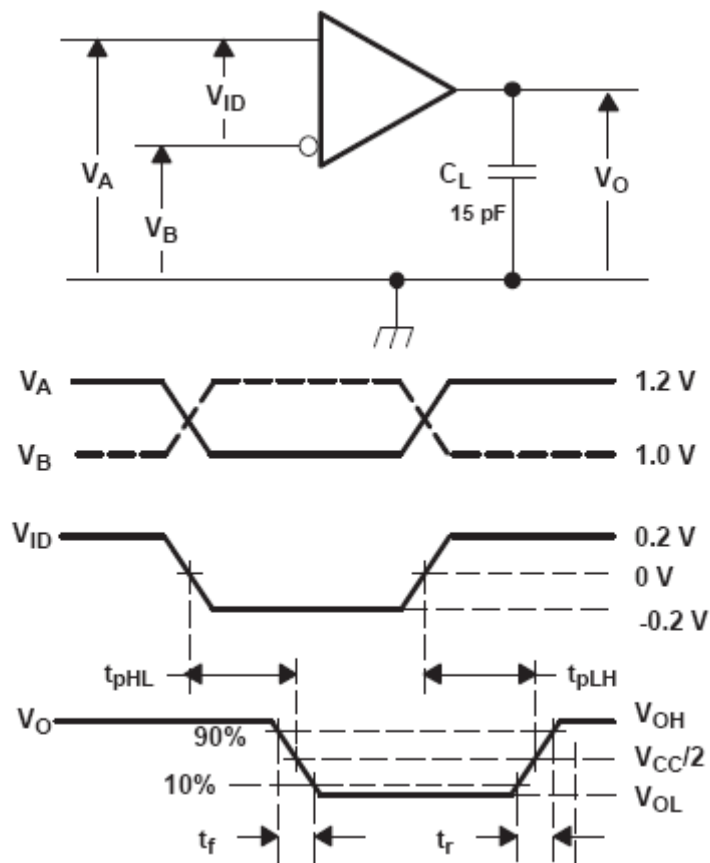
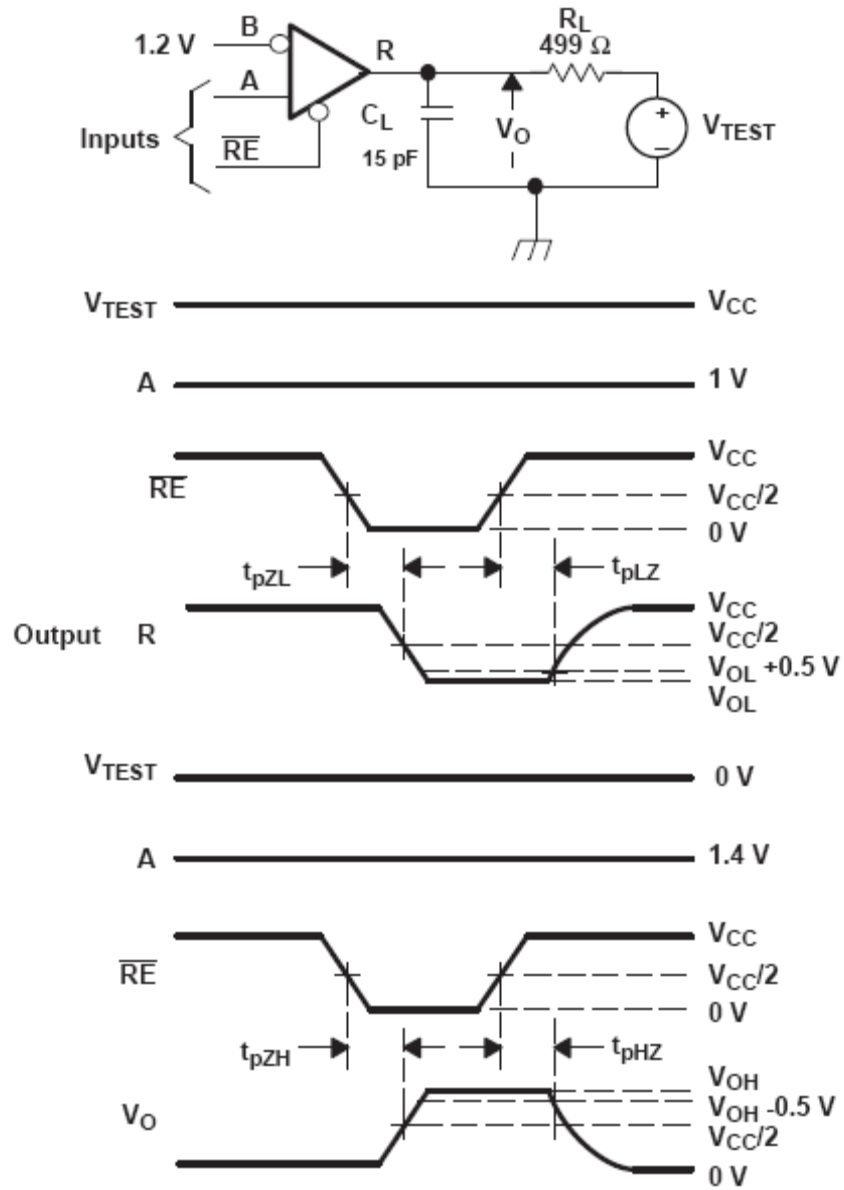


Figure 11. Receiver Voltage and Current Definitions



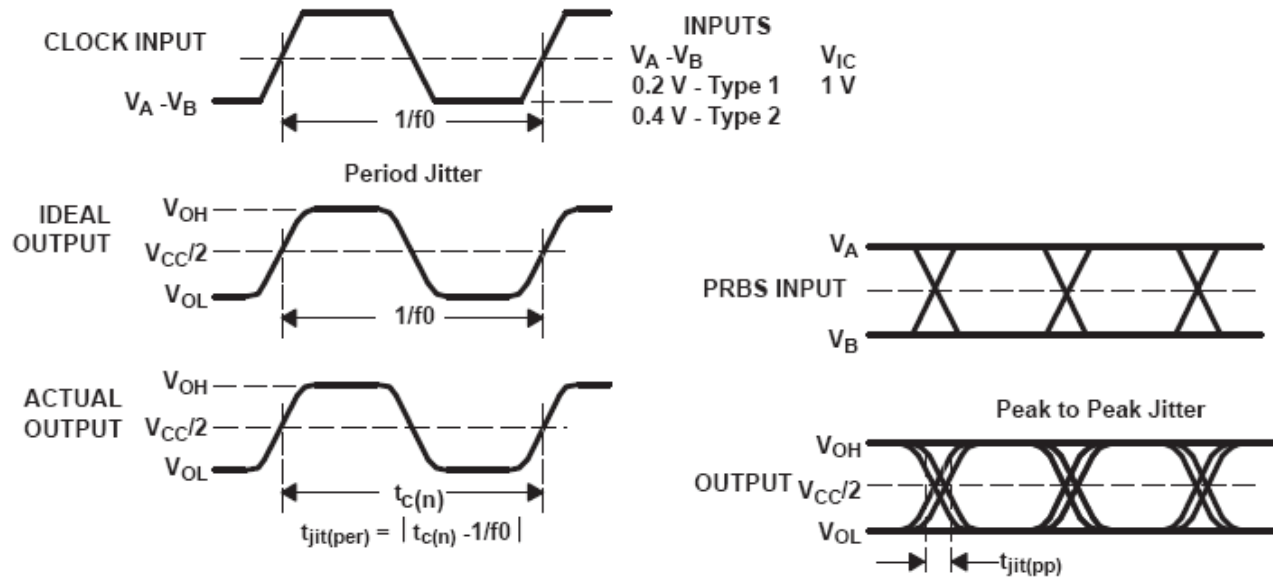
- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 50 MHz, duty cycle = 50  $\pm$  5%.  $C_L$  is a combination of a 20%–tolerance, low–loss ceramic, surface–mount capacitor and fixture capacitance within 2 cm of the D.U.T.
- B. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

**Figure 12. Receiver Timing Test Circuit and Waveforms**



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 500 kHz, duty cycle = 50  $\pm 5\%$ .
- B.  $R_L$  is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- C.  $C_L$  is the instrumentation and fixture capacitance within 2 cm of the DUT and 20%.

Figure 13. Receiver Enable/Disable Time Test Circuit and Waveforms



- A. All input pulses are supplied by an Agilent 8304A Stimulus System.  
 B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software  
 C. Period jitter is measured using a 100 MHz 50  $\pm$ 1% duty cycle clock input.  
 D. Peak-to-peak jitter is measured using a 200 Mbps 2<sup>15</sup>-1 PRBS input.

**Figure 14. Receiver Jitter Measurement Waveforms**

**Table 8. TYPE-1 RECEIVER INPUT THRESHOLD TEST VOLTAGES**

| Applied Voltages |        | Resulting Differential Input Voltage | Resulting Common-Mode Input Voltage | Receiver Output |
|------------------|--------|--------------------------------------|-------------------------------------|-----------------|
| VIA              | VIB    | VID                                  | VIC                                 |                 |
| 2.400            | 0.000  | 2.400                                | 1.200                               | H               |
| 0.000            | 2.400  | -2.400                               | 1.200                               | L               |
| 3.800            | 3.750  | 0.050                                | 3.775                               | H               |
| 3.750            | 3.800  | -0.050                               | 3.775                               | L               |
| -1.350           | -1.400 | 0.050                                | -1.375                              | H               |
| -1.400           | -1.350 | -0.050                               | -1.375                              | L               |

H = high level, L = low level, output state assumes receiver is enabled (RE = L)

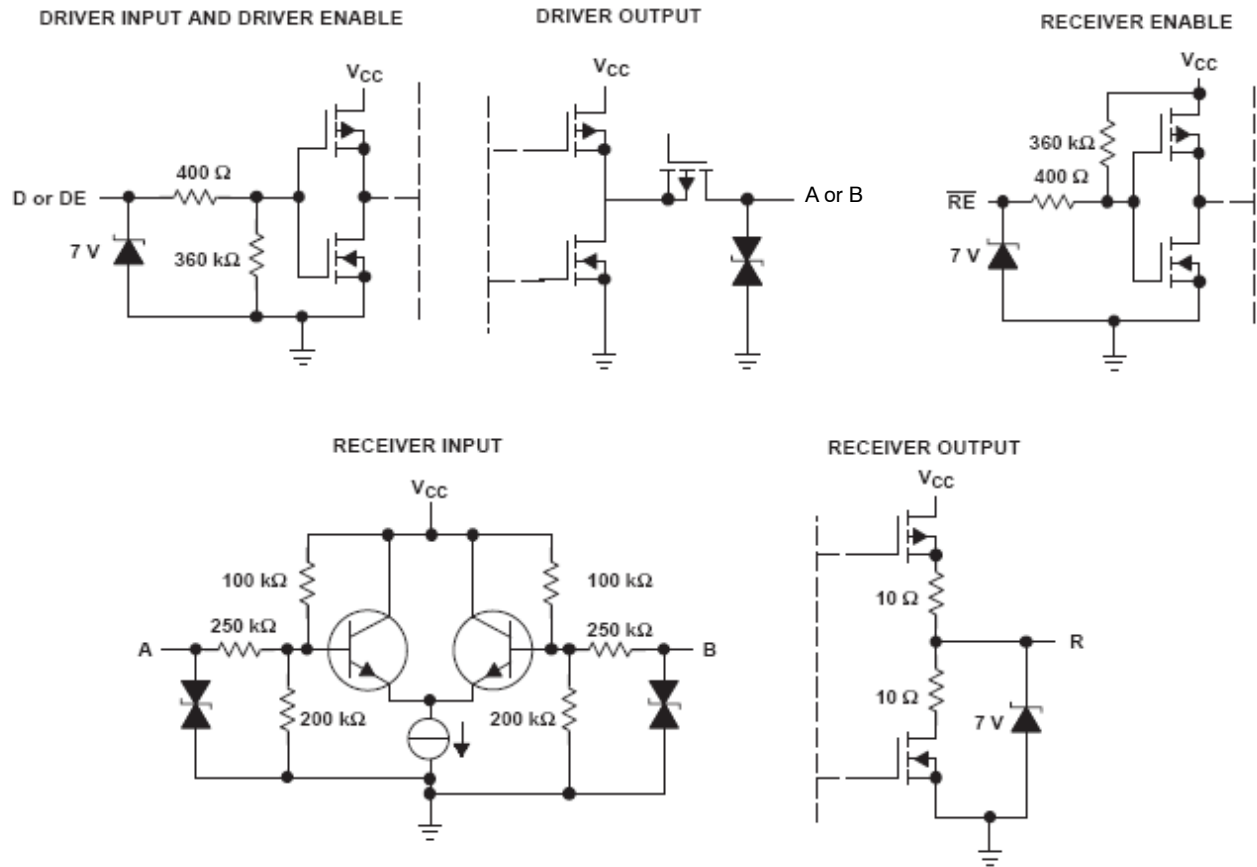


Figure 15. Equivalent Input and Output Schematic Diagrams

## APPLICATION INFORMATION

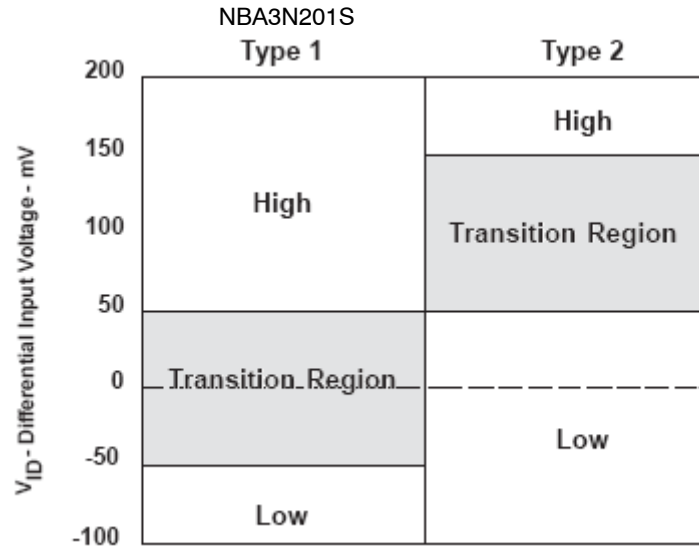
### Receiver Input Threshold (Failsafe)

The MLVDS standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts.

Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in Table 9 and Figure 16.

**Table 9. RECEIVER INPUT VOLTAGE THRESHOLD REQUIREMENTS**

| Receiver Type | Output Low                                          | Output High                                       |
|---------------|-----------------------------------------------------|---------------------------------------------------|
| Type 1        | $-2.4\text{ V} \leq \text{VID} \leq -0.05\text{ V}$ | $0.05\text{ V} \leq \text{VID} \leq 2.4\text{ V}$ |
| Type 2        | $-2.4\text{ V} \leq \text{VID} \leq 0.05\text{ V}$  | $0.15\text{ V} \leq \text{VID} \leq 2.4\text{ V}$ |



**Figure 16. Receiver Differential Input Voltage Showing Transition Regions by Type**

### LIVE INSERTION/GLITCH-FREE POWER UP/DOWN

The NBA3N201S provides a glitch-free power up/down feature that prevents the M-LVDS outputs of the device from turning on during a power up or power down event. This is especially important in live insertion applications, when a device is physically connected to an M-LVDS multipoint bus and  $V_{CC}$  is ramping.

While the M-LVDS interface for these devices is glitch free on power up/down, the receiver output structure is not.

Figure 17 shows the performance of the receiver output pin, R (CHANNEL 2), as  $V_{CC}$  (CHANNEL 1) is ramped. The glitch on the R pin is independent of the RE voltage. Any complications or issues from this glitch are easily resolved in power sequencing or system requirements that suspend operation until  $V_{CC}$  has reached a steady state value.

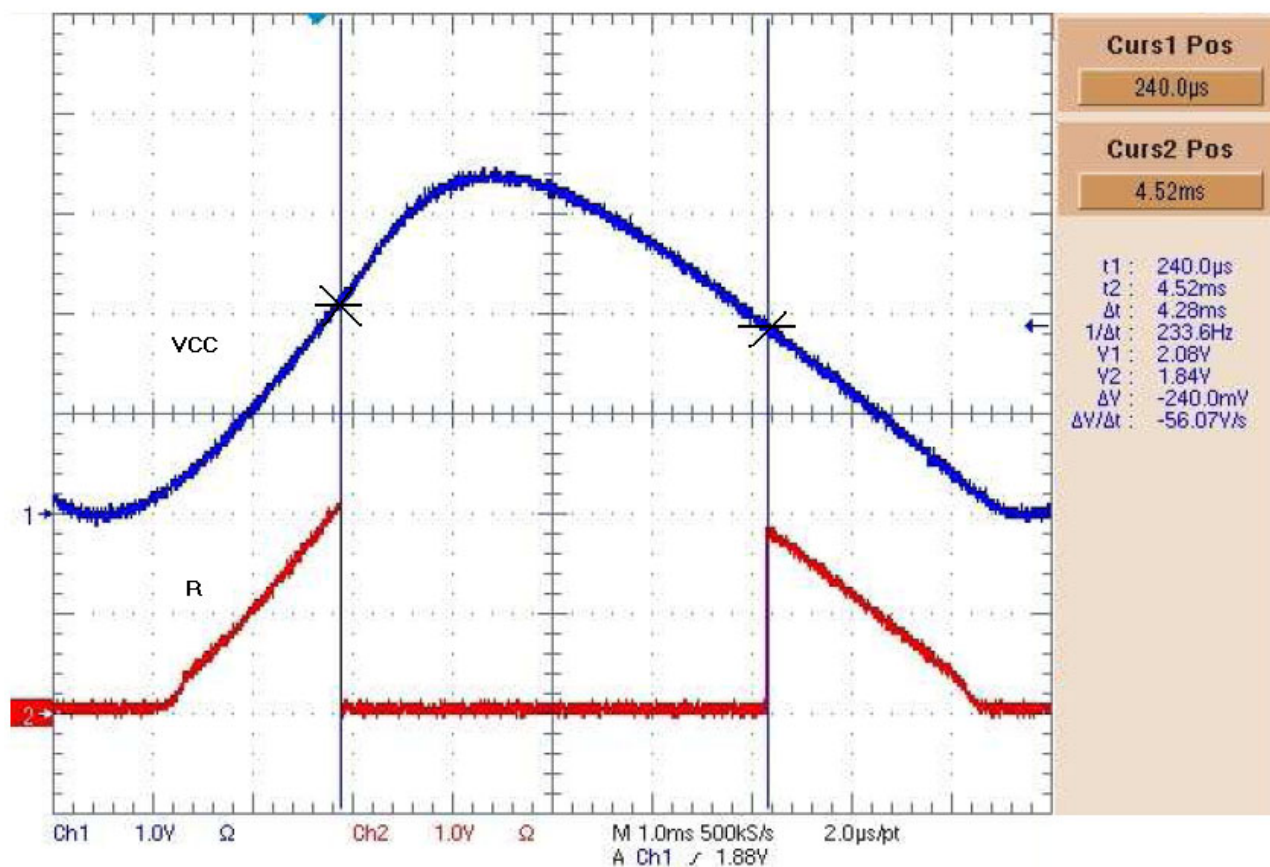


Figure 17. M-LVDS Receiver Output: VCC (CHANNEL 1), R Pin (CHANNEL 2)

**Simplex Theory Configurations:** Data flow is unidirectional and Point-to-Point from one Driver to one Receiver. NBA3N201S devices provide a high signal current allowing long drive runs and high noise immunity. Single terminated interconnects yield high amplitude levels.

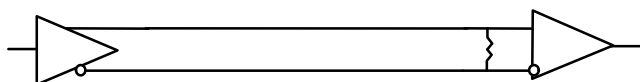


Figure 18. Point-to-Point Simplex Single Termination

**Simplex Multidrop Theory Configurations:** Data flow is unidirectional from one Driver with one or more Receivers. Multiple boards required. Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and

Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. See Figures 18 and 19. A NBA3N201S can be used as the driver or as a receiver.

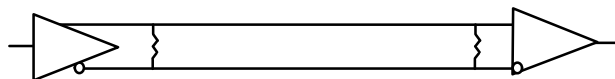


Figure 19. Parallel-Terminated Simplex

minimizes reflections. On the Evaluation Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to a each other or a bus. See Figures 20 and 21. A NBA3N201S can be used as the driver or as a receiver.

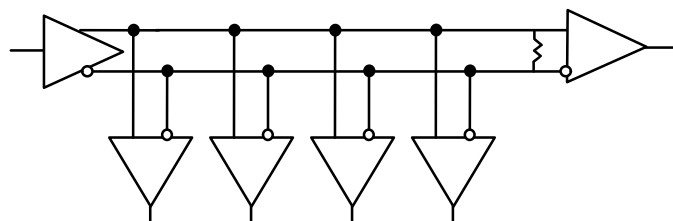


Figure 20. Multidrop or Distributed Simplex with Single Termination

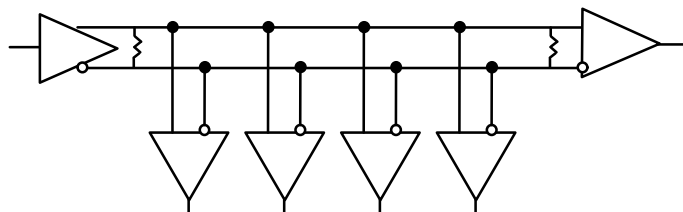


Figure 21. Multidrop or Distributed Simplex with Double Termination

**Half Duplex Multinode Multipoint Theory Configurations:** Data flow is unidirectional and selected from one of multiple possible Drivers to multiple Receivers. One “Two Node” multipoint connection can be accomplished with a single evaluation test board. More than Two Nodes requires multiple evaluation test boards. Parallel terminated interconnects yield typical MLVDS amplitude

levels and minimizes reflections. Parallel terminated interconnects yield typical LMVDS amplitude levels and minimizes reflections. On the Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to each other or a bus. See Figure 22. A NBA3N201S can be used as the driver or as a receiver.

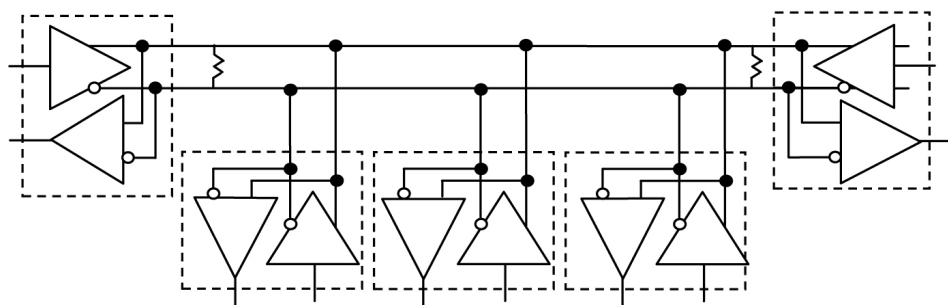


Figure 22. Multinode Multipoint Half Duplex (requires Double Termination)

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

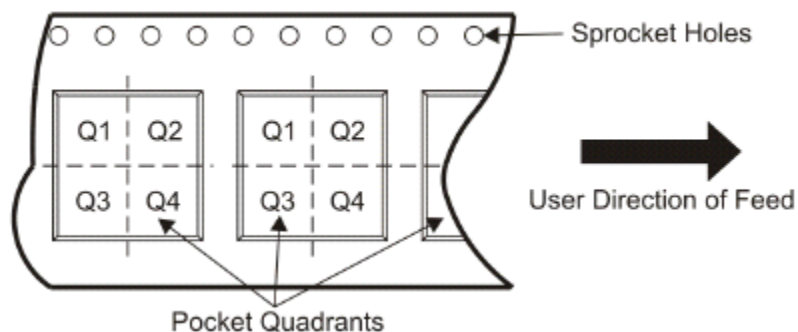


Figure 23.

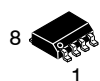
## NBA3N201S

### ORDERING INFORMATION

| Device        | Receiver | Pin 1 Quadrant | Package               | Shipping <sup>†</sup> |
|---------------|----------|----------------|-----------------------|-----------------------|
| NBA3N201SDR2G | Type 1   | Q1             | SOIC – 8<br>(Pb-Free) | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

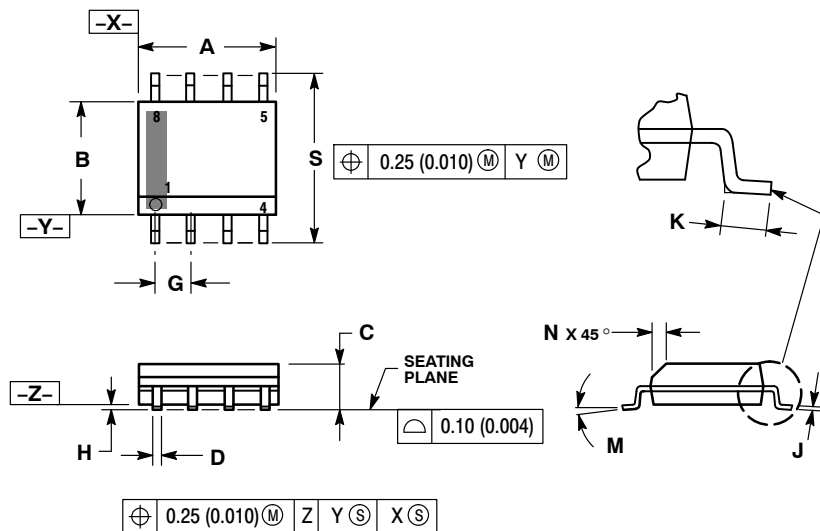
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011

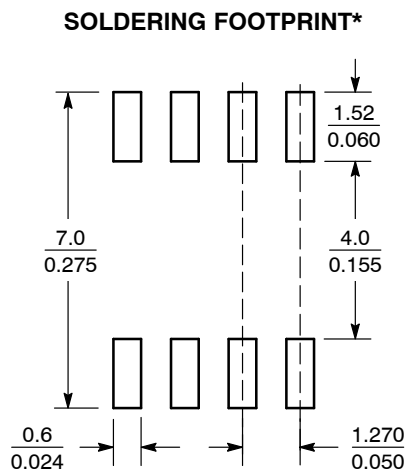


## NOTES:

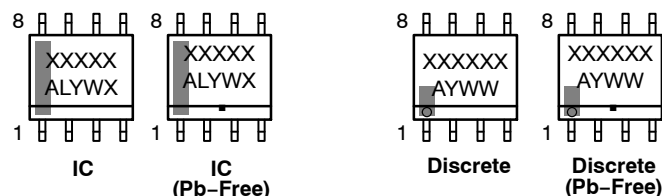
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

## GENERIC MARKING DIAGRAM\*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                  |
|------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2                                                                                                                                                                      |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
|-------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42564B</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-8 NB</b>   | <b>PAGE 2 OF 2</b>                                                                                                                                                                  |

**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)