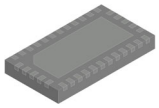
3.3 V USB 3.2 10 Gbps Quad Channel / Dual Port Linear Redriver

NB7NPQ1404E2M



UQFN34
CASE 523BR

MARKING DIAGRAM



NB7N404E = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NB7NPQ1404E2MMUTWG	UQFN34 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Description

The NB7NPQ1404E2M is a high performance 2−Port linear redriver designed for USB 3.2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter−symbol interference (ISI). The NB7NPQ1404E2M compensates for these losses by engaging varying levels of equalization at the input receiver, and flat gain amplification on the output transmitter.

The NB7NPQ1404E2M offers programmable equalization and flat gain for each independent channel to optimize performance over various physical mediums.

The NB7NPQ1404E2M contains an automatic receiver detect function which will determine whether the output is active. The receiver detection loop will be active if the corresponding channel's signal detector is idle for a period of time. The channel will then move to Unplug Mode if a load is not detected, or it will return to Low Power Mode (Slumber mode) due to inactivity.

The NB7NPQ1404E2M comes in a 2.5 x 4.5 x 0.55 mm UQFN34 package and is specified to operate across the entire industrial temperature range, –40°C to 85°C.

Features

- 3.3 V ± 0.3 V Power Supply
- 5 Gbps & 10 Gbps Serial Link with Linear Amplifier
- Device Supports USB 3.2 Gen2 and Gen1
- Automatic Receiver Detection
- Supports USB−IF VCM Requirement
- Integrated Input and Output Termination
- Pin Adjustable Receiver Equalization and Flat Gain
- 100 Ω Differential CML I/O's
- Auto Slumber Mode for Adaptive Power Management
- Hot−Plug Capable
- ESD Protection ±4 kV HBM
- Operating Temperature Range Industrial: −40°C to +85°C
- Package: UQFN34, 2.5 x 4.5 x 0.55 mm
- This is a Pb−Free Device

Typical Applications

- USB3.2 Type−A and Type−C Signal Routing
- Mobile Phone and Tablet
- Computer, Laptop and Notebook
- External Storage Device
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V.

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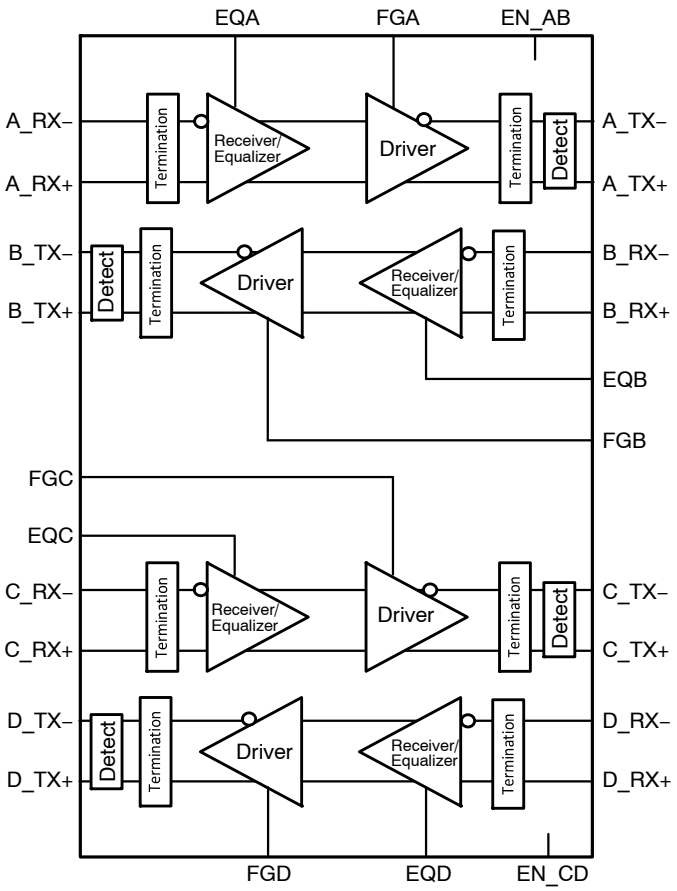


Figure 1. Logic Diagram of NB7NPQ1404E2M

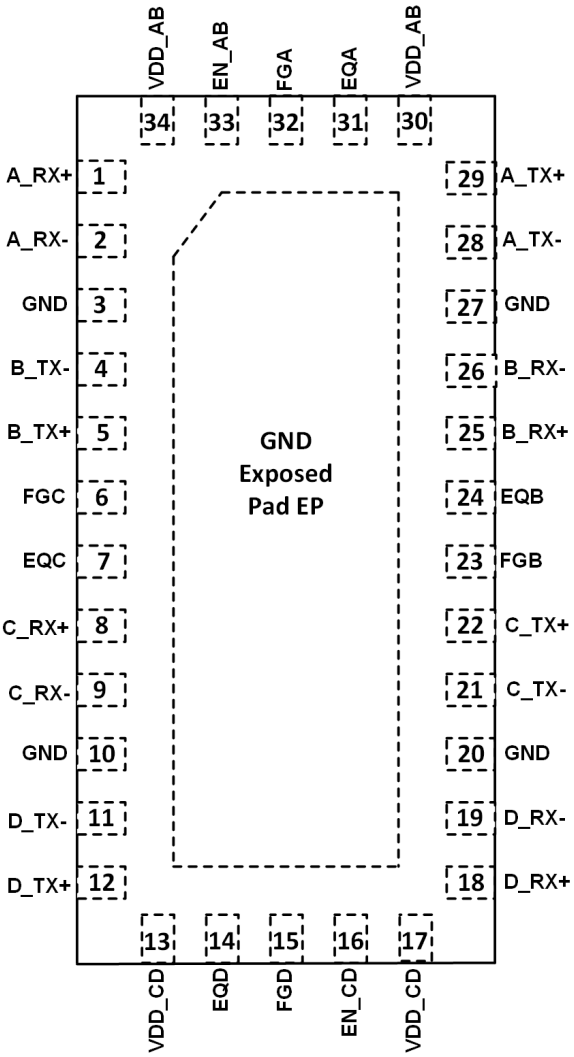


Figure 2. UQFN34 Package Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
1	A_RX+	INPUT	Channel A Differential CML input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system. UFP/DFP transmitter should provide this capacitor.
2	A_RX−		
3, 10, 10, 27	GND	GND	Reference Ground. GND pins must be externally connected to power supply ground to guarantee proper operation.
4	B_TX−	OUTPUT	Channel B Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system.
5	B_TX+		
6	FGC	INPUT	DC flat gain for channel C. 4−level input pin. Internal 100 kΩ pull−up and 200 kΩ pull−down.
7	EQC	INPUT	EQ select for channel C. 4−level input pin. Internal 100 kΩ pull−up and 200 kΩ pull−down.
8	C_RX+	INPUT	Channel C Differential CML input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system. UFP/DFP transmitter should provide this capacitor.
9	C_RX−		
11	D_TX−	OUTPUT	Channel D Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system.
12	D_TX+		
13, 17	VDD_CD	POWER	3.3 V power supply for Channel C and D. VDD pins must be externally connected to power supply.
14	EQD	INPUT	EQ select for channel D. 4−level input pin. Internal 100 kΩ pull−up and 200 kΩ pull−down.
15	FGD	INPUT	DC flat gain for channel D. 4−level input pin. Internal 100 kΩ pull−up and 200 kΩ pull−down.
16	EN_CD	INPUT	Channel CD Enable. Internal 300 kΩ pull−up. High−Channel is in normal operation. Low−Channel is in power down mode.
18	D_ RX+	INPUT	Channel D Differential CML input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system. UFP/DFP transmitter should provide this capacitor.
19	D_ RX−		
21	C_TX−	OUTPUT	Channel C Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system.
22	C_TX+		
23	FGB	INPUT	DC flat gain for channel B. 4−level input pin. Internal 100 kΩ pull−up and 200 kΩ pull−down.
24	EQB	INPUT	EQ select for channel B. 4−level input pin. Internal 100 kΩ pull−up and 200 kΩ pull−down.
25	B_ RX+	INPUT	Channel B Differential CML input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system. UFP/DFP transmitter should provide this capacitor.
26	B_ RX−		
28	A_TX−	OUTPUT	Channel A Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system.
29	A_TX+		
30, 34	VDD_AB	POWER	3.3 V power supply for Channel A and B. VDD pins must be externally connected to power supply.
31	EQA	INPUT	EQ select for channel A. 4−level input pin. Internal 100 kΩ pull−up and 200 kΩ pull−down.
32	FGA	INPUT	DC flat gain for channel A. 4−level input pin. Internal 100 kΩ pull−up and 200 kΩ pull−down.
33	EN_AB	INPUT	Channel AB Enable. Internal 300 kΩ pull−up. High−Channel is in normal operation. Low−Channel is in power down mode.
EP	GND	GND	Exposed Pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The exposed pad is electrically connected to the die and must be soldered to GND on the PC board.

Power Management

The NB7NPQ1404E2M has an adaptive power management feature in order to minimize power consumption. When the receiver signal detector is idle, the corresponding channel will change to low power slumber mode. Accordingly, both channels will move to low power slumber mode individually.

While in the low power slumber mode, the receiver signal detector will continue to monitor the input channel. If a channel is in low power slumber mode, the receiver detection loop will be active again. If a load is not detected, then the channel will move to Device Unplug Mode and continuously monitor for the load. When a load is detected, the channel will return to Low Power Slumber Mode and receiver detection will be active again per 6 ms.

Table 2. OPERATING MODES

Mode	R_{IN}	R_{OUT}
PD	67 kΩ to GND	High−Z
Unplug Mode	High−Z	40 kΩ to VDD
Low Power Slumber Mode	50 Ω to VDD	40 kΩ to VDD
Active	50 Ω to VDD	50 Ω to VDD

Table 3. EQUALIZATION SETTING
EQ A/B/C/D are the selection pins for the equalization.

EQA/B/C/D	Equalizer Setting (dB)	
	@2.5 GHz	@5 GHz
L (Tie 0−Ω to GND)	5.0	9.9
R (Tie Rext to GND)	2.7	6.9
F (Leave Open)	4.0	8.2 (Default)
H (Tie 0−Ω to VDD)	6.5	12.1

Table 4. FLAT GAIN SETTING
FGA/B/C/D are the selection pins for the DC gain.

FGA/B/C/D	Flat Gain Settings (dB)
L (Tie 0 Ω to GND)	−1.2
R (Tie Rext to GND)	−0.2
F (Leave Open)	+0.8 (Default)
H (Tie 0 Ω to VDD)	+1.8

Table 5. CHANNEL ENABLE SETTING
EN_AB / EN_CD are the channel enable pins for channels A&B and C&D respectively.

EN	Channel Enable Setting
0	Disabled
1	Enabled (Default)

Table 6. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	± 4 kV > 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Dry pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−O @ 0.125 in
Transistor Count		81034
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test		

1. For additional information, see Application Note AND8003/D.

Table 7. ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 2)	V_{DD}	−0.5	4.6	V
Voltage range at any input or output terminal	Differential I/O	−0.5	V_{DD} + 0.5	V
	LVCMOS inputs	−0.5	V_{DD} + 0.5	V
Output Current		−25	+25	mA
Power Dissipation, Continuous			1.2	W
Storage Temperature Range, T_{SG}		−65	150	°C
Maximum Junction Temperature, T_J			125	°C
Junction−to−Ambient Thermal Resistance @ 500 lfm, θ_{JA} (Note 3)			34	°C/W
Wave Solder, Pb−Free, T_{SOL}			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. All voltage values are with respect to the GND terminals.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 8. RECOMMENDED OPERATING CONDITIONS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description		Min	Typ	Max	Unit
V_{DD}	Main power supply		3.0	3.3	3.6	V
T_A	Operating free−air temperature	Industrial Temperature Range	−40		+85	°C
C_{AC}	AC coupling capacitor		75	100	265	nF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 9. POWER SUPPLY CHARACTERISTICS and LATENCY

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Unit
VDD	Supply Voltage		3.0	3.3	3.6	V
IDD_{Active}	Active mode current	EN_AB & EN_CD = 1, 10 Gbps, compliance test pattern		250	334	mA
$IDD_{LPSlumber}$	Low Power Slumber mode current	EN_AB & EN_CD = 1, no input signal longer than TLP-Slumber		0.8	1.3	mA
IDD_{Unplug}	Unplug mode current	EN_AB & EN_CD = 1, no output load is detected		0.5	0.8	mA
IDDpd	Power−down mode current	EN_AB & EN_CD = 0		50	100	μA
tpd	Latency	From Input to Output			2	ns

4. TYP values use VDD = 3.3 V, T_A = 25°C

Table 10. LVCMOS CONTROL PIN CHARACTERISTICS
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
2−Level Control Pins LVCMOS Inputs (EN_AB, EN_CD)						
V_{IH}	DC Input Logic High		0.65 x VDD	VDD	VDD	V
V_{IL}	DC Input Logic Low		GND	GND	0.35 x VDD	V
I_{IH}	High−level input current				25	μA
I_{IL}	Low−level input current		−25			μA
4−Level Control Pins LVCMOS Inputs (EQA/B/C/D, FGA/B/C/D)						
V_{IH}	DC Input Logic High; Setting “H”	Input pin connected to VDD	0.92 x VDD	VDD		V
V_{IF}	DC Input Logic 2/3 VDD; Setting “F”	Input pin is left floating (Open) (Note 5)	0.59 x VDD	0.67*VDD	0.75 x VDD	V
V_{IR}	DC Input Logic 1/3 VDD; Setting “R”	R_{ext} 68 kΩ must be between pin and GND	0.25 x VDD	0.33*VDD	0.41 x VDD	V
V_{IL}	DC Input Logic Low; Setting “L”	Input pin connected to GND		GND	0.08 x VDD	V
I_{IH}	High−level input current				50	μA
I_{IL}	Low−level input current		−50			μA
R_{ext}	External Resistor for input setting “R”	Rext connect to GND (±5%)	64.6	68	71.4	kΩ

5. Floating refers to a pin left in an open state, with no external connections.

Table 11. CML RECEIVER AC/DC CHARACTERISTICS
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{RX-DIFF-DC}$	Differential Input Impedance (DC)		72	100	120	Ω
$R_{RX-SINGLE-DC}$	Single−ended Input Impedance (DC)	Measured with respect to GND over a voltage of 500 mV max.	18		30	Ω
ZRX−HIZ−DC−PD	Common−mode input impedance for V>0 during reset or power−down (DC)	VCM = 0 to 500 mV	25			kΩ
Cac_coupling	AC coupling capacitance		75		265	nF
VRX−CM−AC−P	Common mode peak voltage	AC up to 5 GHz			150	mVpeak
VRX−CM−DC−Active −Idle−Delta−P	Rx AC common mode voltage during the U1 to U0 transition	Measured at Rx pins into a pair of 50 Ω terminations into ground. Includes Tx and channel conversion, AC range up to 5 GHz			200	mVpeak
VRX−CM−DC−Conn (Note 6, Note 7)	Instantaneous DC common mode voltage coupled from the far−end Tx	Apply to all link states and during power−on, and power−off when Rx termination is equivalent of 200 kΩ	−0.5		1	V
VRX−CM−DC−Conn (Note 6, Note 7)	Instantaneous DC common mode voltage coupled from the far−end Tx	Apply to all link states and during power−on, and power−off when Rx termination is 50 Ω	−0.3		1	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Not include +/−250 mV AC ground offset.
7. The receiver supports legacy implementations with VTX−DC+AC−CONN common mode transient up to 2.2 V.

Table 12. TRANSMITTER AC/DC CHARACTERISTICS
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Output differential p−p voltage swing at 100 MHz	Differential Swing $\|V_{TX-D+}-V_{TX-D-}\|$	0.8	1.0	1.2	V_{PPd}
$R_{TX-DIFF-DC}$	Differential TX impedance (DC)		72	100	120	Ω
$V_{TX-RCV-DET}$	Voltage change allowed during receiver detect				600	mV
Cac_coupling	AC coupling capacitance		75		265	nF
TTX−EYE(10 Gbps)	Transmitter eye, Include all jitter	At the silicon pad. 10 Gbps	0.646			UI
TTX−EYE(5 Gbps)	Transmitter eye, Include all jitter	At the silicon pad. 5 Gbps	0.625			UI
TTX−DJ−DD(10 Gbps)	Transmitter deterministic jitter	At the silicon pad. 10 Gbps			0.17	UI
TTX−DJ−DD(5 Gbps)	Transmitter deterministic jitter	At the silicon pad. 5 Gbps			0.205	UI
Ctxparasitic	Parasitic capacitor for TX				1.1	pF
RTX−DC−CM	Common−mode output impedance (DC)		18		30	Ω
VTX−DC−CM	Instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	200 kΩ single ended receiver load	−0.5		1	V
VTX−DC−CM	Instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	50 Ω single ended receiver load	−0.3		1	V
VTX−C	Common−mode voltage	$\|V_{TX-D+}+V_{TX-D-}\|/2$	VDD − 1.5		VDD	V
VTX−CM−AC−PP−Active	TX AC common−mode peak−to−peak voltage swing in active mode	$V_{TX-D+}+V_{TX-D-}$ for both time and amplitude			100	mV_{PP}

Table 12. TRANSMITTER AC/DC CHARACTERISTICS
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{TX-CM-DC-Active_Idle-Delta}$	Common mode delta voltage |AvgU0(|V_{TX-D+}+V_{TX-D-}|)/2 −AvgU1(|V_{TX-D+}+V_{TX-D-}|)/2|	Between U0 to U1			200	mVpeak
$V_{TX-Idle-DIFF-AC-pp}$	Idle mode AC common mode delta voltage |V_{TX-D+}−V_{TX-D-}|	Between TX+ and TX− in idle mode. Use the HPF to remove DC components. 1/LPF. No AC and DC signals are applied to RX terminals.			10	mVppd
$V_{TX-Idle-DIFF-DC}$	Idle mode DC common mode delta voltage |V_{TX-D+}−V_{TX-D-}|	Between TX+ and TX− in idle mode. Use the LPF to remove DC components. 1/HPF. No AC and DC signals are applied to RX terminals.			10	mV
CHANNEL PERFORMANCE						
Gp	Peaking gain (Compensation at 5 GHz, relative to 100 MHz, 100 mVp−p sine wave input)	EQx = L EQx = R EQx = F EQx = H		9.9 6.9 8.2 12.1		dB
		Variation around typical	−3		+3	dB
GF	Flat Gain (<100 MHz, EQx=F)	FGx = L FGx = R FGx = F FGx = H		−1.2 −0.2 +0.8 +1.8		dB
		Variation around typical	−3		+3	dB
V_{SW_100M}	−1 dB compression point output swing (100 MHz)			1000		mVppd
V_{SW_5G}	−1 dB compression point output swing (5 GHz)			800		mVppd
DDNEXT	Differential near−end crosstalk (Note 8)	100 MHz to 5 GHz, Figure 5		−40		dB
SIGNAL AND FREQUENCY DETECTORS						
Vth_dsm	Low power slumber mode detector threshold	LFPS signal threshold in Low power Slumber mode	100		600	mVppd
Vth_am	Active mode detector threshold	Signal threshold in Active and Slumber mode (Note 9)	45		175	mVppd

8. Measured using a vector network analyzer (VNA) with −15 dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50 Ω.
9. Below the minimum is no signal ≥ 25°C. Above the maximum is active.

PARAMETER MEASUREMENT DIAGRAMS

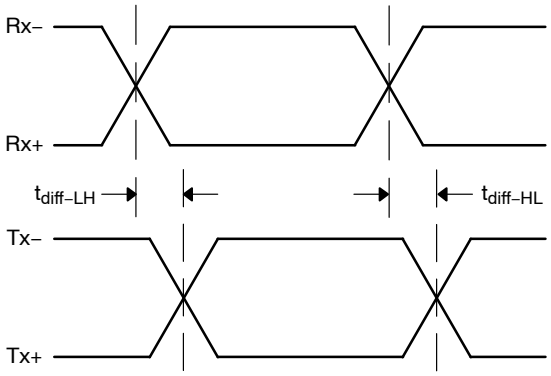


Figure 3. Propagation Delay

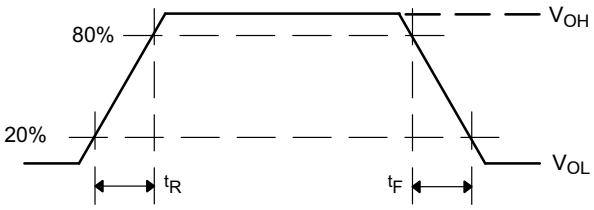


Figure 4. Output Rise and Fall Times

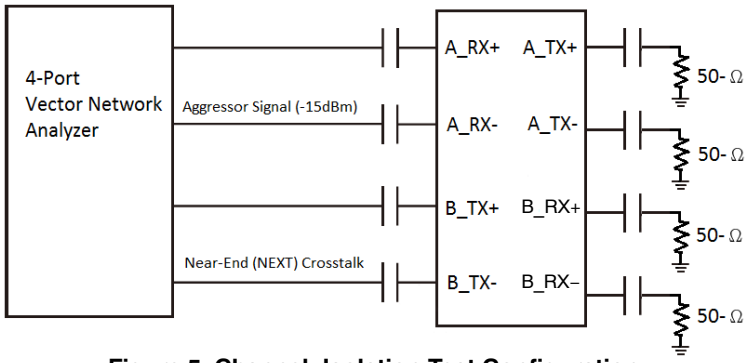


Figure 5. Channel−Isolation Test Configuration

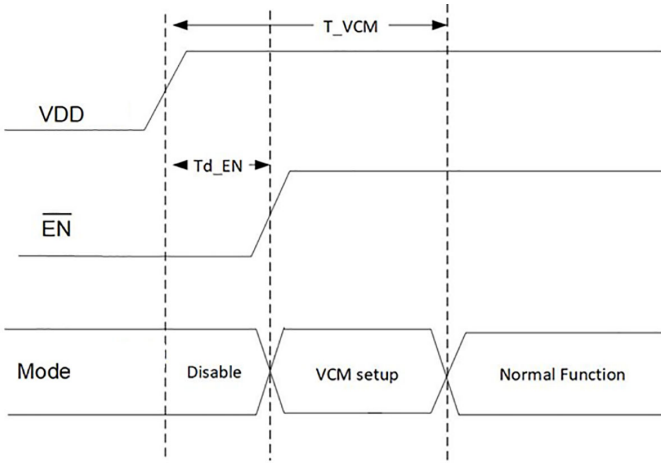


Figure 6. Power Up Timing

Table 13. POWER UP TIMING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Td_EN	VDD to Enable Assertion timing requirement	Figure 6.	0			ms
T_VCM	Stabilization time for VCM	Figure 6.		330	400	ms

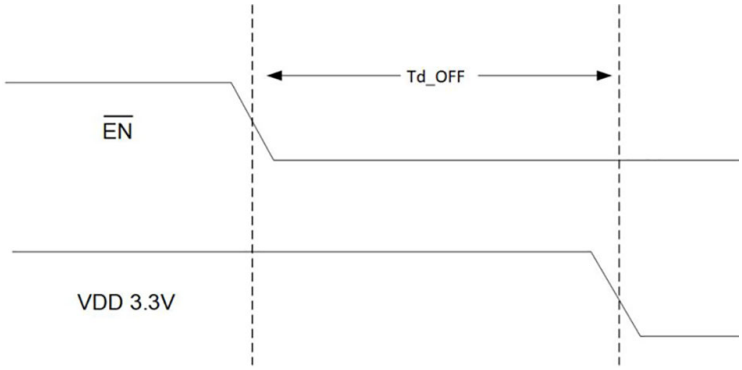


Figure 7. Power Down Timing

Table 14. POWER DOWN TIMING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Td_OFF	Delay time required from EN de−assertion until VDD is powered off	Figure 7.	900			ms

APPLICATION GUIDELINES

LFPS Compliance Testing

As part of USB 3.2 compliance test, the host or peripheral must transmit a LFPS signal that adheres to the spec parameters. The NB7NPQ1404E2M is tested as a part of a USB compliant system to ensure that it maintains compliance while increasing system performance.

LFPS Functionality

USB 3.2 Low Frequency Periodic Signaling.

(LFPS) to implement functions like exiting low−power modes, performing warm resets and providing link training between host and peripheral devices. LFPS signaling consists of bursts of frequencies ranging between 10 to 50 MHz and can have specific burst lengths or repeat rates.

Ping.LFPS for TX Compliance

During the transmitter compliance, the system under test must transmit certain compliance patterns as defined by the USB−IF. In order to toggle through these patterns for various tests, the receiver must receive a ping.LFPS signal from either the test suite or a separate pattern generator. The standard signal comprises of a single burst period of 100 ns at 20 MHz.

Control Pin Settings

Control pins A1, A0, B1, and B0 control the Flat Gain and the Equalization of channels A and B and control pins C1, C0, D1, and D0 control the Flat Gain and the Equalization of channels C and D of the NB7NPQ1404E2M Device.

The Float (Default) Setting “F” can be set by leaving the control pins in a floating state. The Redriver will internally bias the control pins to the correct voltage to achieve this if the pin is not connected to a voltage source. The low Setting “L” is set by pulling the control pin to ground. Likewise the high setting “H” is set by pulling the pin high to VCC. The $R_{external}$ setting can be set by adding a 68 kΩ resistor from the control pin to ground. This will bias the Redriver internal voltage to 33% of VCC.

Linear Equalization

The linear equalization that the NB7NPQ1404E2M provides compensates for losses that occur naturally along board traces and cable lines. Linear Equalization boosts high frequencies and lower frequencies linearly so when transmitting at varying frequencies, the voltage amplitude will remain consistent. This compensation electrically counters losses and allows for longer traces to be possible when routing.

DC Flat Gain

DC flat gain equally boosts high and low frequency signals, and is essential for countering low frequency losses.

DC flat gain can also be used to simulate a higher input signal from a USB Controller. If a USB controller can only provide 800 mV differential to a receiver, it can be boosted to 1128 mV using 2 dB of flat gain.

Total Gain

When using Flat Gain with Equalization in a USB application it is important to make sure that the total voltage does not exceed 1200 mV. Total gain can be calculated by adding the EQ gain to the FG.

Typical Layout Practices

- RX and TX pairs should maintain as close to a 90 Ω differential impedance as possible.
- Limit the number of vias used on each data line. It is suggested that two or fewer are used.
- Traces should be routed as straight and symmetric as possible.
- RX and TX differential pairs should always be placed and routed on the same layer directly above a ground plane. This will help reduce EMI and noise on the data lines.
- Routing angles should be obtuse angles and kept to 135 degrees or larger.
- To minimize crosstalk, TX and RX data lines should be kept away from other high speed signals.

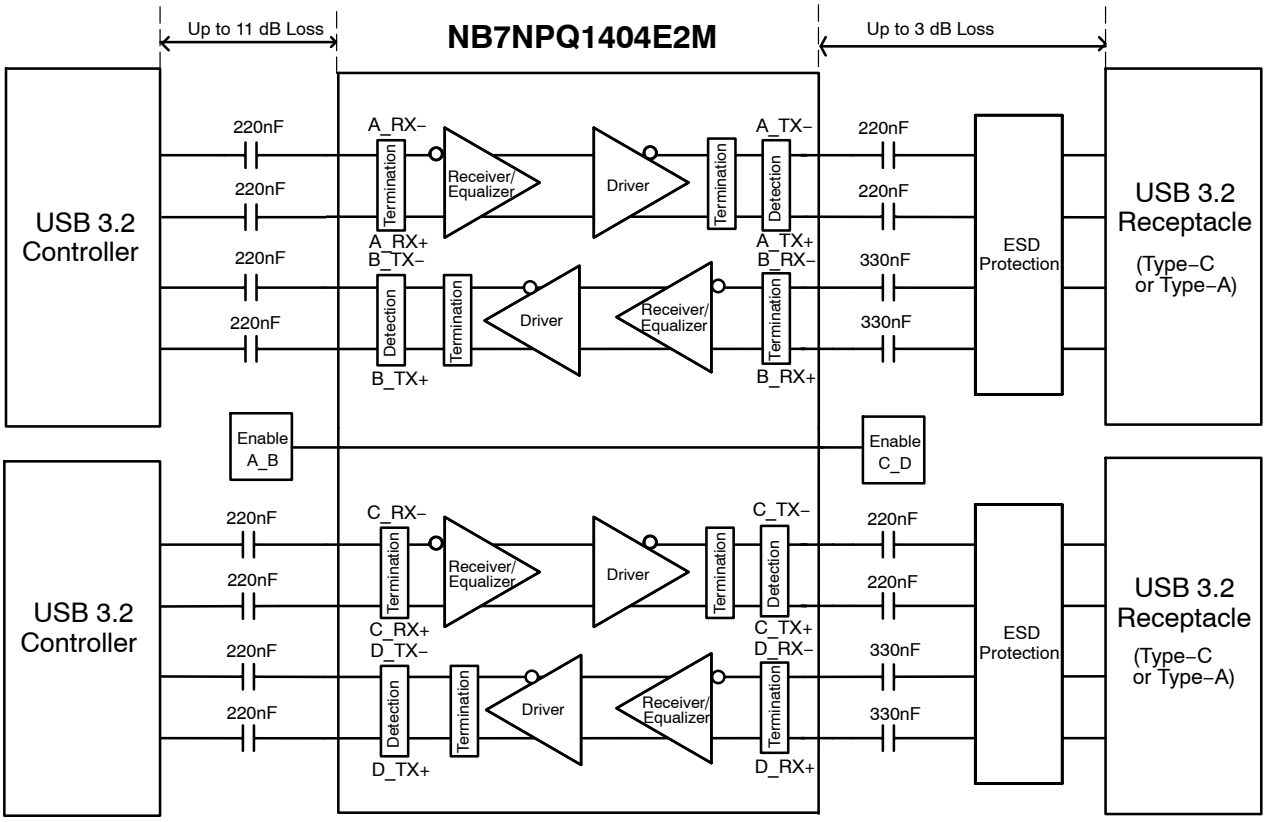
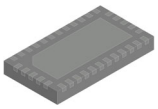


Figure 8. Typical Application

Table 15. DESIGN REQUIREMENTS

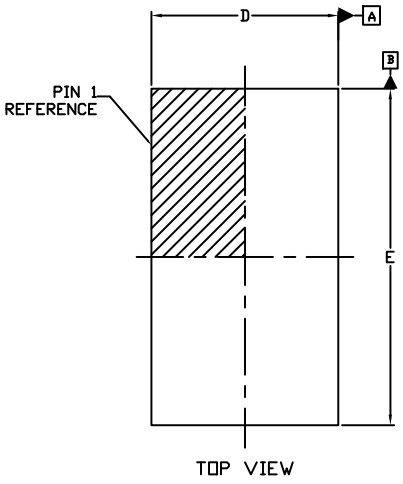
Design Parameter	Value
Supply Voltage	3.3 V nominal, (3.0 V to 3.6 V)
Operation Mode (Control Pin Selection)	Floating by Default, adjust for application losses
TX AC Coupling Capacitors	220 nF nominal, 75 nF to 265 nF, see Figure 8
RX AC Coupling Capacitors	330 – 470 nF nominal, see Figure 8
Power Supply Capacitors	100 nF to GND close to each VCC pin, and 10 mF to GND on the VCC plane
Trace loss of FR4 before NB7NPQ1404E2M (Note 10)	Up to 11 dB Losses
Trace loss of FR4 after NB7NPQ1404E2M (Note 10)	Up To 3 dB Losses. Keep as short as possible for best performance.
Linear Range at 5 GHz	900 mV differential
DC Flat Gain Options	−1.2 dB, −0.2 dB, +0.8 dB, +1.8 dB
Equalization Options	6.9 to 12.1 dB
Differential Trace Impedance	90 Ω ±10%

10. Trace loss of FR4 was estimated to have 1 dB of loss per 1 inch of FR4 length with matched impedance and no VIAS.

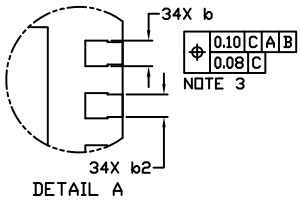


UQFN34 2.5x4.5, 0.35P
CASE 523BR
ISSUE A

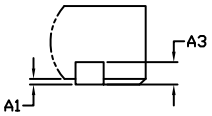
DATE 10 DEC 2020

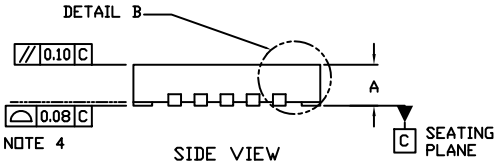


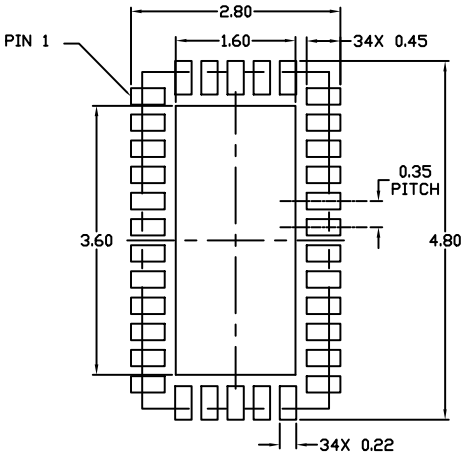
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



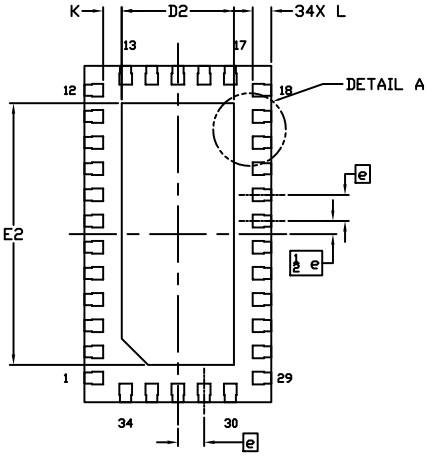
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0.00	---	0.05
A3		0.15 REF	
b	0.12	0.17	0.22
b2	0.10	0.15	0.20
D	2.40	2.50	2.60
D2	1.40	1.50	1.60
E	4.40	4.50	4.60
E2	3.40	3.50	3.60
e		0.35 BSC	
K		0.25 REF	
L	0.15	0.25	0.35



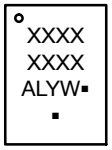




* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



GENERIC
MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**UQFN34 2.5x4.5, 0.35P**	**PAGE 1 OF 1**

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