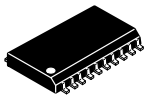
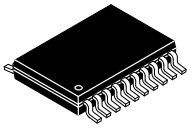
Octal D-Type Flip-Flop with Clear

MM74HCT273



SOIC−20 WB
CASE 751D−05



TSSOP−20 WB
CASE 948E

General Description

The MM74HCT273 utilizes advanced silicon−gate CMOS technology. It has an input threshold and output drive similar to LS−TTL with the low standby power of CMOS.

These positive edge−triggered flip−flops have a common clock and clear−independent Q outputs. Data on a D input, having the specified set−up and hold time, is transferred to the corresponding Q output on the positive−going transition of the clock pulse. The asynchronous clear forces all outputs LOW when it is LOW.

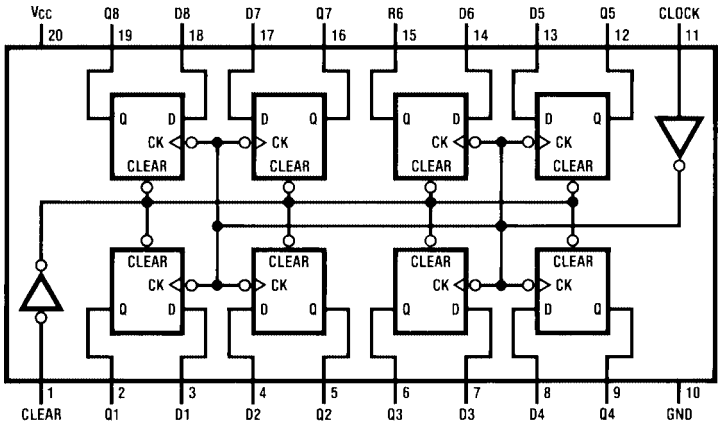
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. These parts can be used as plug−in replacements to reduce system power consumption in existing designs.

Features

- Typical Propagation Delay: 18 ns
- Low Quiescent Current: 160 μA Maximum (74HCT Series)
- Fanout of 10 LS−TTL Loads
- This is a Pb−Free Device

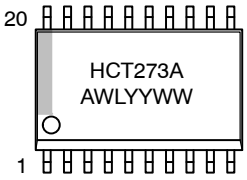
Connection Diagram



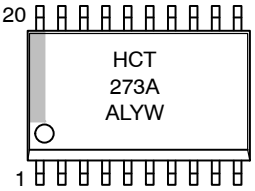
Top View

Figure 1. Pin Assignments for SOIC and TSSOP

MARKING DIAGRAM



SOIC−20



TSSOP−20 WB

HCT273A	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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TRUTH TABLE (Each Flip−Flop)

Inputs			Outputs
Clear	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

NOTE: H = HIGH Level (steady−state)
L = LOW Level (steady−state)
X = Don't Care
↑ = Transition from LOW−to−HIGH level
Q0 = The level of Q before the indicated steady−state input conditions were established.

Logic Diagram

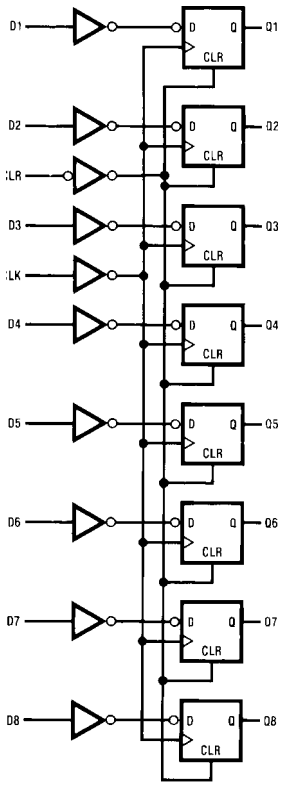


Figure 2. Logic Diagram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Rating
V_{CC}	Supply Voltage		–0.5 to +7.0 V
V_{IN}	DC Input Voltage		–0.5 to V_{CC} + 0.5 V
V_{OUT}	DC Output Voltage		–0.5 to V_{CC} + 0.5 V
I_{IK}, I_{OK}	Clamp Diode Current		±20 mA
I_{OUT}	DC Output Current, per Pin		±25 mA
I_{CC}	DC V_{CC} or GND Current, per Pin		±50 mA
T_{STG}	Storage Temperature Range		–65°C to +150°C
P_D	Power Dissipation	S.O. Package only	500 mW
T_L	Lead Temperature (Soldering 10 Seconds)		260°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–55	+125	°C
t_r, t_f	Input Rise or Fall Times		500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		T_A = −40°C to 85°C	T_A = −55°C to 125°C	Unit
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		–	2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage		–	0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5 V	4.2	3.98	3.84	3.7	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5 V	5.2	4.98	4.84	4.7	V
V_{OL}	Minimum LOW Level Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5 V	0.2	0.26	0.33	0.4	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5 V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}	–	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA	–	8	80	160	μA
		V_{IN} = 2.4 V or 0.5 V (Note 2)	–	0.6	0.8	0.9	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Measured per pin, all other inputs held at V_{CC} or GND.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency		68	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		21	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−1	5	ns
t_S	Minimum Set−Up Time D to Clock		6	20	ns
t_H	Minimum Hold Time Clock to D		−3	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified))

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C		Unit
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		68	27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		22	37	46	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		25	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock		−1	5	6	7	ns
t_S	Minimum Set−Up Time D to Clock		6	20	25	30	ns
t_H	Minimum Hold Time Clock to D		−3	5	5	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	25	30	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		–	500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		11	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 3)	(Per Flip−Flop)	50	–	–	–	pF
C_{IN}	Maximum Input Capacitance		6	10	10	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}^2\ f + I_{CC}$.

ORDERING INFORMATION

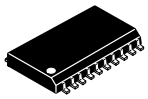
Part Number	Package	Shipping†
MM74HCT273WM	SOIC−20 WB, Case 751D−05 (Pb−Free and Halide−Free)	38 Units / Tube
MM74HCT273WMX		1000 Units / Tape & Reel
MM74HCT273MTC	TSSOP−20 WB, Case 948E (Pb−Free)	75 Units / Tube
MM74HCT273MTCX		2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



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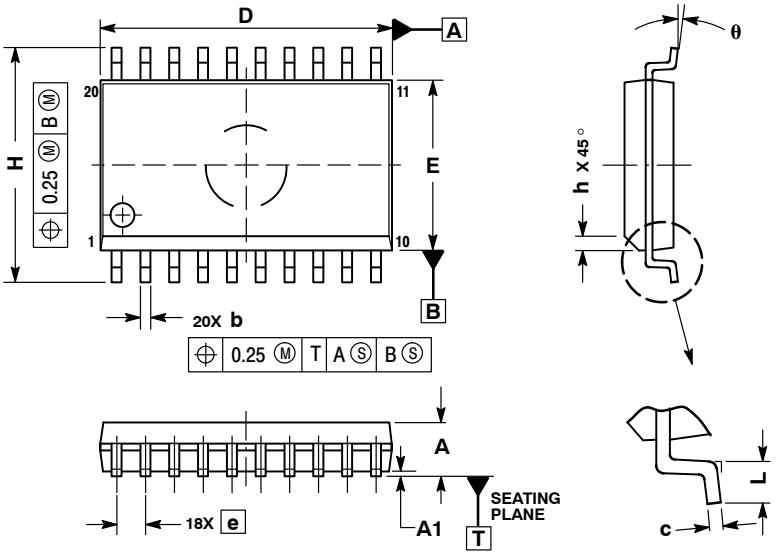
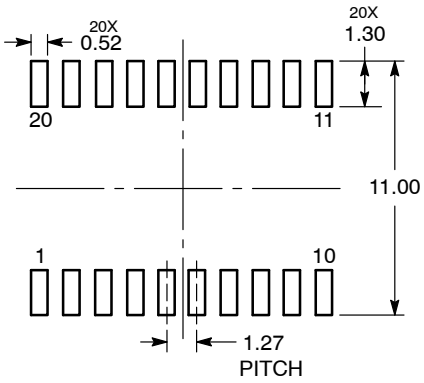


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

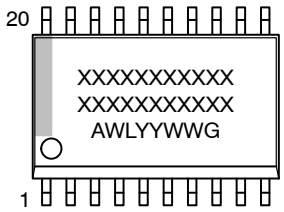
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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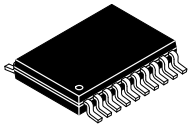
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016



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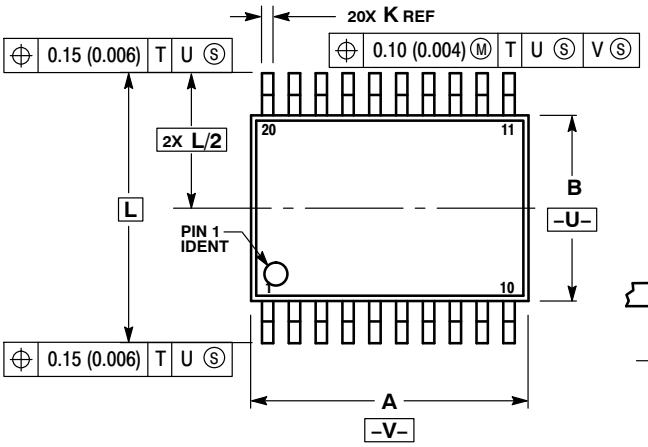

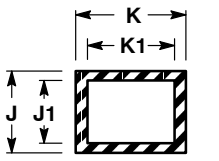

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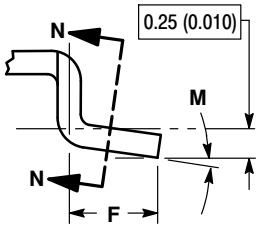
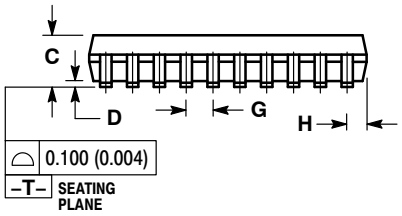
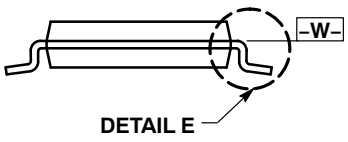


DETAIL E

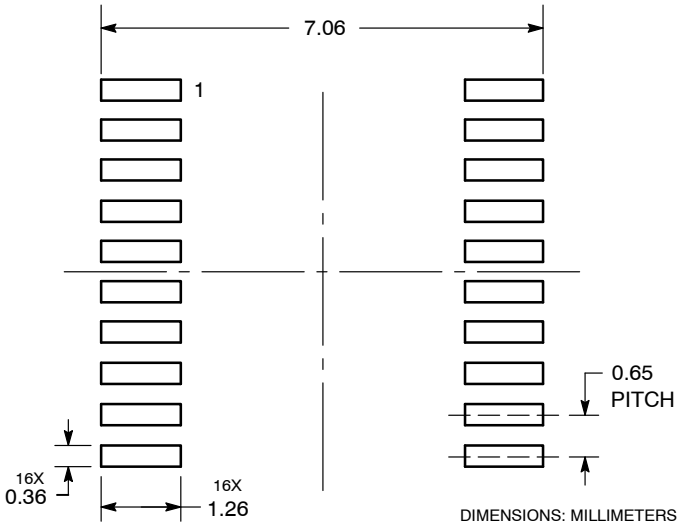




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

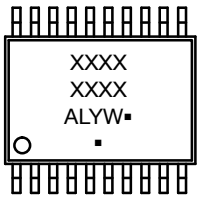
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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