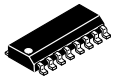
# 8-Stage Shift/Store Register with Three-State Outputs

# MC14094B



SOIC−16
D SUFFIX
CASE 751B



TSSOP−16
DT SUFFIX
CASE 948F

The MC14094B combines an 8−stage shift register with a data latch for each stage and a 3−state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The $Q_S$ output data is for use in high−speed cascaded systems. The $Q_S$ output data is shifted on the following negative clock transition for use in low−speed cascaded systems.

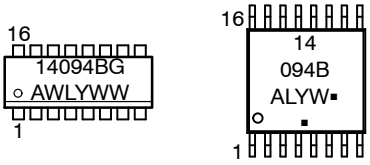
Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by 3−state buffers which are placed in the high−impedance state by a logic Low on Output Enable.

### Features

- 3−State Outputs
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial−to−Parallel Data Conversion
- Pin−for−Pin Compatible with CD4094B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

### MARKING DIAGRAMS




SOIC−16 TSSOP−16

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Indicator

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

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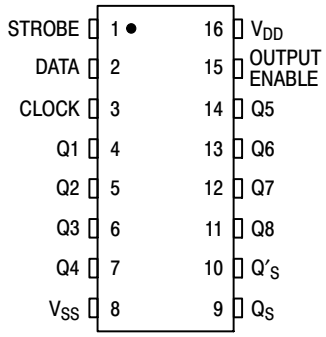
## PIN ASSIGNMENT




## TRUTH TABLE

| Clock | Output Enable | Strobe | Data | Parallel Outputs | | Serial Outputs | |
|---|---|---|---|---|---|---|---|
| | | | | Q1 | $Q_N$ | $Q_S$* | $Q'_S$ |
| ↗ | 0 | X | X | Z | Z | Q7 | No Chg. |
| ↘ | 0 | X | X | Z | Z | No Chg. | Q7 |
| ↗ | 1 | 0 | X | No Chg. | No Chg. | Q7 | No Chg. |
| ↗ | 1 | 1 | 0 | 0 | $Q_N$–1 | Q7 | No Chg. |
| ↗ | 1 | 1 | 1 | 1 | $Q_N$–1 | Q7 | No Chg. |
| ↘ | 1 | 1 | 1 | No Chg. | No Chg. | No Chg. | Q7 |

Z = High Impedance X = Don't Care

* At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and $Q_S$.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC14094BDG | SOIC–16 (Pb–Free) | 48 Units / Rail |
| MC14094BDR2G | SOIC–16 (Pb–Free) | 2500 Units / Tape & Reel |
| NLV14094BDR2G* | SOIC–16 (Pb–Free) | 2500 Units / Tape & Reel |
| MC14094BDTR2G | TSSOP–16 (Pb–Free) | 2500 Units / Tape & Reel |
| NLV14094BDTR2G* | TSSOP–16 (Pb–Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | −55°C Min | −55°C Max | 25°C Min | 25°C Typ (Note 2) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0<br>0<br>0 | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | Vdc |
| “1” Level<br>$V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0<br>10<br>15 | 4.95<br>9.95<br>14.95 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | 5.0<br>10<br>15 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | –<br>–<br>– | Vdc |
| Input Voltage “0” Level<br>($V_O$ = 4.5 or 0.5 Vdc)<br>($V_O$ = 9.0 or 1.0 Vdc)<br>($V_O$ = 13.5 or 1.5 Vdc) | $V_{IL}$ | <br>5.0<br>10<br>15 | <br>–<br>–<br>– | <br>1.5<br>3.0<br>4.0 | <br>–<br>–<br>– | <br>2.25<br>4.50<br>6.75 | <br>1.5<br>3.0<br>4.0 | <br>–<br>–<br>– | <br>1.5<br>3.0<br>4.0 | Vdc |
| “1” Level<br>($V_O$ = 0.5 or 4.5 Vdc)<br>($V_O$ = 1.0 or 9.0 Vdc)<br>($V_O$ = 1.5 or 13.5 Vdc) | $V_{IH}$ | <br>5.0<br>10<br>15 | <br>3.5<br>7.0<br>11 | <br>–<br>–<br>– | <br>3.5<br>7.0<br>11 | <br>2.75<br>5.50<br>8.25 | <br>–<br>–<br>– | <br>3.5<br>7.0<br>11 | <br>–<br>–<br>– | Vdc |
| Output Drive Current<br>($V_{OH}$ = 2.5 Vdc) Source<br>($V_{OH}$ = 4.6 Vdc)<br>($V_{OH}$ = 9.5 Vdc)<br>($V_{OH}$ = 13.5 Vdc) | $I_{OH}$ | <br>5.0<br>5.0<br>10<br>15 | <br>–3.0<br>–0.64<br>–1.6<br>–4.2 | <br>–<br>–<br>–<br>– | <br>–2.4<br>–0.51<br>–1.3<br>–3.4 | <br>–4.2<br>–0.88<br>–2.25<br>–8.8 | <br>–<br>–<br>–<br>– | <br>–1.7<br>–0.36<br>–0.9<br>–2.4 | <br>–<br>–<br>–<br>– | mAdc |
| ($V_{OL}$ = 0.4 Vdc) Sink<br>($V_{OL}$ = 0.5 Vdc)<br>($V_{OL}$ = 1.5 Vdc) | $I_{OL}$ | 5.0<br>10<br>15 | 0.64<br>1.6<br>4.2 | –<br>–<br>– | 0.51<br>1.3<br>3.4 | 0.88<br>2.25<br>8.8 | –<br>–<br>– | 0.36<br>0.9<br>2.4 | –<br>–<br>– | mAdc |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc |
| Input Capacitance<br>($V_{in}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current<br>(Per Package) | $I_{DD}$ | 5.0<br>10<br>15 | –<br>–<br>– | 5.0<br>10<br>20 | –<br>–<br>– | 0.005<br>0.010<br>0.015 | 5.0<br>10<br>20 | –<br>–<br>– | 150<br>300<br>600 | μAdc |
| Total Supply Current (Notes 3 & 4)<br>(Dynamic plus Quiescent, Per Package)<br>($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0<br>10<br>15 | $I_T$ = (4.1 μA/kHz) f + $I_{DD}$<br>$I_T$ = (14 μA/kHz) f + $I_{DD}$<br>$I_T$ = (140 μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |
| 3−State Output Leakage Current | $I_{TL}$ | 15 | – | ±0.1 | – | ±0.0001 | ±0.1 | – | ±3.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in μA (per package), $C_L$ in pF, V = ($V_{DD}$ − $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

**SWITCHING CHARACTERISTICS** (Note 5) ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$, | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.35 ns/pF) $C_L$ + 33 ns | $t_{THL}$ | 5.0 | – | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.6 ns/pF) $C_L$ + 20 ns | | 10 | – | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.4 ns/pF) $C_L$ + 20 ns | | 15 | – | 40 | 80 | |
| Propagation Delay Time (Figure 1) | $t_{PLH}$, | | | | | ns |
| Clock to Serial out QS | $t_{PHL}$ | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (0.90 ns/pF) $C_L$ + 305 ns | | 5.0 | – | 350 | 600 | |
| $t_{PLH}$, $t_{PHL}$ = (0.36 ns/pF) $C_L$ + 107 ns | | 10 | – | 125 | 250 | |
| $t_{PLH}$, $t_{PHL}$ = (0.26 ns/pF) C L + 82 ns | | 15 | – | 95 | 190 | |
| Clock to Serial out Q'S | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (0.90 ns/pF) $C_L$ + 350 ns | | 5.0 | – | 230 | 460 | |
| $t_{PLH}$, $t_{PHL}$ = (0.36 ns/pF) $C_L$ + 149 ns | | 10 | – | 110 | 220 | |
| $t_{PLH}$, $t_{PHL}$ = (0.26 ns/pF) $C_L$ + 62 ns | | 15 | – | 75 | 150 | |
| Clock to Parallel out | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (0.90 ns/pF) $C_L$ + 375 ns | | 5.0 | – | 420 | 840 | |
| $t_{PLH}$, $t_{PHL}$ = (0.35 ns/pF) $C_L$ + 177 ns | | 10 | – | 195 | 390 | |
| $t_{PLH}$, $t_{PHL}$ = (0.26 ns/pF) $C_L$ + 122 ns | | 15 | – | 135 | 270 | |
| Strobe to Parallel out | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (0.90 ns/pF) $C_L$ + 245 ns | | 5.0 | – | 290 | 580 | |
| $t_{PLH}$, $t_{PHL}$ = (0.36 ns/pF) C L + 127 ns | | 10 | – | 145 | 290 | |
| $t_{PLH}$, $t_{PHL}$ = (0.26 ns/pF) $C_L$ + 87 ns | | 15 | – | 100 | 200 | |
| Output Enable to Output | | | | | | |
| $t_{PHZ}$, $t_{PZL}$ = (0.90 ns/pF) $C_L$ + 95 ns | $t_{PHZ}$, | 5.0 | – | 140 | 280 | |
| $t_{PHZ}$, $t_{PZL}$ = (0.36 ns/PF) $C_L$ + 57 ns | $t_{PZL}$ | 10 | – | 75 | 150 | |
| $t_{PHZ}$, $t_{PZL}$ = (0.26 ns/pF) $C_L$ + 42 ns | | 15 | – | 55 | 110 | |
| $t_{PLZ}$, $t_{PZH}$ = (0.90 ns/pF) $C_L$ + 180 ns | $t_{PLZ}$, | 5.0 | – | 225 | 450 | |
| $t_{PLZ}$, $t_{PZH}$ = (0.36 ns/pF) $C_L$ + 77 ns | $t_{PZH}$ | 10 | – | 95 | 190 | |
| $t_{PLZ}$, $t_{PZH}$ = (0.26 ns/pF) $C_L$ + 57 ns | | 15 | – | 70 | 140 | |
| Setup Time | $t_{su}$ | 5.0 | 125 | 60 | – | ns |
| Data in to Clock | | 10 | 55 | 30 | – | |
| | | 15 | 35 | 20 | – | |
| Hold Time | $t_h$ | 5.0 | 0 | – 40 | – | ns |
| Clock to Data | | 10 | 20 | – 10 | – | |
| | | 15 | 20 | 0 | – | |
| Clock Pulse Width, High | $t_{WH}$ | 5.0 | 200 | 100 | – | ns |
| | | 10 | 100 | 50 | – | |
| | | 15 | 83 | 40 | – | |
| Clock Rise and Fall Time | $t_{r(cl)}$ | 5 | – | – | 15 | μs |
| | $t_{f(cl)}$ | 10 | – | – | 5.0 | |
| | | 15 | – | – | 4.0 | |
| Clock Pulse Frequency | $f_{cl}$ | 5.0 | – | 2.5 | 1.25 | MHz |
| | | 10 | – | 5.0 | 2.5 | |
| | | 15 | – | 6.0 | 3.0 | |
| Strobe Pulse Width | $t_{WL}$ | 5.0 | 200 | 100 | – | ns |
| | | 10 | 80 | 40 | – | |
| | | 15 | 70 | 35 | – | |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## 3–STATE TEST CIRCUIT

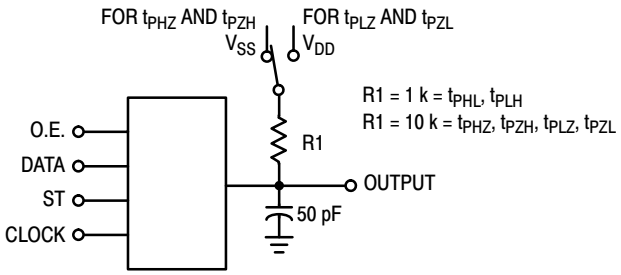
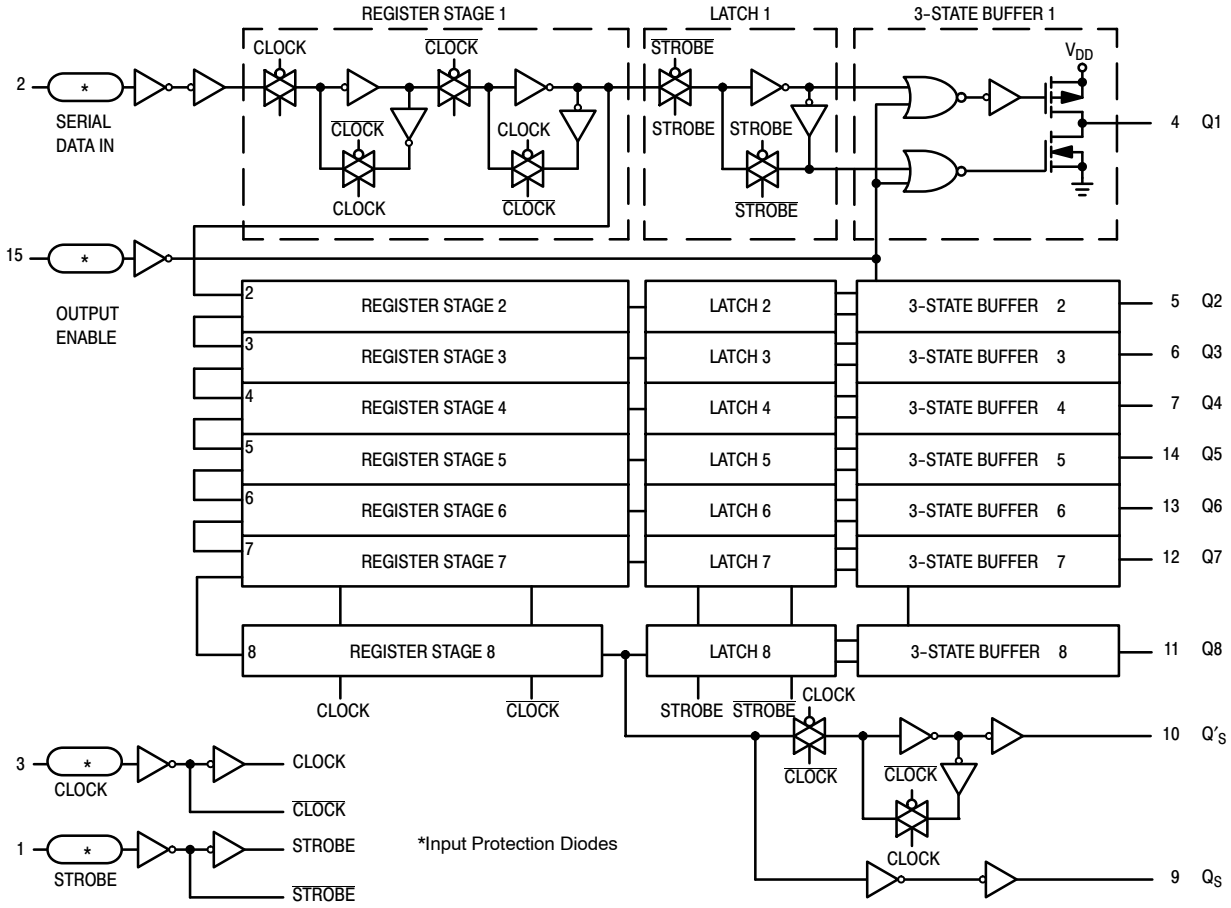
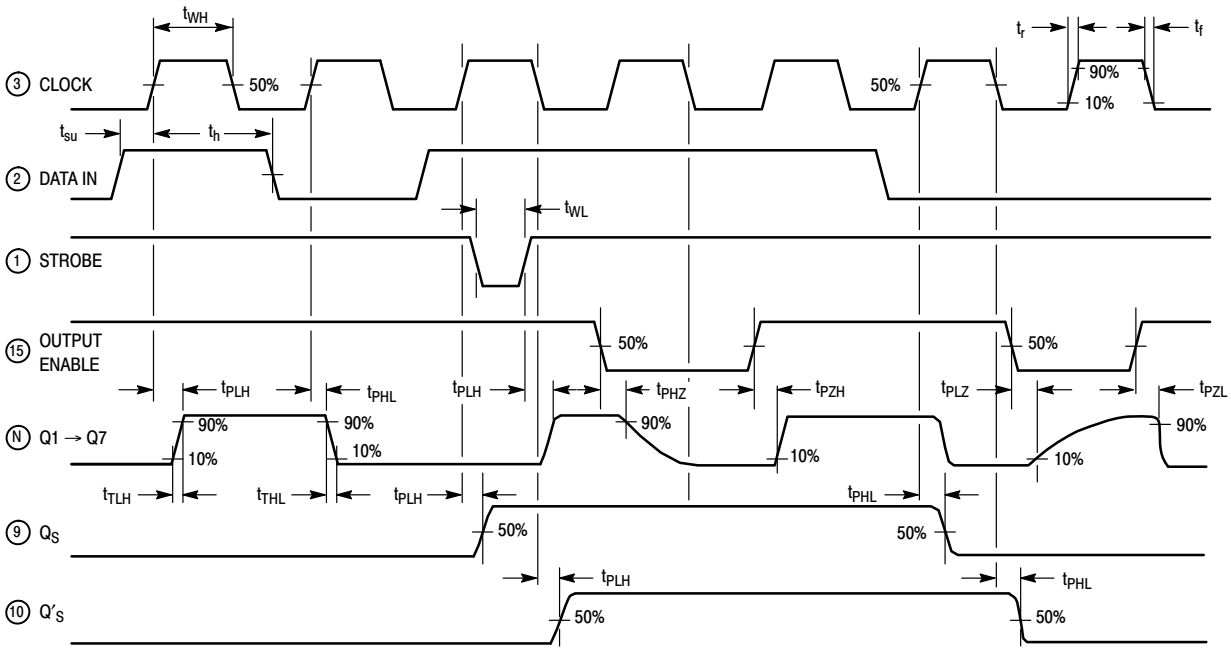


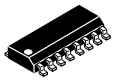

**Figure 1.**

## BLOCK DIAGRAM



## DYNAMIC TIMING DIAGRAM

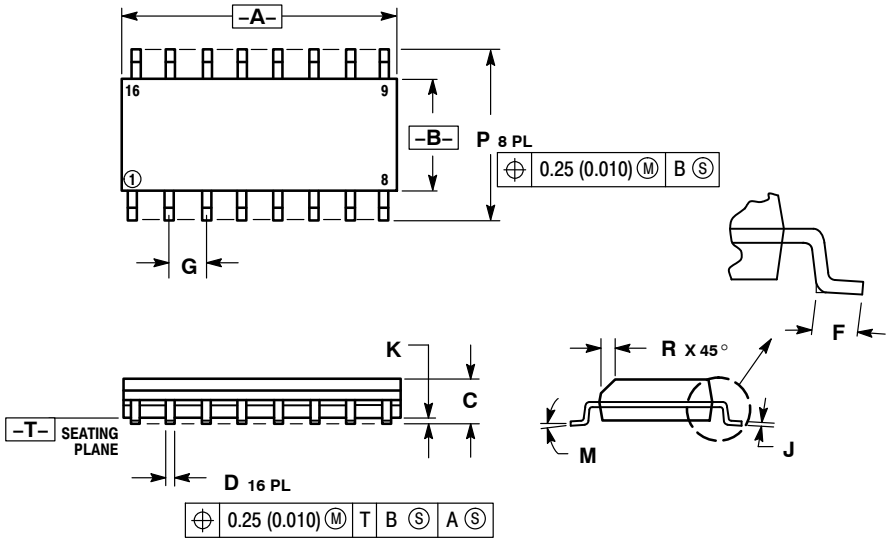




SCALE 1:1

**SOIC–16**
CASE 751B–05
ISSUE K

DATE 29 DEC 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

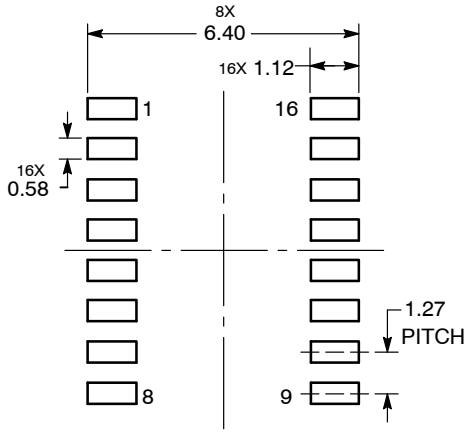
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

**SOLDERING FOOTPRINT**




DIMENSIONS: MILLIMETERS

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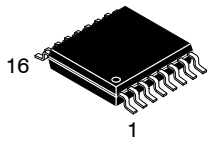
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

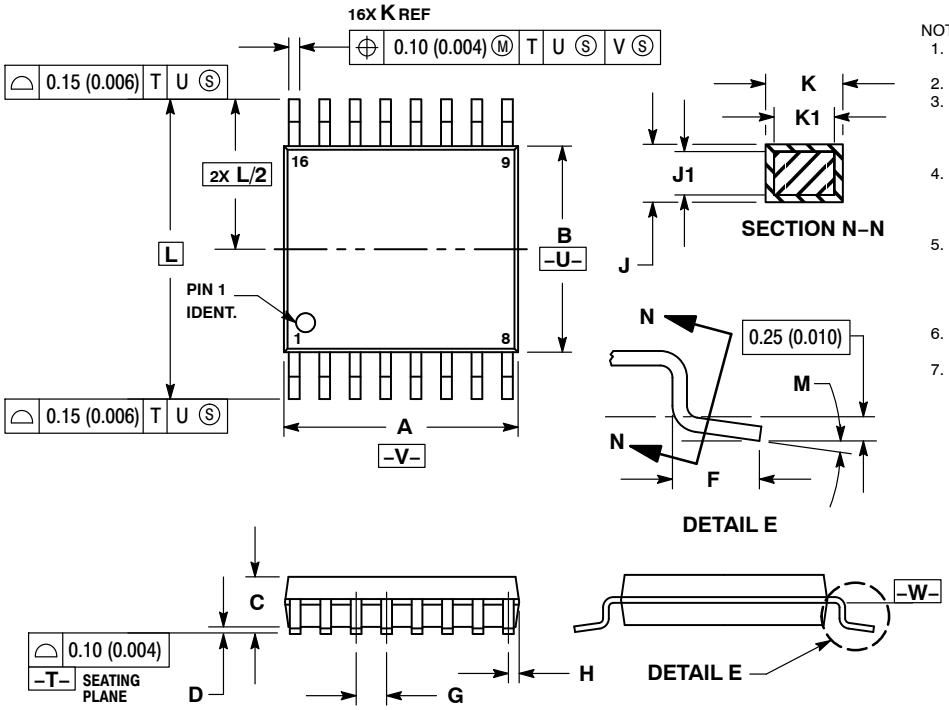
ON Semiconductor®




SCALE 2:1

**TSSOP−16**
CASE 948F−01
ISSUE B

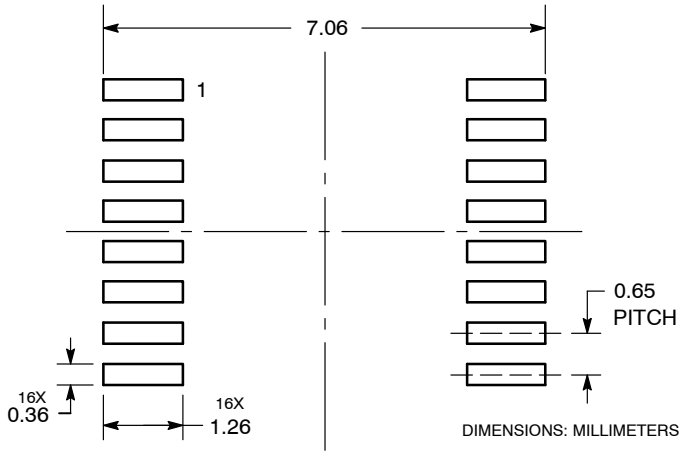
DATE 19 OCT 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

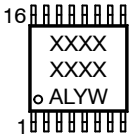
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or ▪ | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
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| DESCRIPTION: | TSSOP−16 | PAGE 1 OF 1 |

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