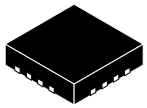
USB Type-C Port Controller with USB-PD

FUSB307B



SCALE 3:1
WQFN16 3 x 3, 0.5P
CASE 510BS

Description

The FUSB307B targets system designers looking to implement up to four USB Type−C port controllers (TCPC) with USB−PD capabilities.

This solution provides integrated Type−C Rev 1.3 detection circuitry enabling manual attach/detach detection. Time critical Power Delivery functionality is handled autonomously, offloading the µProcessor or Type−C Port Manager (TCPM).

The FUSB307B complies with the USB−PD Interface Specification Rev 1.0 as a TCPC for a standardized interface with TCPM.

Features

- USB−PD Interface Specification Rev 1.0 Ver. 1.2 Compatible
- USB Type−C Rev 1.3 Compatible
- USB−PD Rev3.0 Ver. 1.1 Compatible
- Fast Role Swap
- Sink Transmit
- Extended Data Messages (Chunked)
- Dual−Role Functionality
  - Manual Type−C Detection
  - Automatic DRP Toggling
- USB−PD Interface Specification Support
  - Automatic GoodCRC Packet Response
  - Automatic Retries of Sending Packet
  - All SOP* Types Supported
- VBUS Source and Sink Control
- Integrated 3 W Capable VCONN to CCx Switch
- 10−bit VBUS ADC
- Programmable GPIOs
- 4 Selectable I^2C Addresses

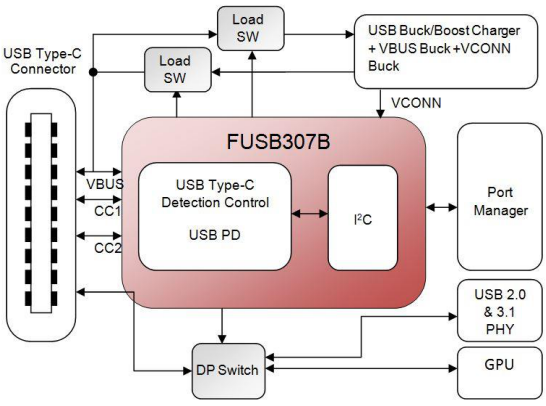
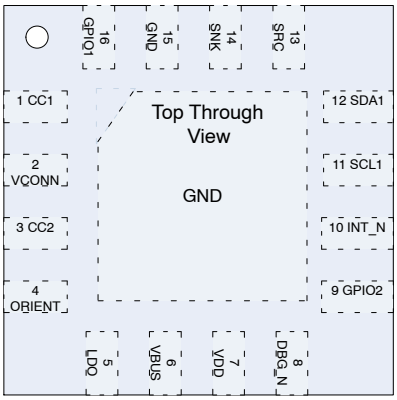


Figure 1. FUSB307B Block Diagram

PIN ASSIGNMENT



QFN16

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

Features (continued)

- Dead Battery Operation
  - Powered from VBUS
  - LDO Output Provides Power to TCPM
- Packaging:
  - FUSB307B− 16 Pin QFN

Applications

- Smartphones and Tablets
- Digital Cameras
- Desktops and Laptops
- Rechargeable Docks/Speakers
- Wall Adapters
- Automotive

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Table 1. ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method†
FUSB307BMPX	−40 to 85°C	16−Lead Molded Leadless Package (QFN) JEDEC, ML220, 3 mm Square	Tape and Reel
FUSB307BVMPX	Automotive −40 to 105°C		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Application

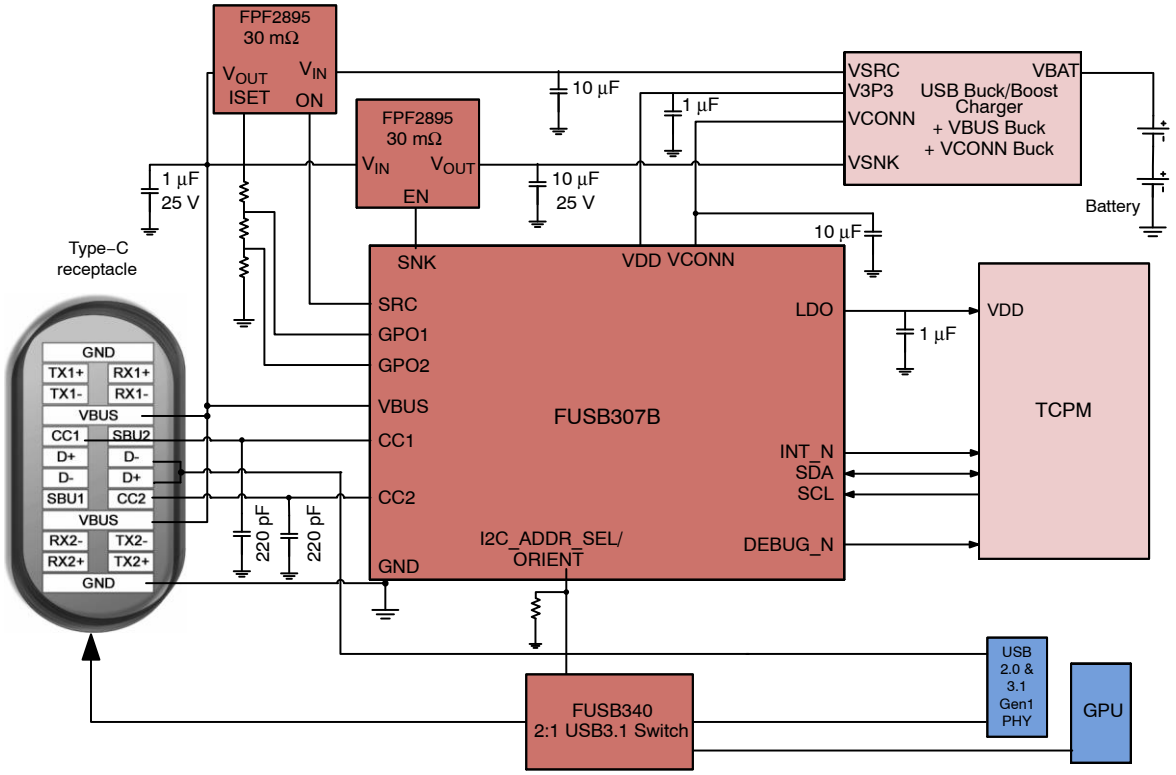


Figure 2. FUSB307B Typical Mobile Computing Application

Block Diagram

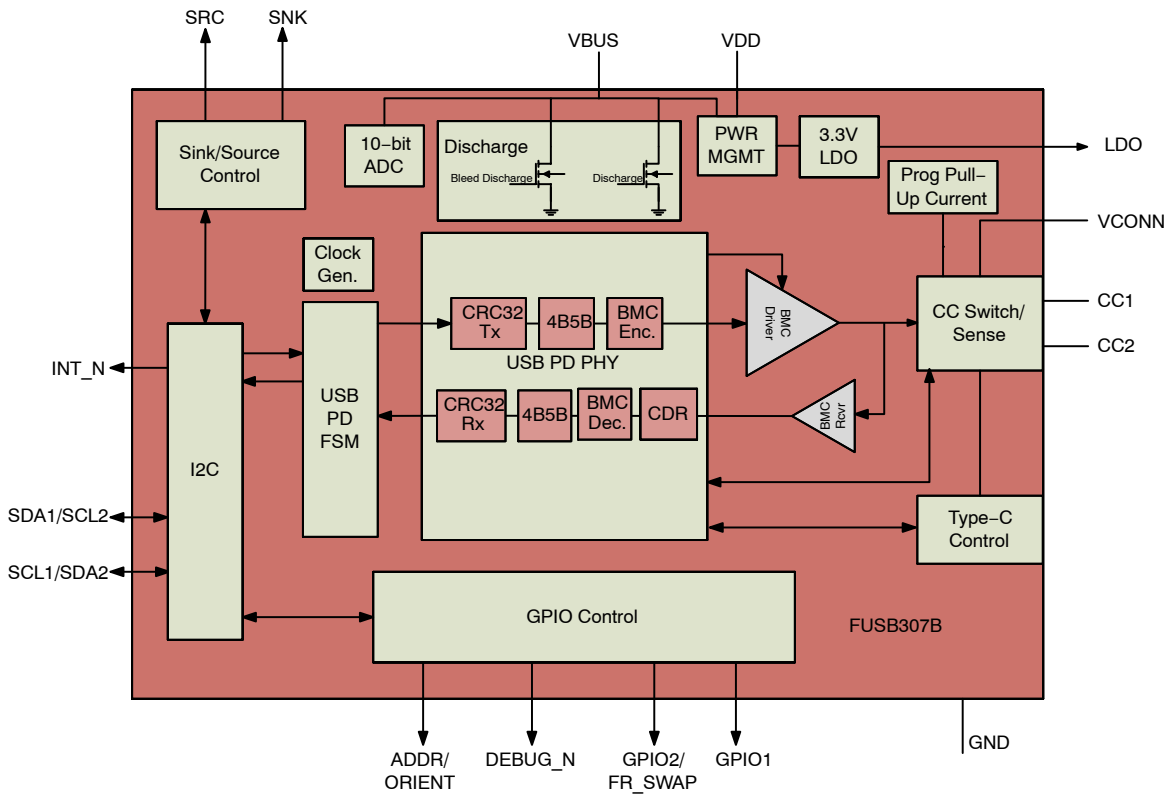


Figure 3. FUSB307B Block Diagram

Pin Configurations

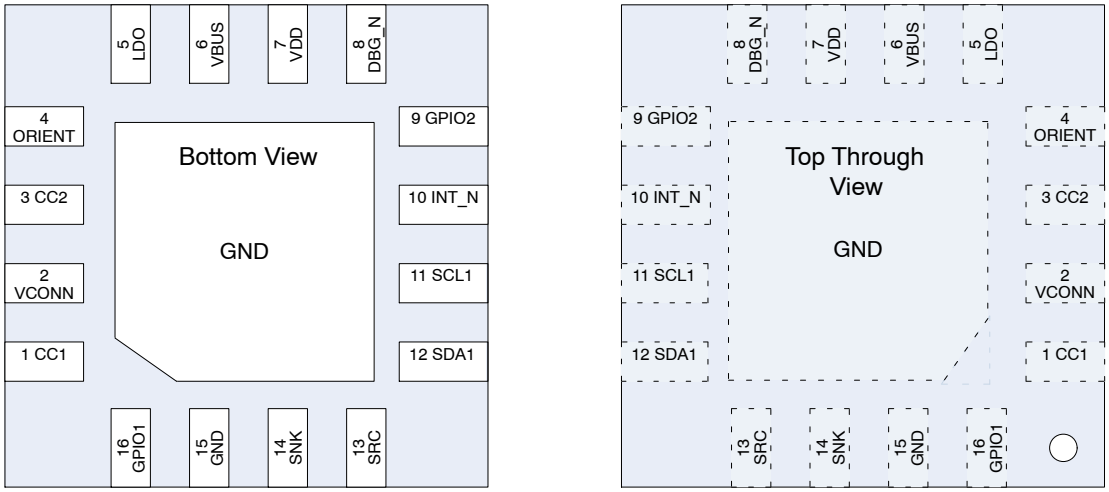


Figure 4. Pin Assignment QFN (FUSB307B)

Pin Descriptions

Table 2. PIN DESCRIPTION

Name	Type	Description
USB TYPE−C CONNECTOR INTERFACE		
CC1	I/O	Type−C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation of the insertion is. Functionality after attach depends on mode of operation detected. Operating as a host: − Sets the allowable charging current for VBUS to be sensed by the attached device − Used to communicate with devices using USB BMC Power Delivery − Used to detect when a detach has occurred Operating as a device: − Indicates what the allowable sink current is from the attached host − Used to communicate with devices using USB BMC Power Delivery
CC2	I/O	
GND	Ground	Ground
VBUS	Power	VBUS supply pin for attach and detach detection when operating as an upstream facing port (Device)
POWER INTERFACE		
VDD	Power	Input supply voltage
LDO	LDO Output	3.3 V LDO Output
VCONN	Power Switch	Regulated input to be switched to correct CC pin as VCONN to power USB3.1 fully featured cables, powered accessories or dongles bridging Type C to other video or audio connectors
SIGNAL INTERFACE		
SCL1/SDA2 (Note 1)	Open−Drain I/O	I^2C serial clock/data signal to be connected to the I^2C master
SDA1/SCL2 (Note 1)	Open−Drain I/O	I^2C serial clock/data signal to be connected to the I^2C master
INT_N	Open−Drain Output	Active LOW open drain interrupt output used to prompt the processor to read the I^2C register bits
ORIENT/I2C_ ADDR (Note 1)	3−State CMOS Output	Selects I^2C Address on Power up and then becomes a General Purpose CMOS Output
DBG_N	Open−Drain I/O	Debug Accessory Detection Open−Drain Output
GPIO2	3−State CMOS I/O	General Purpose I/O 2
GPIO1	3−State CMOS I/O	General Purpose I/O 1
VBUS SOURCE AND SINK INTERFACE		
SNK	CMOS Output	Controls external VBUS Sink Load Switch on/off (Active High)
SRC	CMOS Output	Controls external VBUS Source Load Switch on/off (Active High)

1. A different I2C address is used depending on which SDA and SCL are used and the state of ORIENT/I2C_ADDR at power up.

Power Up, Initialization and Reset

When power is first applied to VDD or VBUS, the FUSB307B goes through its POR sequence to load up all the default values in the register map, read all the fuses so that the trimmed values are available when VDD or VBUS is in its valid range. A software reset can be executed by writing SW_RES to 1 in RESET Register. This executes a full reset of the FUSB307B similar to POR where all the I2C registers go to their default state.

When powered down, the FUSB307B is configured as a UFP with CC1 and CC2 have their respective Rd pull−downs enabled such that a SOURCE can detect this as a UFP and turn on VBUS.

For the FUSB307B device, power may become available from VBUS when VDD is not present. This state is still considered “Dead Battery” until VDD is present. During Dead Battery, the FUSB307B will continue presenting Rd.

Once VDD is available, the TCPM can start the DRP toggle by setting COMMAND.LOOK4CON on the FUSB307B device.

Dead Battery Power−up

During a dead battery condition in a mobile application, the FUSB307B will be powered by VBUS and provide an LDO output to power a µController or TCPM to establish a USB−PD contract.

The FUSB307B will enable the Sink Path when attached to a source with any advertised current.

Systems with more than one Type−C port, the TCPM can enable or disable the appropriate sink paths.

Once VDD is greater than V_{DDGOOD}, the internal LDO is bypassed and the device switches from VBUS to VDD power.

Figure 5 demonstrates a dead battery power up sequence for FUSB307B.

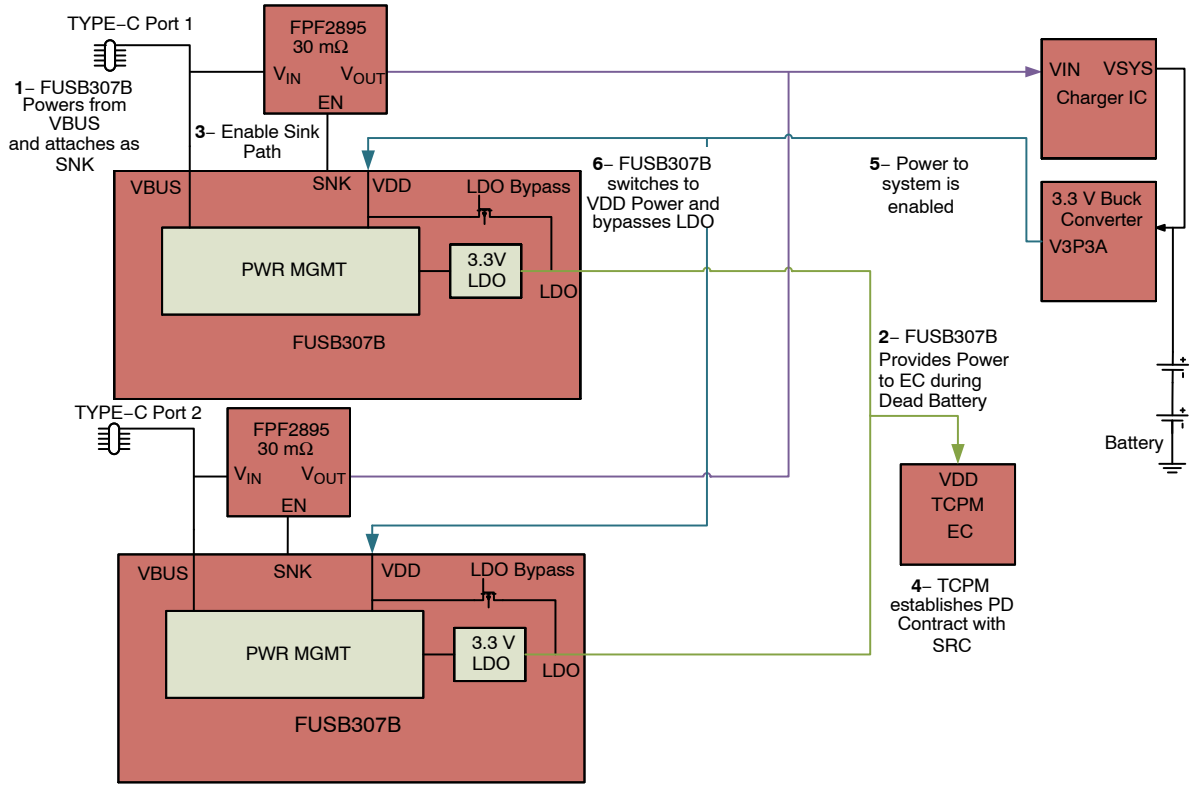


Figure 5. FUSB307B Dead Battery Operation

Programmable GPIOx

The FUSB307B has two programmable GPIOs. These can be programmed to be Inputs, CMOS Outputs or Open Drain Outputs. To configure them, the TCPM writes to GPIO1_CFG and GPIO2_CFG. If the GPIO is configured as an input, its logic value can be read in GPIO_STAT and ALERT_VD registers.

Standard Outputs

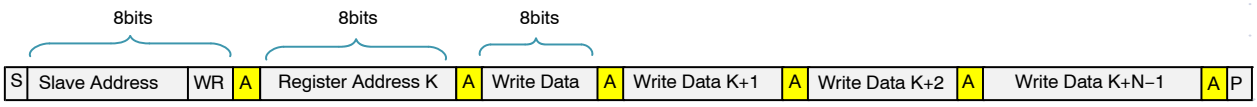
The FUSB307B implements Orientation and supports Debug Accessory detection output as indicated in STD_OUT_CAP register.

To configure the Orientation, Mux selection, and Debug Accessory, the TCPM writes to STD_OUT_CFG.

I²C Interface

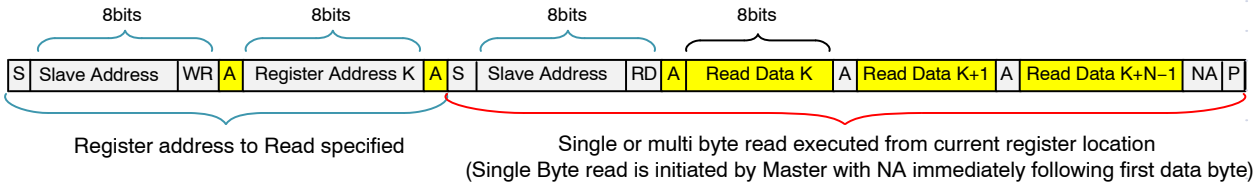
The FUSB307B includes a full I²C slave controller. The I2C slave fully complies with the I2C specification version 6 requirements. This block is designed for fast mode plus signals.

Examples of an I²C write and read sequence are shown in Figure 7 and Figure 8 respectively.



NOTE: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 6. I2C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

From Master to Slave
From Slave to Master

S Start Condition
A Acknowledge (SDA Low)
NA NOT Acknowledge (SDA High)
WR Write = 0
RD Read =1
P Stop Condition

Figure 7. I2C Read Example

I²C Address Selection

I2C Slave addresses can be changed by configuring the I2C_ADDR_GPO input on power up with a pull−up or pull−down resistor and routing the SCL and SDA lines according to Table 3.

Interrupt Operation

The INT_N pin is an active low, open drain output which indicates to the host processor that an interrupt has occurred in the FUSB307B which needs attention. The INT_N pin is asserted after power−up or device reset RESET.SW_RES set to 1b (due to ALERTL.I_PORT_PWR and PWRSTAT.TCPC_INIT).

When an interruptible event occurs, INT_N is driven low and is high−Z again when the processor clears the interrupt by writing a 1 to the corresponding interrupt bit position. Writing a 0 to an interrupt bit has no effect.

A processor firmware has additional control of INT_N through individual event mask bits which can be set or cleared to enable or disable INT_N from being driven low when each event occurs.

Table 3. I²C ADDRESSES

I2C_ADDR	SCLx/SDAx	Slave Address							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SCL1/SDA1	1	0	1	0	0	0	0	R/W
1	SCL1/SDA1	1	0	1	0	0	0	1	R/W
0	SCL2/SDA2	1	0	1	0	0	1	0	R/W
1	SCL2/SDA2	1	0	1	0	0	1	1	R/W

I²C Idle Mode

Entering I²C Idle Mode

The FUSB307B does not need to enter I²C Idle Mode in order to save power. Entering this mode has no effect on I²C function. The FUSB307B can enter idle mode if 0xFF is written to the COMMAND register. Once in Idle mode, the FUSB307B will not set the PWRSTAT.TCPC_INIT to one.

Exiting I²C Idle Mode

The FUSB307B will exit I²C Idle mode when any I²C communication is addressed to the slave. The ALERTL.I_PRT_PWR interrupt will be set and no PWRSTAT bits will be set.

The device's I²C block is always on without power penalties.

VCONN Control

The FUSB307B integrates a CCx to VCONN switch with programmable OCP capability via the VCONN_OCP register. If PWRCTRL.VCONN_PWR is set to 0, the standard VCONN current limit is used (210.5 mA). If PWRCTRL.VCONN_PWR is set to 1, the programmable VCONN_OCP is used.

The VCONN switch can be enabled via the PWRCTRL register bits EN_VCONN and TCPC_CTRL.ORIENT bits (for CC1/2 selection).

A VCONN valid voltage is monitored and reported on PWRSTAT.VCONN_VAL. The valid voltage threshold is fixed at 2.4 V.

Debug Accessory Support

The FUSB307B implements autonomous detection of Source and Sink debug accessories. A debug accessory detection is indicated via a standard output. The FUSB307B powers on looking for a debug accessories without processor intervention.

If debug accessory detection is not wanted, the processor can write TCPC_CTRL.DEBUG_ACC_CTRL = 1b.

Type−C Manual Mode Detection

The CC pull up (Rp) or pull down (Rd) resistors and DRP toggle are setup via the ROLECTRL register.If a TCPM wishes to control Rp/Rd directly, it can write ROLECTRL.DRP = 0b and the desired ROLECTRL bits [3:0] (CC1/CC2).

The FUSB307B can autonomously toggle the Rp/Rd by setting ROLECTRL.DRP = 1b and the starting value of Rp/Rd in ROLECTRL.bits [3:0]. DRP toggling starts by writing to the COMMAND register

If ROLECTRL.DRP = 1b, the only allowed values for CC1/CC2 in ROLECTRL bits [3:0] are Rp/Rp or Rd/Rd.

When ROLECTRL bits 3:0 are set to Open and ROLECTRL.DRP = 0b, the PHY and CC comparators are powered down.

The FUSB307B updates the CCSTAT register on a Connect, Disconnect, a change in ROLECTRL.DRP or a change (tTCPCFilter debounced) on the CC1 or CC2 wire.

The TCPM reads CCSTAT upon detecting an interrupt and seeing the ALERTL.I_CCSTAT = 1. The FUSB307B indicates the DRP status, the DRP result, and the current CC status in this register.

The FUSB307B will set CCSTAT.LOOK4CON = 0b when it has stopped toggling as a DRP.

The TCPM reads the CCSTAT.LOOK4CON to determine if the FUSB307B is toggling Rp/Rd when operating as a DRP, it then reads CCSTAT.CON_RES to determine if the FUSB307B is presenting an Rp or Rd and read the CCSTAT.CC1_STAT and CCSTAT.CC2_STAT to determine the CC1 and CC2 states.

The FUSB307B debounces the CC lines for tTCPCfilter before reporting the status on CCSTAT. The TCPM must complete the debounce as defined in Type−C Specification.

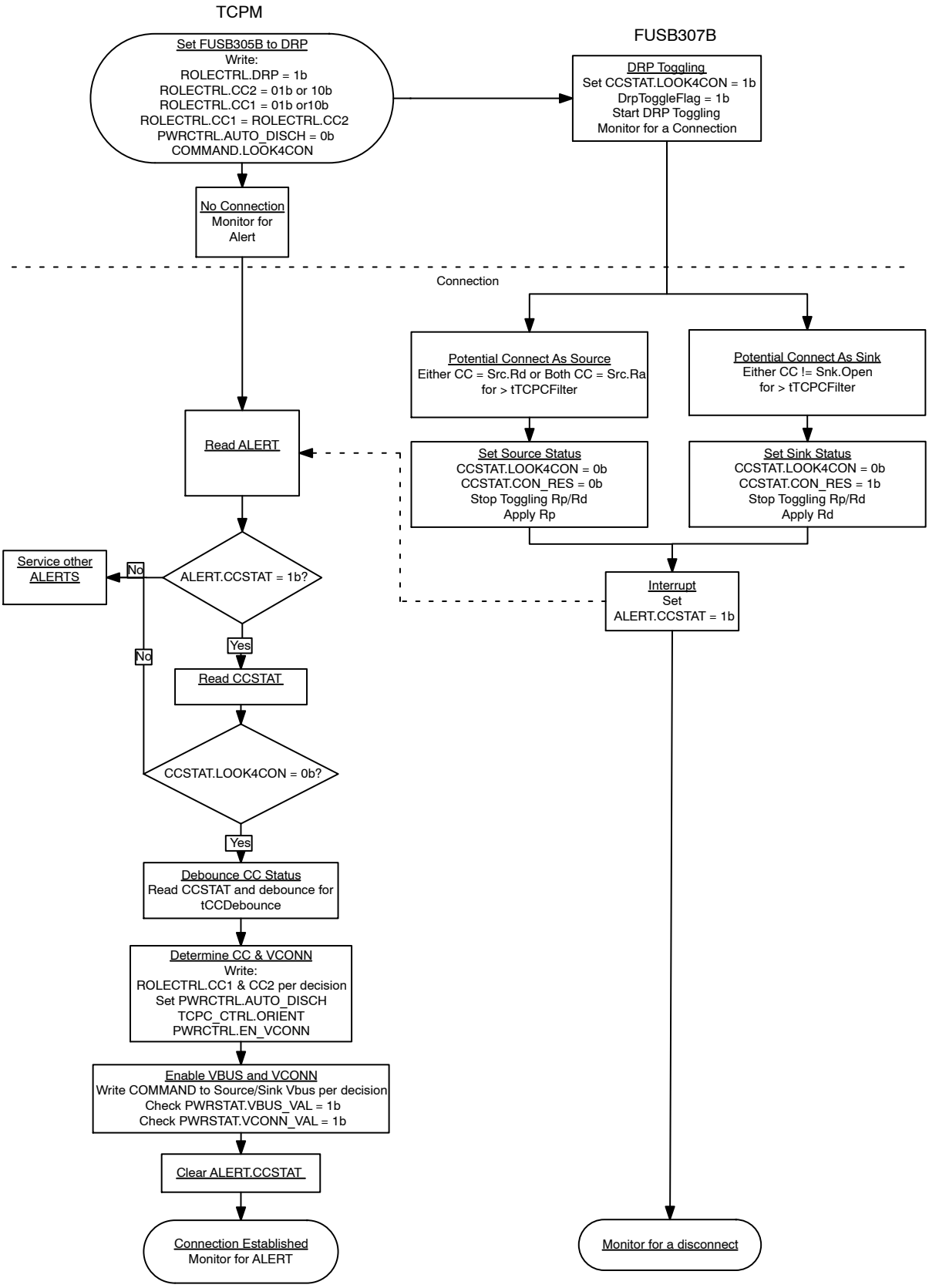


Figure 8. DRP Initialization and Connection Detection

BMC Power Delivery

The Type−C connector allows USB Power Delivery (PD) to be communicated over the connected CC pin between two ports. The communication method is the BMC Power Delivery protocol and is used for many different reasons with the Type−C connector. Possible uses are outlined below.

- Negotiating and controlling charging power levels
- Alternative Interfaces such as MHL, Display Port
- Vendor specific interfaces for use with custom docks or accessories
- Role swap for dual−role ports that want to switch who is the host or device
- Communication with USB3.1 full featured cables

The FUSB307B integrates a thin BMC PD client which includes the BMC physical layer and packet buffers which allows packets to be sent and received by the host software through I^2C accesses.

Receive State Machine

The TCPM can setup the desired types of messages to be received by the FUSB307B via the RXDETECT register. This register defaults to 0x00 (Receiver disabled) upon power up, reset, Hard Reset transmission and reception, and upon detecting a cable disconnect. A message is not received unless it is first enabled. Figure 9 shows the FUSB307B receive state machine.

Upon a successfully transmitting GoodCRC, the RXSTAT register is updated with the type of message received and the TCPM is alerted via ALERTL.I_RXSTAT bit (see transition from PRL_Rx_Send_GoodCRC to PRL_Rx_Report_SOP* in Figure 9). The total number of bytes in the receive buffer RXDATA is stored in RXBYTECNT This number includes the header bytes that are stored in RXHEADL and RXHEADH and the RXSTAT register.

The RXBYTECNT, RXSTAT registers and the internal receive buffer will be cleared after the ALERTL.I_RXSTAT bit is cleared.

The FUSB307B will automatically transmit a GoodCRC message for valid enabled messages within tTransmit.

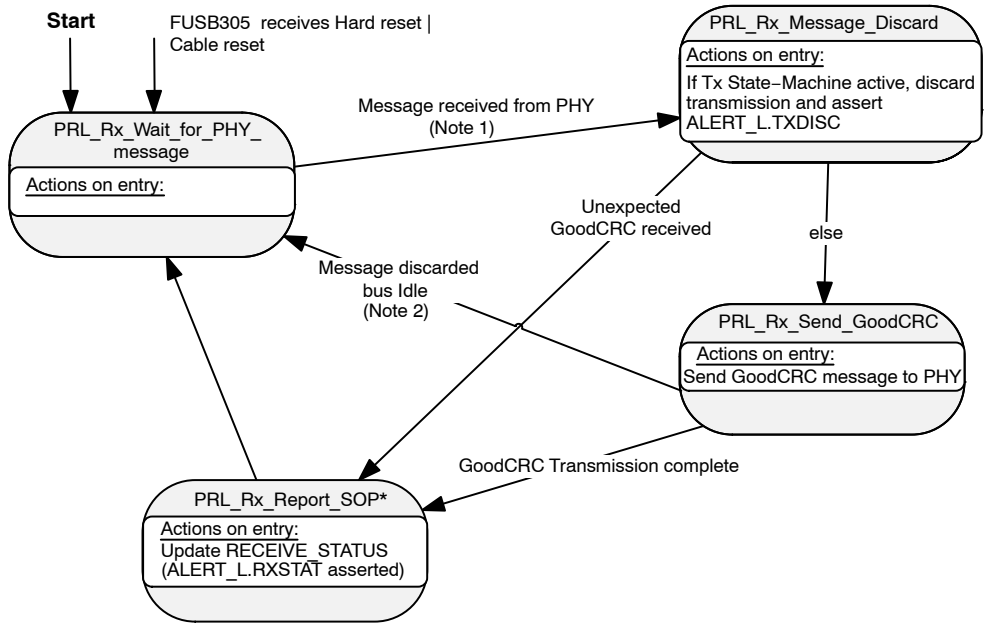
A received message is valid when:

- It is not a GoodCRC message
- The calculated CRC is correct
- The SOP* type is enabled

The makeup of the GoodCRC message is formed by the received SOP* type and the contents of MSGHEADR register.

When an expected GoodCRC message or a Hard Reset signaling is received, they will not be replied with a GoodCRC message (see Note 2 in Figure 9). If a GoodCRC message received was not expected due to the SOP* type or mismatched Message ID, the receive state machine will not send a GoodCRC message and will transition to PRL_Rx_Report SOP* to inform the TCPM.

If a Hard Reset message is received, the FUSB307B will reset the RXDETECT preventing the reception of future messages until the TCPM re−enables it.



1. This indication is sent by the PHY when a message has been discarded due to CC being busy, and after CC becomes idle again (see USB PD Spec).
2. Messages do not include Hard Reset or Cable Reset signals or expected GoodCRC messages (GoodCRC messages are only expected after the FUSB305 PHY has received the tx message and the FUSB305 Tx state−machine is in the PRL_Tx_Wait_for_PHY_response state).

Figure 9. Receive State Machine

Transmit State Machine

To transmit a message, the TCPM must first write the entire message in the following registers: TXHEADL, TXHEADH, TXBYTECNT and the TXDATA.

The actual transmission starts when the TCPM writes the TRANSMIT register.

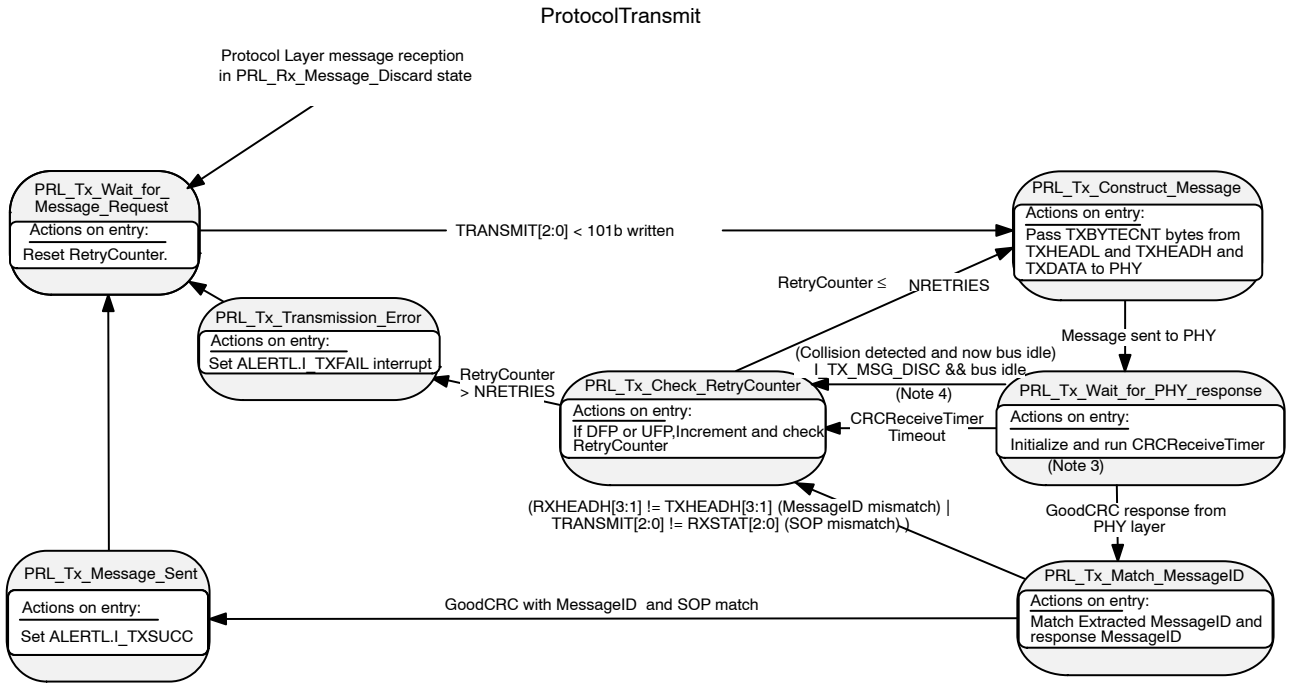
The TRANSMIT register is where the message selection is done and it must be written once per transmission.

The TRANSMIT and TXBYTECNT will be reset after executing a successful or failed transmission.

If the TRANSMIT.RETRY_CNT is set to a number greater than 0, the FUSB307B will automatically retry sending the same message if a GoodCRC is not received within tCRCReceiveTimer. An automatic retry is not performed when sending Hard−Resets, Cable−Resets, or BIST Carrier Mode 2 signaling.

The TCPM must not write the TRANSMIT register again until ALERTL.I_TXSUCC, I_TXFAIL, I_TX_DISC have been asserted and cleared.

The TCPM will not write the TRANSMIT register to request a transmission other than a Hard reset until it has cleared all received message alerts. If a TRANSMIT is written when ALERTL.I_RXSTAT = 1 or ALERTL. I_RXHRDRST = 1, the transmit request is discarded and ALERTL.I_TX_DISC is asserted.



3. The CRCReceiveTimer is only started after the FUSB305 has sent the message. If the message is not sent due to a busy channel then the CRCReceiveTimer will not be started.
4. This Indication is sent by the PHY layer when a message has been discarded due to CC being busy, and after CC becomes idle again. The CRCReceiveTimer is not running in this case since no message has been sent.

Figure 10. Receive State Machine

Hard Reset/ Cable Reset State Machine

The TCPM will write the TRANSMIT register to initiate the Hard Reset/Cable Reset state machine, see Figure 11. If a the FUSB307B is in the middle of a transmission when instructed to send a Hard or Cable reset, it will set the ALERTL.I_TXDISC bit and send the hard reset signaling as soon as possible. The FUSB307B implements the HardResetCompleteTimer. A Hard Reset or Cable Reset will be attempted until the HardResetCompleteTimer times out. After a successful transmission or timeout, the FUSB307B will indicate that a Hard Reset or Cable Reset has been sent by asserting both ALERTL.I_TXSUCC and ALERTL.I_TXFAIL registers simultaneously. The bits in RXDETECT and RXBYTECNT will be reset to disable PD message passing after a Hard Reset is received or transmitted.

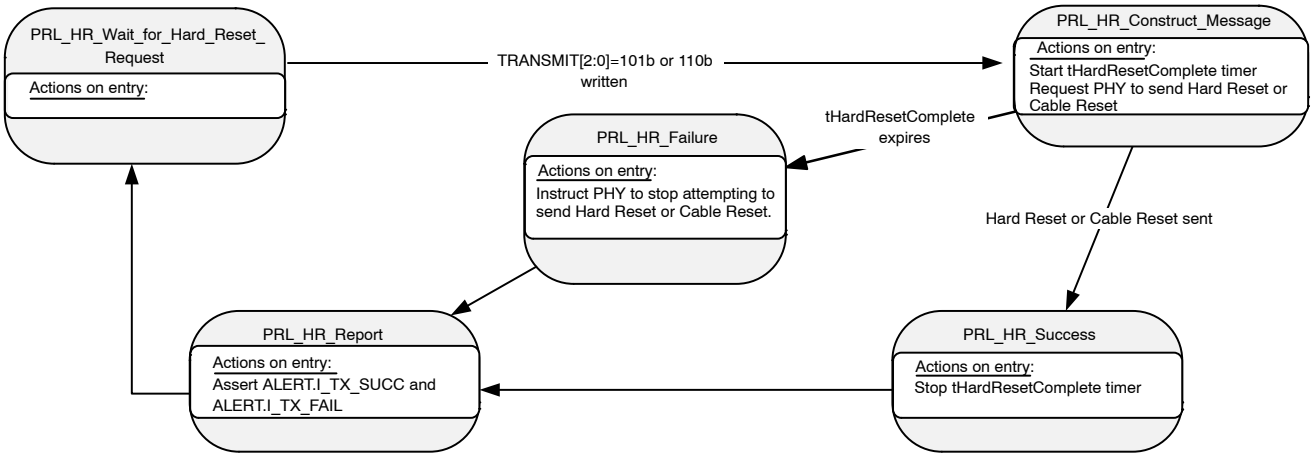


Figure 11. Hard Reset and Cable Reset State Machine

Automatic GoodCRC Response

Power Delivery packets require a GoodCRC acknowledge packet to be sent for each received packet where the calculated CRC is the correct value. This calculation is done by the FUSB307B.

The FUSB307B will automatically send the GoodCRC control packet in response to alleviate the local processor from responding quickly to the received packet. Once the GoodCRC packet is sent the FUSB307B will trigger the ALERTL.I_RXSTAT interrupt.

The following sequence of events occur internally within the FUSB307B without processor intervention when it is determined that the receive message has the correct CRC. If the host processor attempts a packet transmission during an Automatic GoodCRC response, the FUSB307B will set the ALERTL.I_TXDISC bit interrupting the processor. The processor should only transmit a new packet once ALERTL.I_TXSUCC or ALERTL.I_TX_FAIL has been received.

It is assumed that the processor will set the PWRCTRL.ORIENT to specify which channel USB−PD traffic will be transmitted or received.

BIST Mode

Bist Transmit

The FUSB307B will transmit Bist Carrier Mode 2 signaling when directed by the TCPM via TRANSMIT register. The FUSB307B will exit Bist Mode after tBISTContMode timer expires.

Bist Receive

When the FUSB307B is in Bist receive mode via TCPC_CTRL register, it will acknowledge these packets with a GoodCRC and automatically flush the buffer to allow for thousands of packets to be received without filling the receive buffer. Bist Receive mode will exit on a cable disconnect or a Hard Reset received.

VBUS Source and Sink Control

The FUSB307B can control a source and sink path via two outputs: SRC for the source path and SNK for the sink VBUS path.

These two outputs are controlled via the COMMAND register.

The SNK and SRC outputs will autonomously disable upon a cable detach.

Voltage Transitions

The FUSB307B device can control a vSafe5V path via its SRC output.

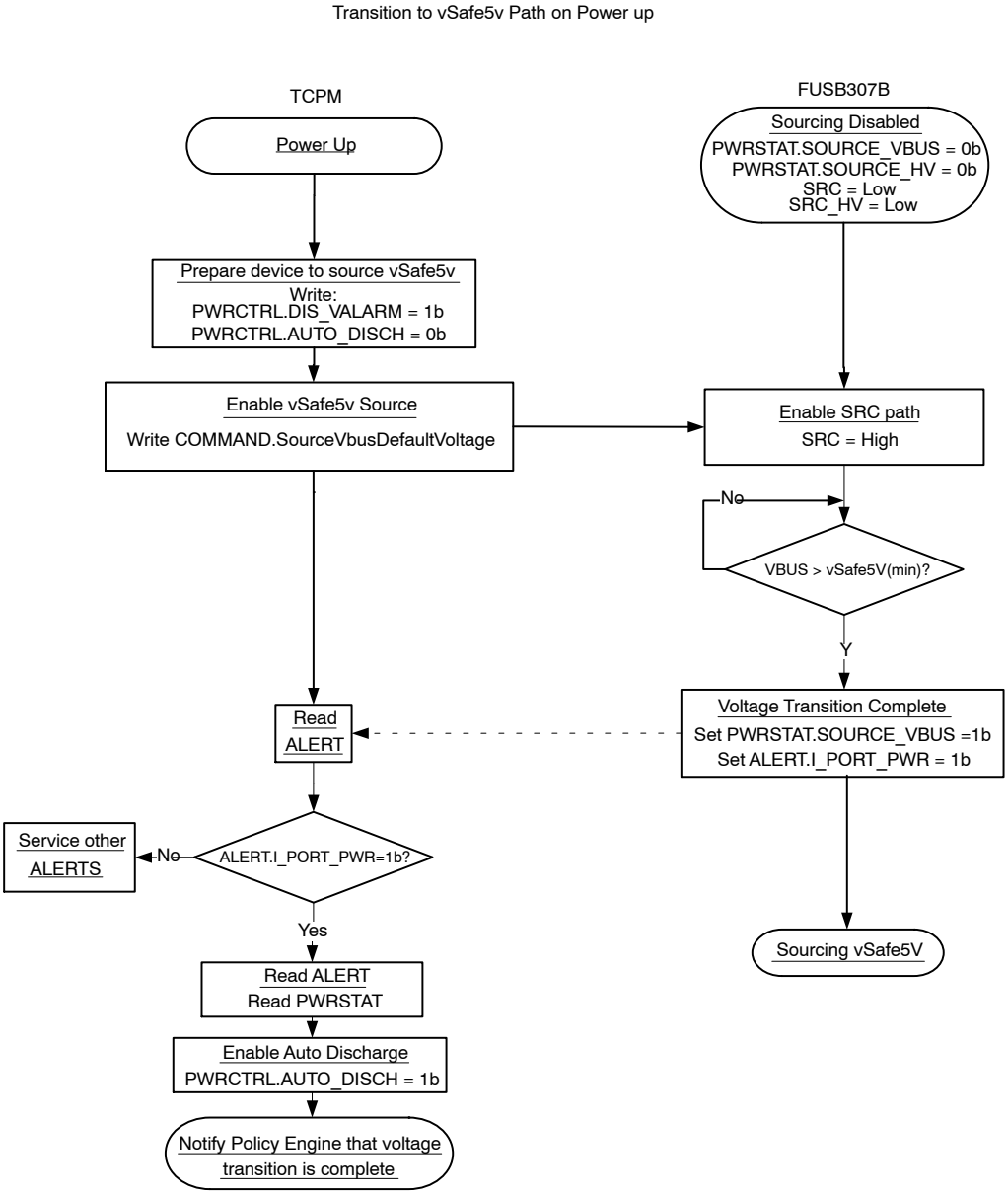
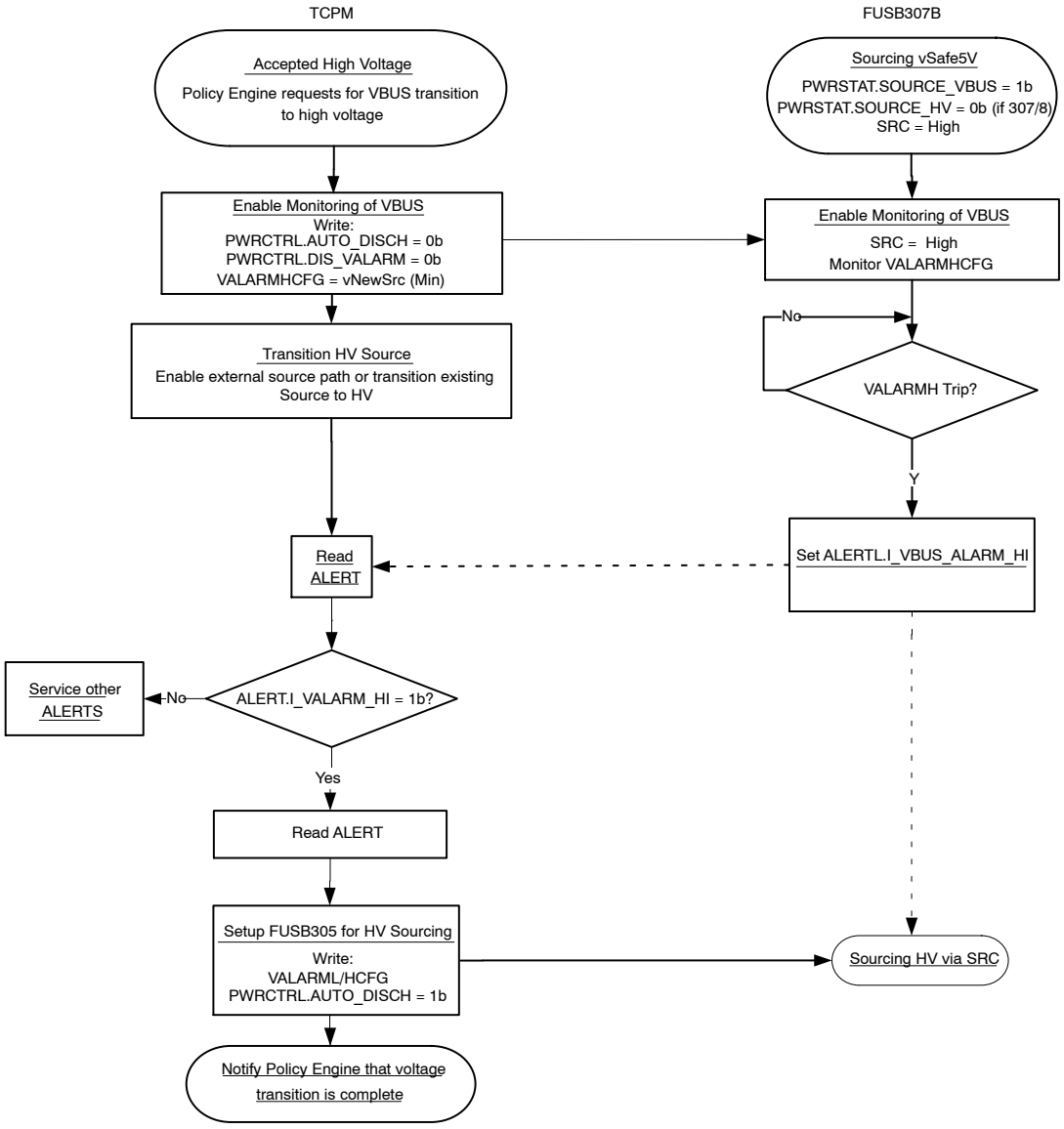


Figure 12. Transition to vSafe5V on Power Up

Transition to HV using SRC enabled Path



NOTE: Transitioning from HV on SRC to vSafe5v also on SRC can be done by using Voltage Alarm Low. Power supply is responsible for transitioning voltages to meet USB PD spec− no discharge necessary.

Figure 13. Transition to vSafe5V on Power Up

VBUS Monitoring and Measurement

The FUSB307B can monitor the presence of VBUS and will report it on PWRSTAT.VBUS_VAL and interrupt ALERT.I_PORT_PWR.

VBUS_VAL is set according to VBUS thresholds in *vVBUSthr*.

The FUSB307B also supports a more precise voltage measurement via an on−board ADC. The voltage on VBUS is measured at a rate of tVBUSsample and it is reported on VBUS_VOLTAGE_L/H register. The precision of the measurement is +/2% with a resolution of 25 mV LSB.

In addition to providing the µProcessor an accurate measurement of VBUS, the measurement in VBUS_VOLTAGE will be used when monitoring various user defined thresholds:

- Voltage alarms in registers VALARMLCFG and VALARMHCFGL
- VBUS Disconnect Threshold in registers VBUS_SNK_DISCL and VBUS_SNK_DISCH
- VBUS Stop Discharge Threshold in registers VBUS_STOP_DISCL and VBUS_STOP_DISCH
- The FUSB307B implements Low and High VBUS Voltage Alarms that can be programmable via VALARMLCFG and VALARMHCFG respectively. If the High or the Low thresholds are crossed, the FUSB307B will signal an interrupt on ALERTL.I_VBUS_ALRM_HI or ALERTH.I_VBUS_ALRM_LO respectively. These alarms can be disabled by writing PWRCTRL.DIS_VALARM to one

ALERTL.I_PORT_PWR is asserted if the bit−wise AND of PWRSTAT and PWRSTAMSK results in any bits that have the value 1.

VBUS Discharge

Manual Discharge

There are two types of manual discharge circuits implemented: A bleed discharge for low current and a force discharge. The bleed discharge can be manually enabled by writing a one to register bit PWRCTRL.EN_BLEED_DISCH. When enabled, the bleed discharge provides a low current load on VBUS of 7 kΩ (max.) via RBLEED. The force discharge is used to quickly discharge VBUS to vSafe0V by applying a dynamic load to VBUS via RFULL_DISCH. The force discharge can be manually enabled by writing a one to register bit PWRCTRL.FORCE_DISCH. When RFULL_DISCH is applied, the maximum slew rate allowed for discharging VBUS does not exceed vSrcSlewNeg 30 mV/µs as it is specified in the USB−PD spec.

Automatic discharge bit PWRCTRL. AUTO_DISCH must be disabled before enabling force discharge.

Automatic Source Discharge after a Disconnect

Automatic discharge can be enabled by setting PWRCTRL. AUTO_DISCH register bit. When in Source mode the FUSB307B will fully discharge VBUS to vSafe5V (max.) within tSafe5V and to vSafe0V within tSafe0V when a Disconnect occurs. The FUSB307B is in Source mode when the SRC output is asserted.

The FUSB307B in Source mode will detect a Disconnect if the CCSTAT.CCx_STAT field for the monitored CC pin indicates SRC.Open and enable the FULL Discharge pull−down device. The monitored CC pin is specified by TCPC_CTRL.ORIENT.

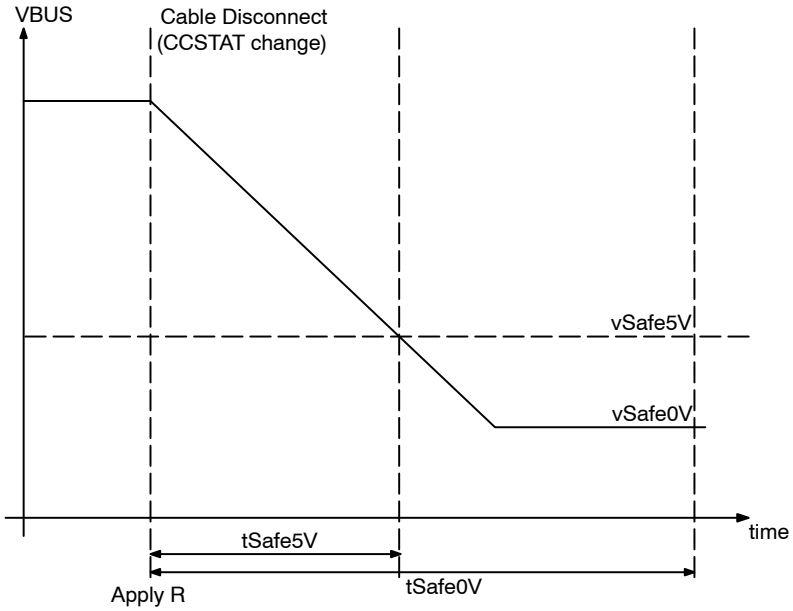


Figure 14. VBUS Auto Discharge as Source

Automatic Sink Discharge after a Disconnect

Automatic discharge can be enabled by setting PWRCTRL. AUTO_DISCH register bit. When in Sink mode the FUSB307B will fully discharge VBUS to vSafe5V (max.) within tSafe5V and to vSafe0V within tSafe0V when a disconnect occurs. The FUSB307B is in Sink mode any time MSGHEADR.POWER_ROLE = 0.

Whenever the system is sinking voltages greater than vSafe5V, a disconnect will be detected based on VBUS_SNK_DISC registers.

If the system is only sinking vSafe5V, a disconnect will be detected when VBUS_VAL goes low.

Due to the high capacitance on VBUS (up to 100 μF) the FUSB307B may not immediately know if VBUS has been removed. The FUSB307B with Automatic Discharge on will apply RBLEED discharge load to VBUS until it crosses below VBUS_SNK_DISC.

The FUSB307B has to detect a disconnect within tDisconnectDetect (6 ms) from VBUS crossing VBUS_SNK_DISCL. Once the FUSB307B has detected a Disconnect, RFULL_DISCH will be enabled bringing the VBUS voltage down to vSafe0V.

Whenever the FUSB307B detects a Disconnect, it will not present Rd (or Rp) until VBUS reaches vSafe0V.

When the VBUS voltage goes below vSafe0V, the auto−discharge circuit will disable.

If the discharge of VBUS to below vSafe0V is not accomplished by tSafe0V (650 ms), the FUSB307B will set the interrupt

NOTE: ALERTL.I_PORT_PWR is asserted if the bit−wise AND of PWRSTAT and PWRSTAMSK results in any bits that have the value 1.

ALERTH. I_FAULT bit and the status FAULTSTAT.DISCH_FAIL. The discharge circuit is not turned off when this happens.

In tSinkDischargeBleed + tSinkDischargeFull have to be less than tSafe5V to comply with USB−PD spec.

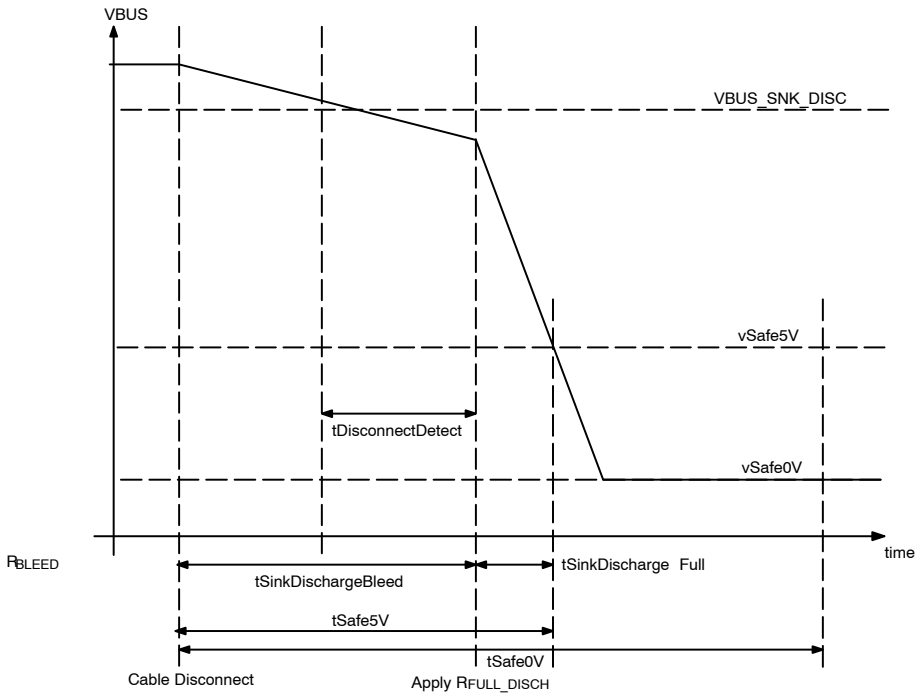


Figure 15. VBUS Auto Discharge as SinkSource

Discharge during a Connection

The discharge functions can be manually activated via the PWRCTRL.FORCE_DISCH register. The discharge pull−down is specified by *RFULL_DISCH*. The FUSB307B will automatically disable discharge when VBUS reaches VBUS_STOP_DISC threshold

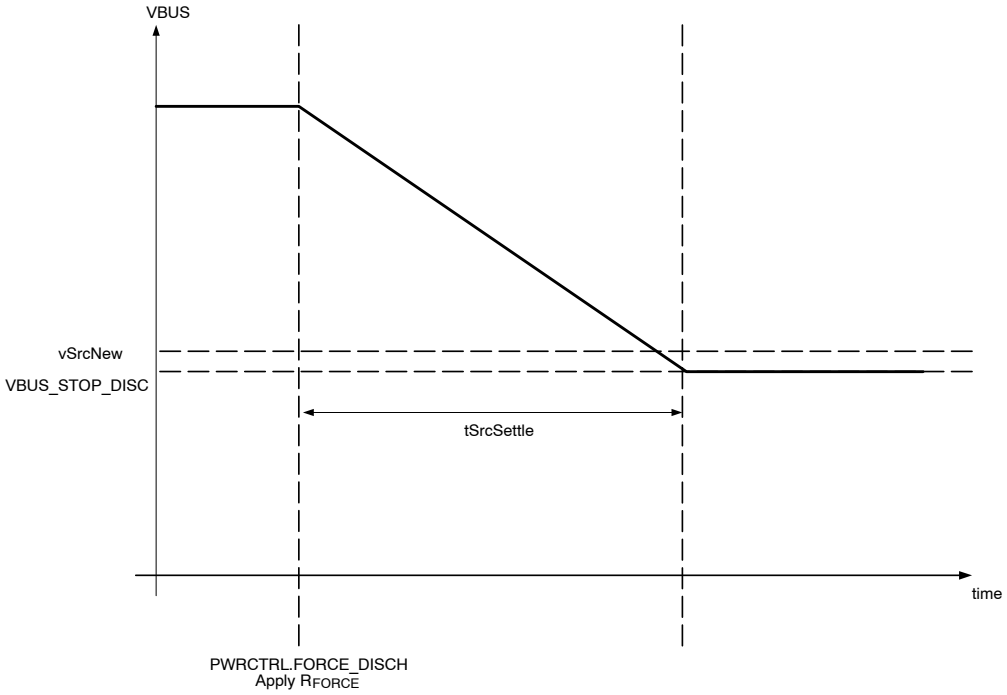


Figure 16. Sink Discharge during a Connection

Sink Discharge during a Connection

When the device is operating as a sink and it receives a Hard Reset or a Power Role Swap, the automatic discharge circuitry and SNK output will be disabled by the host processor to avoid a disconnect detection.

Watchdog Timer

The watchdog timer functionality is enabled whenever TCPC_CTRL.EN_WATCHDOG is set to 1b. The watchdog timer should only be enabled after an attach when the device is in Attached.Src, Attached.Snk or Apply.ROLECONTROL states. The watchdog timer starts when any of the interrupts that are not masked in the Alert register are set or when the INTB pin is asserted. The watchdog timer is cleared on an I2C access by the TCPM (either read or write). If the INTB pin is still asserted after this I2C access, the watchdog timer will reinitialize and start monitoring again until all of the Alerts are cleared or until the INTB pin is de−asserted.

When the watchdog timer expires, the FUSB307B will immediately disconnect the CC terminations by setting ROLE_CONTROL bits 3..0 to 1111b, disable all SRC/SRC_HV or SNK outputs, discharge VBUS to vSafe0V, and set FAULT_STATUS.I2CInterfaceError.

USB−PD Rev 3.0 Features

Extended Data Messages

Extended Data Messages is only supported via Chunking where large messages are broken into 2 or more 26 byte chunks.

SinkTx

The USB−PD Rev 3.0 has added this feature to allow the Sink to safely transmit a message reducing the risk of collisions.

The Protocol layer in the Source will request to set the Rp value to SinkTxOk to indicate that the Sink can initiate an Atomic Message Sequence (AMS). The Protocol layer in the Source will request to set the Rp value to SinkTxNG to indicate that the Sink cannot initiate an AMS since the Source is about to initiate an AMS.

The Sink TCPM that desires to transmit will write the TX Buffers and SINK_TRANSMIT register. The FUSB307B will wait for the Rp value to be set to SinkTxOk before transmitting the message. If Rp is already set to SinkTxOk, a SINK_TRANSMIT will transmit immediately.

In the case where the Sink TCPM wants to abort the message transmission before the Rp value has changed to SinkTxOk, it can write SINK_TRANSMIT.EN_SNK_TX = 0b. If a transmission has already started, writing this register will be ignored and a FAULTSTAT.I2C_ERR interrupt will be generated.

If TXBYTECNT is less than 2h when a SINK_TRANSMIT.TXSOP <101 is requested, a FAULTSTAT.I2CERR interrupt is generated.

The ALERTL.I_RXSTAT must be cleared when SINK_TRANSMIT is written or an ALERTL.I_TX_DISC is asserted.

Table 4. R_P SETTINGS FOR SINK T_X

Source Rp	Parameter	Description	Sink Operation	Source Operation
1.5 A @5 V	SinkTxNG	Sink Transmit “No Go”	Sink cannot initiate an AMS. Sink can only respond to Messages as part of an AMS	Source can initiate an AMS tSinkTx after setting Rp to this value (Note 5)
3.0 A @5 V	SinkTxOk	Sink Transmit “OK”	Sink can initiate an AMS	Source cannot initiate an AMS while this value is set

5. The TCPM is responsible for tSinkTx timer.

Fast Role Swap

Fast Role Swap is the process of exchanging the Source and Sink roles between Port Partners rapidly due to the disconnection of an external power supply.

The Fast Role Swap process is intended for use by a PDUSB HUB that presently has an external wall supply, and is providing power both through its downstream Ports to USB Devices and upstream to a USB Host such as a notebook. On removal of the external wall supply Fast Role Swap enables a VBUS supply to be maintained by allowing the USB Host to apply vSafe5V after having detected Fast Role Swap signaling.

The initial Source will signal a Fast Role Swap request by driving CC to ground with a resistance of less than *rFRSwapTx* for *tFRSwapTx*. The initial Source shall only signal a Fast Role Swap when it has an Explicit Contract. On transmission of the Fast Role Swap signal any pending Messages will be Discarded by internally toggling PD_RESET. The Fast Role Swap signal may override any active transmissions. Since the initial Sink’s response to the Fast Role Swap signal is to send a FR_Swap Message, the initial Source shall ensure Rp is set to *SinkTxOk* once the Fast Role Swap signal is complete.

The flow diagram in Figure 17 demonstrates the HUB and Host function during the initial Fast Role Swap process. The AMS and Power Role swap necessary to complete the Fast Role Swap is performed by the respective TCPMs.

Fast Role Swap Cable Disconnect (Informational Only)

The Initial Sink device waiting for FRSwap will not disconnect on VBUS since PWRCTRL.AUTO_DISCH will be set to zero by the TCPM. If the Type−C cable detaches while the Initial Sink is ready for a FRSwap, it will look like the Initial Source has initiated a FRSwap; The CC lines will be driven to GND by Rd.

The initial Sink will perform the FRSwap and the TCPM will initiate the FR_Swap message. Since there is no device attached, there will be no GoodCRC response which will transition to Type−C Error Recovery.

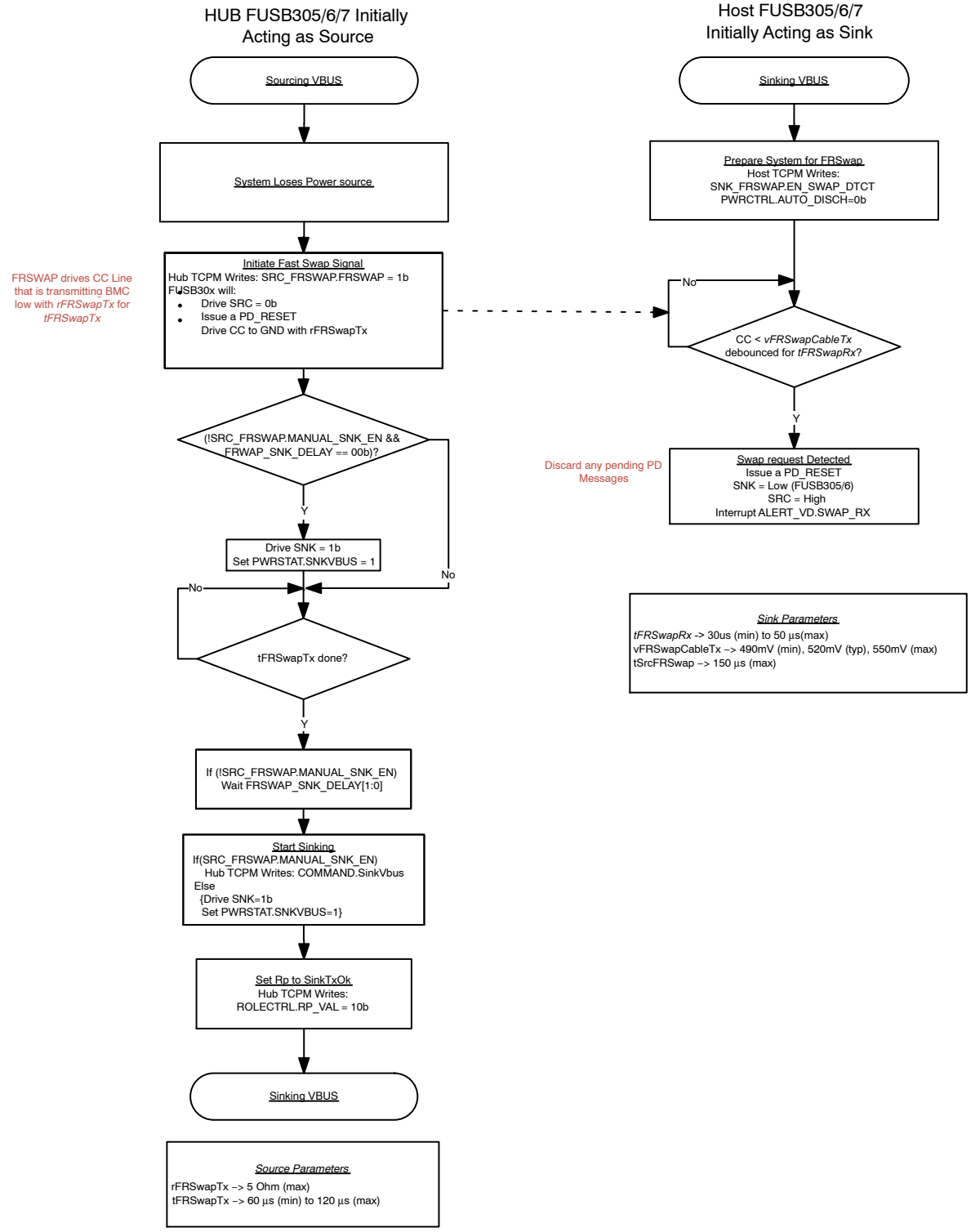


Figure 17. Fast Role Swap Flow Diagram

Table 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{DDAMR}	Supply Voltage from VDD		−0.5	6.0	V
V_{CC_HDDRP} (Note 6)	CC pins when configured as Host, Device or Dual Role Port		−0.5	6.0	V
V_{VBUS}	VBUS Supply Voltage		−0.5	28.0	V
$T_{STORAGE}$	Storage Temperature Range		−65	+150	C
T_J	Maximum Junction Temperature			+150	C
T_L	Lead Temperature (Soldering, 10 seconds)			+260	C
ESD	Human Body Model, JEDEC JESD22−A114	Connector Pins (VBUS, CCx)	4		kV
		Others	2		kV
	Charged Device Model, JEDEC LESD22−C101	All Pins	1		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. As host, device drives CC, VConn.

Table 6. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{BUS}	VBUS Supply Voltage (Note 7)	4.0	5.0	21.5	V
V_{DD}	VDD Supply Voltage	2.8 (Note 8)	3.3	5.5	V
V_{CONN}	VCONN Supply Voltage (Note 9)	2.7		5.5	V
I_{CONN}	VCONN Supply Current			560	mA
T_A	Operating Temperature	−40		+85	C
T_A	Operating Temperature (Note 10)	−40		+105	C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. 20 V PD + 5% Tolerance per spec + 0.5 V Load Transition.
8. This is for functional operation only and isn't the lowest limit for all subsequent electrical specifications below. All electrical parameters have a minimum of 3 V operation.
9. For powered accessories Vconn minimum is 2.7 V.
10. Automotive part only, FUSB307BVMPX.

DC and Transient Characteristics

Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.

Table 7. CURRENT CONSUMPTION

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
$I_{DISABLE}$	Disable Current (ROLECTRL = 0x0F)			10	μA
I_{STBY}	Unattached Sink		6	10	μA
	Unattached DRP or Source		7	20	μA
I_{ATTACH_TypeC}	Attached as Sink (No PD, AUTO_DISCH = 0)		11	26	μA
	Attached as Source (No PD)		12	22	μA

Table 8. BASEBAND PD

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
UI	Unit Interval	3.03	3.33	3.70	μs
TRANSMITTER					
zDriver	TX output impedance at 750 kHz with an external 220 pF or equivalent load	33		75	Ω
tEndDriveBMC	Time to cease driving the line after the end of the last bit of the Frame			2	UI
tHoldLowBMC	Time to cease driving the line after the final high−to−low transition	1			μs
tStartDrive	Time before the start of the first bit of the preamble when the transmitter shall start driving the line	−1		1	μs
tBISTContMode	Time a BIST Carrier Mode 2 transmission is performed	30		60	ms
tBUFFER2CC	Time from I2C Stop from writing to TRANSMIT register to first bit of Preamble transmitted			195	μs
t_R	Rise Time	300			ns
t_F	Fall Time	300			ns
RECEIVER					
cReceiver	Receiver capacitance when driver isn't turned on (Note 11)		25		pF
zBmcRx	Receiver Input Impedance	1			MΩ
tCC2BUFFER	Time between last bit of EOP to I_RXSTAT			50	μs
tRxFilter	Rx bandwidth limiting filter (Note 11)	100			ns
nTransitionCount	Transitions count in a time window of 20 μs max	3			Edges
tTransitionWindow	Time window for detecting non−idle	12		20	μs

11. Guaranteed by characterization and/or design. Not production tested.

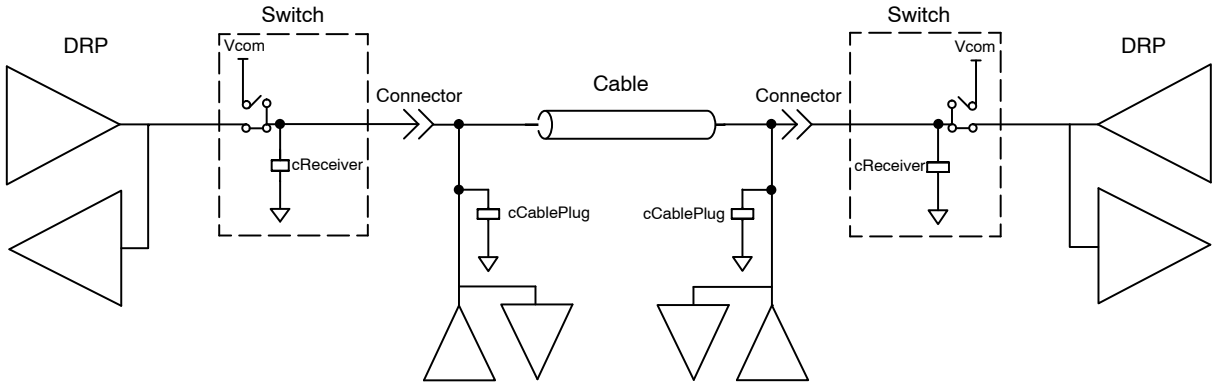


Figure 18. Transmitter Test Load

Table 9. USB-PD R3.0 SPECIFIC PARAMETERS

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C Min	Typ	Max	Unit
TRANSMITTER					
rFRSwapTx	Fast Role Swap request transmit driver resistance Measured from V_{CCx} = 0 to vFRSwapCableTx			5	Ω
tFRSwapTx	Fast Role Swap request transmit duration	60		120	μs
RECEIVER					
tFRSwapRx	Fast Role Swap request detection time	30		50	μs
vFRSwapCableTx	Fast Role Swap request voltage detection threshold	490	520	550	mV

Table 10. TYPE C SPECIFIC PARAMETERS

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C Min	Typ	Max	Unit
R_{SW_CCx}	R_{DSON} for VCONN to CC1 or VCONN to CC2		0.4	1.0	Ω
I_{SW_CCX}	Over Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range VCONN_OCP = 0Fh	600	800	1000	mA
$t_{SoftStart}$	Time taken for the VCONN switch to turn on during which Over−Current Protection is disabled		1.5		ms
I_{80_CCX}	DFP 80 μA CC Current (Default) ROLECTRL = 05h	64	80	96	μA
I_{180_CCX}	DFP 180 μA CC Current (1.5 A) ROLECTRL = 15h	166	180	194	μA
I_{330_CCX}	DFP 330 μA CC Current (3 A) ROLECTRL = 25h	304	330	356	μA
V_{UFPDB}	UFP pull−down voltage in dead battery under all pull−up DFP loads			2.18	V
R_{DEVICE}	Device pull−down resistance (Note 12)	4.6	5.1	5.6	kΩ
Ra	Powered Accessory Termination	800		1200	Ω
vRa−SRCdef	Ra Detection Threshold for CC Pin for Source for Default Current on VBUS	0.15	0.20	0.25	V
vRa−SRC1.5A	Ra Detection Threshold for CC Pin for Source for 1.5 A Current on VBUS	0.35	0.40	0.45	V

Table 10. TYPE C SPECIFIC PARAMETERS (continued)

Symbol	Parameter		T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C Min	Typ	Max	Unit
vRa−SRC3A	Ra Detection Threshold for CC Pin for Source for 3 A Current on VBUS		0.75	0.80	0.85	V
vRd−SRCdef	Rd Detection Threshold for Source for Default Current (HOST_CUR1/0 = 01)		1.50	1.60	1.65	V
vRd−SRC1.5A	Rd Detection Threshold for Source for 1.5 A Current (HOST_CUR1/0 = 10)		1.50	1.60	1.65	V
vRd−SRC3A	Rd Detection Threshold for Source for 3 A Current (HOST_CUR1/0 = 11)		2.45	2.60	2.75	V
vRa−SNK	Ra Detection Threshold for CC Pin for Sink		0.15	0.20	0.25	V
vRd−def	Rd Default Current Detection Threshold for Sink		0.61	0.66	0.70	V
vRd−1.5A	Rd 1.5 A Current Detection Threshold for Sink		1.16	1.23	1.31	V
vRd−3.0A	Rd 3 A Current Detection Threshold for Sink		2.04	2.11	2.18	V
zOPEN	CC resistance for disabled state, ROLECTRL = 0Fh		126			kΩ
vVCONNthr	Valid VCONN Voltage Assumes PWRCTRL.EN_VCONN = 1b				2.4	V
tTCPCfilter	Debounce time on CC lines to prevent CCSTAT change in case of minor changes in voltage on CC because of noise		4		500	μs
tCCDebounce	Debounce Time for CC Attach Detection		100	150	200	ms
tPDDebounce (Note 13)	Time a port shall wait before it can determine there has been a change in USB Type−C current due to the potential for USB−PD BMC signaling on CC		10	15	20	ms
tSetReg	Time between CC status change and I2C registers updated				50	μs
tTCPCSampleRate	CC Sample rate for indicating changes on CC lines				1	ms
tDRP	Sum of tToggleSrc and tToggleSnk timers		50		100	ms
tToggleSrc	Time Spent in Apply Rp before transitioning to Apply Rd	DRPTOGGLE = 00	15		30	ms
		DRPTOGGLE = 01	20		40	ms
		DRPTOGGLE = 10	25		50	ms
		DRPTOGGLE = 11	30		60	ms
tToggleSnk	Time Spent in Apply Rd before transitioning to Apply Rp	DRPTOGGLE = 00	35		70	ms
		DRPTOGGLE = 01	30		60	ms
		DRPTOGGLE = 10	25		50	ms
		DRPTOGGLE = 11	20		40	ms

12. RDEVICE minimum and maximum specifications are only guaranteed when power is applied.
13. Only Applicable to Autonomous Debug State machine.

Table 11. VBUS MEASUREMENT CHARACTERISTICS

Symbol	Parameter		T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C			Unit
			Min	Typ	Max	
vMDACstepVBUS	VBUS Measure block LSB reported on VBUS_VOLTAGE[9:0] register			25		mV
pMDACVBUS	Accuracy of VBUS Voltage Measurement	T_A = −40 to +85°C			±2	%
		T_A = +85 to +105°C (Note 12)			±5	%
tVBUSsample	Sampling period of VBUS Measurement			3		ms
vVBUSthr	VBUS threshold at which VBUS_VAL interrupt is triggered. Assumes VBUS present detection is enabled	VDD > V_{DDGOOD}	3.5		4.0 (Note 14)	V
		VDD < V_{DDGOOD} (Dead Battery)	3.4		4.0	
vVBUShys	Hysteresis on VBUS Comparator			50		mV
vSafe0Vthr	Safe Operating Voltage at “Zero Volts” Threshold				0.8	V
vSafe0Vhys	vSafe0V Hysteresis			40		mV
vALARMLSB	LSB of VBUS thresholds for VBUS_SNK_DISCL VBUS_STOP_DISCL VALARMHCFGL VALARMLCFGL			50		mV
pALARM	Accuracy of VBUS thresholds for VBUS_SNK_DISCL VBUS_STOP_DISCL VALARMHCFGL VALARMLCFGL				±5	%

14. FUSB307BVMPX vVBUSthr (max) = 4.05 V.

Table 12. SOURCE AND SINK CONTROL SPECIFICATIONS

Symbol	Parameter		T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C			
			Min	Typ	Max	Unit
R_{BLEED}	Equivalent Resistance for bleed discharging VBUS	VBUS = 4.0 V to 21.5 V	4		7	kΩ
vSrcSlewNeg	Maximum slew rate allowed when discharging VBUS	VBUS = 4.0 V to 21.5 V			30	mV/μs
tSafe0V	Time to reach vSafe0V max				650	ms
tSafe5V	Time to reach vSafe5V max				275	ms
tSrcSettle	Time to discharge to vSrcNew				275	ms
tAUTO_DISCH_FAIL	Time to declare auto discharge failure to discharge to vSafe0V	Device configured as Source. Measure from CCSTAT change to Open	650			ms
		Device configured as Sink. Measure from I_VBUS_SNK_DISC	440			ms
tAUTO_DISCH_FAIL_5V	Time to declare auto discharge failure to discharge to vSafe5v	Device configured as Source. Measure from CCSTAT change to Open	275			ms
		Device configured as Sink. Measure from I_VBUS_SNK_DISC	60			ms

Table 13. LDO SPECIFICATIONS

Symbol	Parameter	V_{DD}	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J = −40 to +125°C			Unit
				Min	Typ	Max	Unit
V_{V3P3}	LDO Output Voltage	< V_{DDGOOD}	VBUS = 4.0 V to 21.5 V	3.0		3.6	V
V_{LDO_VALID}	Valid VBUS_IN range for LDO operation	< V_{DDGOOD}		4.0		21.5	V
V_{DDGOOD}	VDD Voltage where device is powered from VDD instead of VBUS			2.7		3.0	V
I_{LDO_MAX}	Max. Output Current	< V_{DDGOOD}	VBUS = 4.0 V to 21.5 V, V_{DROP} = 120 mV	30			mA

Table 14. OVER-TEMPERATURE SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
T_{SHUT}	Temp. for VCONN Switch Turn Off		145		°C
T_{HYS}	Temp. Hysteresis for VCONN Switch Turn On		10		°C

Table 15. WATCHDOG TIMER SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
$T_{HVWatchdog}$	Time from last I2C transaction or INTB pin assertion to entering ErrorRecovery	1500		2000	ms

Table 16. IO SPECIFICATIONS

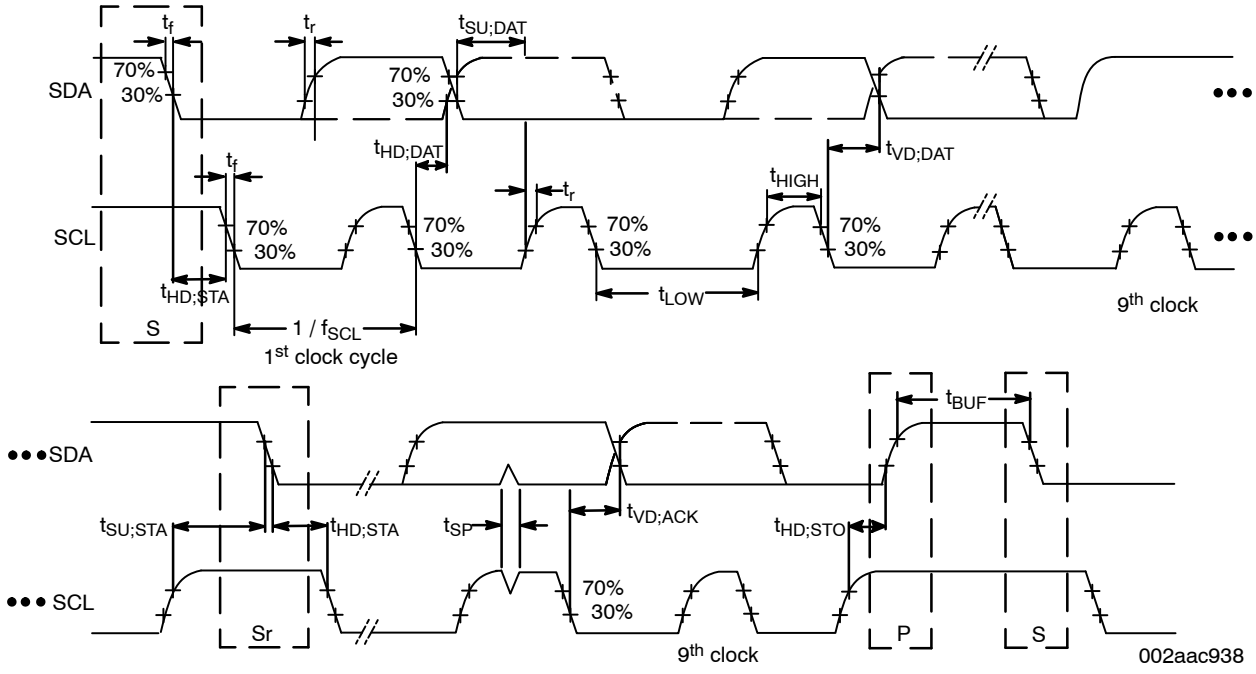
Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J= −40 to +125°C Min	Typ	Max	Unit
HOST INTERFACE PINS(INT_N, DBG_N)							
V_{OLINTN}	Output Low Voltage	3.0 to 5.5	I_{OL} = 4 mA			0.4	V
GPIOS, ORIENT AND MUX_SEL PINS							
V_{IL}	Low−Level Input Voltage	3.0 to 5.5				0.4	V
V_{IH}	High−Level Input Voltage	3.0 to 5.5		1.2			V
V_{OL}	Low−Level Output Voltage	3.0 to 5.5	I_{OL} = 4 mA			0.4	V
V_{OH}	High−Level Output Voltage	3.0 to 5.5	I_{OH} = −2 mA	$0.7V_{DD}$			V
I_{IN}	Input Leakage	3.0 to 5.5	Input Voltage 0 V to 5.5 V (When GPIO is setup as an input or Tri−Stated output)	−5		5	μA
I_{OFF}	Off Input Leakage	0	Input Voltage 0 V to 5.5 V	−5		5	μA
SRC, SNK AND SRC_HV							
V_{OL}	Low−Level Output Voltage	3.0 to 5.5	I_{OL} = 4 mA			0.4	V
V_{OH}	High−Level Output Voltage	3.0 to 5.5	I_{OH} = −2 mA	$0.7V_{DD}$			V
I^2C INTERFACE PINS – STANDARD, FAST OR FAST MODE PLUS SPEED MODE SDA, SCL) (Note 15)							
V_{DDEXT}	External power supply to which SDA and SCL are pulled up			1.8		3.6	V
Symbol	**Parameter**	**V_{DD} (V)**	**Conditions**	**T_A = −40 to +85°C T_A = −40 to +105°C (Note 17) T_J= −40 to +125°C Min.**	**Typ.**	**Max.**	**Unit**
V_{ILI2C}	Low−Level Input Voltage	3.0 to 5.5				0.4	V
V_{IHI2C}	High−Level Input Voltage	3.0 to 5.5		1.2			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	3.0 to 5.5		0.2			V
I_{i2C}	Input Current of SDA and SCL Pins,	3.0 to 5.5	Input Voltage 0.26 V to 2 V	−10		10	μA
I_{CCTI2C}	VDD current when SDA or SCL is HIGH	3.0 to 5.5	Input Voltage 1.8 V	−10		10	μA
V_{OLSDA}	Low−Level Output Voltage at 2 mA Sink Current (Open−Drain)	3.0 to 5.5		0		0.36	V
I_{OLSDA}	Low−Level Output Current (Open−Drain)	3.0 to 5.5	V_{OLSDA} = 0.4 V	20			mA
C_I	Capacitance for Each I/O Pin (Note 16)	3.0 to 5.5			5		pF

15. I^2C pull up voltage is required to be between 1.71 V and V_{DD}.

Table 17. FAST MODE PLUS I²C SPECIFICATIONS

Symbol	Parameter	Fast Mode Plus		
		Min.	Max.	Unit
f_{SCL}	I2C_SCL Clock Frequency	0	1000	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.26		μs
t_{LOW}	Low Period of I2C_SCL Clock	0.5		μs
t_{HIGH}	High Period of I2C_SCL Clock	0.26		μs
$t_{SU;STA}$	Set−up Time for Repeated START Condition	0.26		μs
$t_{HD;DAT}$	Data Hold Time	0		μs
$t_{SU;DAT}$	Data Set−up Time	50		ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals	20 × (V_{DD}/5.5 V)	120	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals (Note 16)	20 × (V_{DD}/5.5 V)	120	ns
$t_{SU;STO}$	Set−up Time for STOP Condition	0.26		μs
t_{BUF}	Bus−Free Time between STOP and START Conditions	0.5		μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

16. Guaranteed by characterization. Not production tested.
17. Automotive part only, FUSB307BVMPX.



V_{IL} = 0.3V_{DD}
V_{IH} = 0.7V_{DD}

Figure 19. Definition of Timing for Full−Speed Mode Devices on the I2C Bus

Table 18. REGISTER DEFINITIONS

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VENDIDL	R	79h	Vendor ID Low							
01h	VENDIDH	R	07h	Vendor ID High							
02h	PRODIDL	R	33h	Product ID Low							
03h	PRODIDH	R	01h	Product ID High							
04h	DEVIDL	R	02h	Device ID Low							
05h	DEVIDH	R	02h	Device ID High							
06h	TYPECREVL	R	12h	USB Type−C Revision Low							
07h	TYPECREVH	R	00h	USB Type−C Revision High							
08h	USBPDVER	R	12h	USB PD Version							
09h	USBPDREV	R	20h	USB PD Revision							
0Ah	PDIFREVL	R	12h	USB PD Interface Revision Low (Version)							
0Bh	PDIFREVH	R	10h	USB PD Interface Revision High (Revision)							
10h	ALERTL	R/WC	00h	I_VBUS_ALRM_HI	I_TXSUCC	I_TXDISC	I_TXFAIL	I_RXHRDRST	I_RXSTAT	I_PORT_PWR	I_CCSTAT
11h	ALERTH	R/WC	00h	I_VD_ALERT	Reserved	Reserved	Reserved	I_VBUS_SNK_DISC	I_RX_FULL	I_FAULT	I_VBUS_ALRM_LO
12h	ALERTMSKL	R/W	FFh	M_VBUS_ALRM_HI	M_TXSUCC	M_TX_DISC	M_TXFAIL	M_RXHRDRST	M_RXSTAT	M_PORT_PWR	M_CCSTAT
13h	ALERTMSKH	R/W	0Fh	M_VD_ALERT	Reserved	Reserved	Reserved	M_VBUS_SNK_DISC	M_RX_FULL	M_FAULT	M_VBUS_ALRM_LO
14h	PWRSTATMSK	R/W	FFh	M_DEBUG_ACC	M_INIT	M_SRC_HV	M_SRC_VBUS	M_VBUS_VAL_EN	M_VBUS_VAL	M_VCONN_VAL	M_SNKVBUS
15h	FAULTSTATMSK	R/W	B3h	M_ALL_REGS_RESET	Reserved	M_AUTO_DISCH_FAIL	M_FORCE_DISCH_FAIL	Reserved	Reserved	M_VCONN_OCP	M_I2C_ERR
16h..17h	Reserved	R	00h	Reserved							
18h	STD_OUT_CFG	R/W	40h	TRI_STATE	DEBUG_ACC	Reserved	Reserved	MUX_CTRL		Reserved	ORIENT
19h	TCPC_CTRL	R/W	00h	Reserved		EN_WATCHDOG	DEBUG_ACC_CTRL	I2C_CLK_STRECTH		BIST_TMODE	ORIENT
1Ah	ROLECTRL	R/W	0Ah 4Ah	Reserved	DRP	RP_VAL		CC2_TERM		CC1_TERM	

Table 18. REGISTER DEFINITIONS (continued)

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Bh	FAULTCTRL	R/W	00h	Reserved			Reserved	DISCH_TIMER_DIS	Reserved	Reserved	VCONN_OCP_DIS
1Ch	PWRCTRL	R/W	60h	Reserved	VBUS_MON	DIS_VALRM	AUTO_DISCH	EN_BLEED_DISCH	FORCE_DISCH	VCONN_PWR	EN_VCONN
1Dh	CCSTAT	R	00h/20h	Reserved		LOOK4CON	CON_RES	CC2_STAT		CC1_STAT	
1Eh	PWRSTAT	R	08h	DEBUG_ACC	TCPC_INIT	SOURCE_HV	SOURCE_VBUS	VBUS_VAL_EN	VBUS_VAL	VCONN_VAL	SNKVBUS
1Fh	FAULTSTAT	R	80h	ALL_REGS_RESET	Reserved	AUTO_DISCH_FAIL	FORCE_DISCH_FAIL	Reserved	Reserved	VCONN_OCP	I2C_ERR
20h..22h	Reserved	R	00h	Reserved							
23h	COMMAND	R	00h	Command							
24h	DEVCAP1L	R	DDh	ROLES_SUPPORT			ROLES_SUPPORT	SWITCH_VCONN	SNK_VBUS	SRC_HV	SRC_VBUS
25h	DEVCAP1H	R	1Eh	Reserved			BLEED_DIS	FORCE_DIS	VBUS_MEAS_ALRM	RP_SUPPORT	
26h	DEVCAP2L	R	D7h	SNK_DISC_DETECT	STOP_DISCH	VBUS_ALRM_LSB		VCONN_POWER_CAP			VCONN_FAULT_CAP
27h	DEVCAP2H	R	01h	Reserved							Watchdog Timer
28h	STD_IN_CAP	R	00h	Reserved							
29h	STD_OUT_CAP	R	41h	Reserved	DEBUG_ACC	Reserved			MUX_CTRL	Reserved	ORIENT
2Ah..2Dh	Reserved	R	00h	Reserved							
2Eh	MSGHEADR	R/W	02h	Reserved			Cable Plug	Data Role	USB PD Rev		PWR Role
2Fh	RXDETECT	R/W	00h	Reserved	EN_CABLE_RST	EN_HRD_RST	EN_SOP2_DBG	EN_SOP1_DBG	EN_SOP2	EN_SOP1	EN_SOP
30h	RXBYTECNT	R	00h	Received Byte Count							
31h	RXSTAT	R	00h	Reserved					Received SOP* Message		
32h	RXHEADL	R	00h	Received Header Low							
33h	RXHEADH	R	00h	Received Header High							
34h..4Fh	RXDATA	R	00h	Received Data Payload							
50h	TRANSMIT	R/W	00h	Reserved		Retry Counter		Reserved	Transmit SOP* Message		

Table 18. REGISTER DEFINITIONS (continued)

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
51h	TXBYTECNT	R/W	00h	Transmit Byte Count							
52h	TXHEADL	R/W	00h	Transmit Header Low							
53h	TXHEADH	R/W	00h	Transmit Header High							
54h..6F	TXDATA	R/W	00h	Transmit Payload							
70h	VBUS_VOLTAGE_L	R	00h	VBUS Measurement Output							
71h	VBUS_VOLTAGE_H	R	00h								
72h	VBUS_SNK_DISCL	R/W	A0h	VBUS SINK Disconnected Threshold (See Register Description Table)							
73h	VBUS_SNK_DISCH	R/W	1Ch								
74h	VBUS_STOP_DISCL	R/W	00h	VBUS Discharge Stop Threshold (See Register Description Table)							
75h	VBUS_STOP_DISCH	R/W	00h								
76h	VALARMHCFGL	R/W	00h	Voltage High Trip Point (See Register Description Table)							
77h	VALARMHCFGH	R/W	00h								
78h	VALARMLCFGL	R/W	00h	Voltage Low Trip Point (See Register Description Table)							
79h	VALARMLCFGH	R/W	00h								
7Ah..7Fh	Reserved	R/W	00h	Reserved							
A0h	VCONN_OCP	R/W	0Fh	Reserved				OCP_RANGE	OCP_CUR		
A2h	RESET	R/WC	00h	Reserved						PD_RST	SW_RST
A4h	GPIO1_CFG	R/W	00h	Reserved					GPO1_VAL	GPI1_EN	GPO1_EN
A5h	GPIO2_CFG	R/W	00h	Reserved				FR_SWAP_FN	GPO2_VAL	GPI2_EN	GPO2_EN
A6h	GPIO_STAT	R	00h	Reserved						GPI2_VAL	GPI1_VAL
A7h	DRPTOGGLE	R/W	00h	Reserved						DRPTOGGLE	
A9h..AFh	Reserved	R	00h	Reserved							
B0h	SINK_TRANSMIT	R/W	40h	Reserved	DIS_SNK_TX	Retry Counter		Reserved	Transmit SOP* Message		
B1h	SRC_FRSWAP	R/W	00h	Reserved				FRSWAP_SNK_DELAY		MANUAL_SNK_EN	FR_SWAP
B2h	SNK_FRSWAP	R/W	00h	Reserved							EN_FRSWAP_DTCT

Table 18. REGISTER DEFINITIONS (continued)

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B3h	ALERT_VD	R/W	00h	Reserved	I_DISCH_ SUCC	I_GPI2	I_GPI1	I_VDD_ DTCT	I_OTP	I_SWAP_TX	I_SWAP_RX
B4h	ALERT_VD_MSK	R/W	7Fh	Reserved	M_DISCH_ SUCC	M_GPI2	M_GPI1	MI_VDD_ DTCT	M_OTP	M_SWAP_ TX	M_SWAP_ RX

Table 19. VENDIDL
Address: 00h
Reset Value: 0x79
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Vendor ID Low Description
7:0	VENDIDL	R	8	**onsemi** Vendor ID Low: 79h

Table 20. VENDIDH
Address: 01h
Reset Value: 0x07
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Vendor ID High Description
7:0	VENDIDH	R	8	**onsemi** Vendor ID High: 07h

Table 21. PRODIDL
Address: 02h
Reset Value: See Below
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Product ID Low Description
7:0	PRODIDL	R	8	Product ID Low, FUSB307B: 33h

Table 22. PRODIDH
Address: 03h
Reset Value: 0x01h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Product ID High Description
7:0	PRODIDH	R	8	Product ID High, All: 1h

Table 23. DEVIDL
Address: 04h
Reset Value: 0x02h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device ID Low (Version) Description
7:0	DEVIDL	R	8	Version ID: 02h A_[Revision ID]: 0x01 (e.g. A_revA) B_[Revision ID]: 0x02 (e.g. B_revA) C_[Revision ID]: 0x03 (e.g. C_revA) etc

Table 24. DEVIDH
Address: 05h
Reset Value: 0x02h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device ID High (Revision) Description
7:0	DEVIDH	R	8	Revision ID: 02h [Version ID]_revA: 0x00 (e.g. A_revA) [Version ID]_revB: 0x01 (e.g. A_revB) [Version ID]_revC: 0x02 (e.g. A_revC) etc

Table 25. TYPECREVL
Address: 06h
Reset Value: 0x12h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Type−C Revision Low Description
7:0	TYPECREVL	R	8	Type−C Revision Low: 12h

Table 26. TYPECREVH
Address: 07h
Reset Value: 0x00h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Type−C Revision High Description
7:0	TYPECREVH	R	8	Type−C Revision High: 00h

Table 27. USBPDVER
Address: 08h
Reset Value: 0x12h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB−PD Version Description
7:0	USBPDVER	R	8	USB−PD Version: 12h

Table 28. USBPDREV
Address: 09h
Reset Value: 0x20h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB−PD Revision Description
7:0	USBPDREV	R	8	USB−PD Revision: 20h

Table 29. PDIFREVL
Address: 0Ah
Reset Value: 0x12h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB−PD Interface Revision Low Description
7:0	PDIFREVL	R	8	USB−PD IF Version: 12h

Table 30. PDIFREVH
Address: 0Bh
Reset Value: 0x10h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB−PD Interface Revision High Description
7:0	PDIFREVH	R	8	USB−PD IF Revision: 10h

Table 31. ALERTL

Address: 10h

Reset Value: 0x00

Type: Read, Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	ALERT1 Description
7	I_VBUS_ALRM_HI	R/WC	1	Voltage Alarm Hi 0b: Cleared 1b: A high−voltage alarm has occurred
6	I_TXSUCC	R/WC	1	0b: Cleared 1b: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty
5	I_TXDISC	R/WC	1	0b: Cleared 1b: Reset or SOP* message transmission not sent due to incoming receive message. Transmit SOP* message buffer registers are empty
4	I_TXFAIL	R/WC	1	0b: Cleared 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
3	I_RXHRDRST	R/WC	1	Received Hard Reset 0b: Cleared 1b: Received Hard Reset message
2	I_RXSTAT	R/WC	1	Receive Status 0b: Cleared 1b: RXSTAT changed. RXBYTECNT being 0 does not set this register
1	I_PORT_PWR (Note 18)	R/WC	1	Port Power Status 0b: Cleared 1b: Port status changed. Read PWRSTAT register
0	I_CCSTAT	R/WC	1	CC Status 0b: Cleared 1b: CC status changed. Read CCSTAT register

18. ALERTL.I_PORT_PWR is asserted if the bit−wise AND of PWRSTAT and PWRSTAMSK results in any bits that have the value 1.
I_VBUS_SNK_DISC

Table 32. ALERTH

Address: 11h
Reset Value: 0x00
Type: Read, Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	ALERT2 Description
7	I_VD_ALERT	RWC	1	Vendor Defined Alert 0b: Cleared 1b: A Vendor Defined alert has occurred. Read ALERT_VD register
6:4	Reserved	R	3	Reserved: 000b
3	I_VBUS_SNK_DISC	RWC	1	VBUS Sink Disconnect Detected 0b: Cleared 1b: A VBUS Sink Disconnect Threshold crossing from High to Low has been detected
2	I_RX_FULL	RWC	1	Rx Buffer Overflow 0b: Internal RX Buffer is functioning properly 1b: Internal RX Buffer has overflowed Note: This interrupt indicates overflow of the internal buffer, not the RXDATA space. To clear overflow condition, write to ALERTL.I_RXSTAT Writing a 1 to this register acknowledges the overflow. The actual overflow is cleared by writing to ALERTL. I_RXSTAT
1	I_FAULT (Note 19)	R/WC	1	Fault Alarm 0b: Cleared 1b: A Fault alarm has occurred. Read FAULTSTAT register
0	I_VBUS_ALRM_LO	R/WC	1	Voltage Alarm Lo 0b: Cleared 1b: A low−voltage alarm has occurred

19. ALERTH.I_FAULT is asserted if the bit−wise AND of FAULTSTAT and FAULTSTAMSK results in any bits that have the value 1.

Table 33. ALERTMSKL

Address: 12h
Reset Value: 0xFF (Resets on POR, SW_RST and Hard Reset)
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Alert Mask 1 Description
7	M_VBUS_ALRM_HI	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
6	M_TXSUCC	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
5	M_TX_DISC	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
4	M_TXFAIL	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
3	M_RXHRDRST	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked Note: Generally this interrupt should not be masked
2	M_RXSTAT	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
1	M_PORT_PWR	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
0	M_CCSTAT	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked

Table 34. ALERTMSKH

Address: 12h
Reset Value: 0xFF (Resets on POR, SW_RST and Hard Reset)
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Alert Mask 2 Description
7	M_VD_ALERT	RW	1	0b: Interrupt masked, 1b: Interrupt unmasked
6:4	Reserved	R	3	Reserved: 000b
3	M_VBUS_SNK_DISC	RW	1	0b: Interrupt masked, 1b: Interrupt unmasked
2	M_RX_FULL	RW	1	0b: Interrupt masked, 1b: Interrupt unmasked
1	M_FAULT	RW	1	0b: Interrupt masked, 1b: Interrupt unmasked
0	M_VBUS_ALRM_LO	RW	1	0b: Interrupt masked, 1b: Interrupt unmasked

Table 35. PWRSTATMSK

Address: 14h
Reset Value: 0xFF (Resets on POR, SW_RST and Hard Reset)
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Power Status Mask Description
7	M_DEBUG_ACC	RW	1	Debug Accessory Connected Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
6	M_INIT	RW	1	TCPC Initialization Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
5	M_SRC_HV	RW	1	Sourcing High Voltage Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
4	M_SRC_VBUS	RW	1	Sourcing VBUS Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
3	M_VBUS_VAL_EN	RW	1	VBUS Valid Detection Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
2	M_VBUS_VAL	RW	1	VBUS Valid Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
1	M_VCONN_VAL	RW	1	VCONN Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	M_SNKVBUS	RW	1	Sinking VBUS Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked

Table 36. FAULTSTATMSK

Address: 15h

Reset Value: 0xB3 (Resets on POR, SW_RST and Hard Reset)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Fault Status Mask Description
7	M_ALL_REGS_RESET	RW	1	All Registers Reset to Default 0b: Interrupt masked 1b: Interrupt unmasked
6	Reserved	R	1	Reserved: 0b
5	M_AUTO_DISCH_FAIL	RW	1	Auto Discharge Fail Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
4	M_FORCE_DISCH_FAIL	RW	1	Force Discharge Fail Interrupt Mask 0b: Interrupt Masked 1b: Interrupt Unmasked
3	Reserved	R	1	Reserved: 0b
2	Reserved	R	1	Reserved: 0b
1	M_VCONN_OCP	RW	1	VCONN OCP Interrupt Mask 0b: Interrupt Masked 1b: Interrupt Unmasked
0	M_I2C_ERROR	RW	1	I2C Interface Error Interrupt Mask 0b: Interrupt Masked 1b: Interrupt Unmasked

Table 37. STD_OUT_CFG

Address: 18h

Reset Value: 0x40

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Standard Outputs Configuration
7	TRI_STATE	R/W	1	0b: Standard Output Control 1b: Force all outputs to tri−state
6	DEBUG_ACC	R/W	1	0b: Debug Connected output is driven Low 1b: No Debug Accessory Connected output is driven High Note: The FUSB307B ignores writes to this bit if TCPC_CTRL.DEBUG_ACC_CTRL = 0b
5	Reserved	R	1	Reserved: 0b
4	Reserved	R	1	Reserved: 0b
3:2	MUX_CTRL	R/W	2	Controls MUX_S0 and MUX_S1 Outputs. 00b: MUX_S0 = 0, MUX_S1 = 0. No connection. 01b: MUX_S0 = 1, MUX_S1 = 0. *USB3.1 Connected* 10b: MUX_S0 = 0, MUX_S1 = 1. *DP Alternate Mode − 4 lanes* 11b: MUX_S0 = 1, MUX_S1 = 1. USB3.*1 + Display Port Lanes 0 & 1*
1	Reserved	R	1	Reserved: 0b
0	ORIENT	R/W	1	Controls ORIENT Output 0b: Normal (CC1 = A5, CC2 = B5, TX1 = A2/A3, RX1 = B10/B11) 1b: Flipped (CC2 = A5, CC1 = B5, TX1 = B2/B3, RX1 = A10/A11)

Table 38. TCPC_CTRL

Address: 19h

Reset Value: 0x00 (POR, and SW_RST)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	TCPC Control Register
7:4	Reserved	R	2	Reserved: 00b
5	EN_WATCHDOG	R/W	1	0b: Watchdog Monitoring is disabled (default) 1b: Watchdog Monitoring is enabled
4	DEBUG_ACC_CTRL	R/W	1	Debug Accessory Control 0b: Standard Output is Controlled by FUSB307B 1b: Standard Output is Controlled by external processor Note: See: Debug Accessory State Machine
3:2	I2C_CLK_STRETCH	R	2	00b: I2C clock stretching is disabled. Writing to these register bits will be ignored.
1	BIST_TMODE	R/W	1	BIST Test Data Receive Enable 0b: Normal Operation. Incoming messages are stored and passed to host 1b: BIST Test Mode. Receive buffer is cleared immediately after GoodCRC response.
0	ORIENT	R/W	1	Plug Orientation 0b: When Vconn is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When Vconn is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled.

Table 39. ROLECTRL

Address: 1Ah

Reset Value (Note 19) 0x0A for FUSB307B Device in dead battery, 0x4A for non−dead−battery.

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Role Control Description
7	Reserved	R	1	Reserved: 0b
6	DRP (Notes 21, 22)	R/W	1	0b: No DRP. Bits B3..0 determine Rp/Rd/Ra settings 1b: DRP
5:4	RP_VAL	R/W	2	00b: Rp default 01b: Rp 1.5 A 10b: Rp 3.0 A 11b: Reserved
3:2	CC2_TERM (Notes 23, 24)	R/W	2	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care)
1:0	CC1_TERM (Notes 23, 24)	R/W	2	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care)

20. Reset values are loaded on either VBUS or VDD power up. Dead battery Reset values loaded on VBUS power up will be maintained when battery is eventually present.
21. Rp value is defined in B5..4 when performing the DRP toggling as well as when a connection is resolved.
22. The FUSB307B toggles CC1 & CC2 after receiving a.LOOK4CON and until a connection is detected. Upon connection, the FUSB307B resolves to either an Rp or Rd and report the CC1/CC2 State in the CCSTAT register. The FUSB307B will continue to present the resolved Rd or Rp regardless of any changes voltage on the CC wires.
23. When CCx_TERM bits are set to Open and DRP = 0, the PHY and CC comparators will power down.
24. If DRP = 1, LOOK4CON starts toggling with the value set in CC1_TERM/CC2_TERM. If CC1_TERM/CC2_TERM is different than Rp/Rp or Rd/Rd, the COMMAND will be ignored.

Table 40. FAULTCTRL

Address: 1Bh
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Fault Control Description
7:4	Reserved	R	4	Reserved: 0000b
3	DISCH_TIMER_DIS	R/W	1	Auto and Force VBUS Discharge Timer Enable 0b: VBUS Discharge timer is enabled 1b: VBUS Discharge timer is disabled
2	Reserved	R	1	Reserved: 0b
1	Reserved	R	1	Reserved: 0b
0	VCONN_OCP_DIS	R/W	1	VCONN OCP Enable 0b: VCONN OCP Enabled 1b: VCONN OCP Disabled

Table 41. PWRCTRL

Address: 1Ch
Reset Value: 0x60
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Power Control Description
7	Reserved	R	1	Reserved: 0b
6	DIS_VBUS_MON (Note 25)	R/W	1	Controls VBUS_VOLTAGE_L Monitoring. 0b: VBUS Voltage Monitoring is enabled 1b: VBUS Voltage Monitoring is disabled
5	DIS_VALARM	R/W	1	Disables VALARMHCFGL and VALARMLCFGL 0b: Voltage Alarm reporting is enabled 1b:Voltage Alarm reporting is disabled
4	AUTO_DISCH (Notes 26, 28)	R/W	1	Auto Discharge on Disconnect 0b: Turn Off Automatically Discharge VBUS based on VBUS Voltage 1b: Turn On Automatically Discharge VBUS based on VBUS Voltage
3	EN_BLEED_DISCH (Note 30)	R/W	1	Enable Bleed Discharge 0b: Disable bleed discharge of VBUS 1b: Enable bleed discharge of V_{BUS}
2	FORCE_DISCH (Note 27, 29)	R/W	1	Force Discharge 0b: Disable forced discharge of VBUS 1b: Enable forced discharge of V_{BUS}
1	VCONN_PWR	R/W	1	V_{CONN} Power Supported Writing this bit has no function. Please use VCONN_OCP to set OCP values
0	EN_VCONN	R/W	1	Enable V_{CONN} 0b: Disable V_{CONN} Source (default) 1b: Enable V_{CONN} Source to CC

25. If VBUS_MON is disabled, VBUS_VOLTAGE_L and VBUS_VOLTAGE_H reports all zeroes.
26. Setting this bit in a Source FUSB307B triggers the following actions upon disconnection detection:
    1. Disable sourcing power over Vbus
    2. VBUS discharge
27. Sourcing power over Vbus shall be disabled before or at same time as starting VBUS discharge.
28. Setting this bit in a Sink FUSB307B triggers the following action upon disconnection detection:
    1. VBUS discharge
29. The FUSB307B will automatically disable discharge once the voltage on VBUS is below vSafe0V (max.).
30. Bleed Discharge is a low current discharge to provide a minimum load current if needed.

Table 42. CCSTAT

Address: 1Dh
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	CC Status Description (Note 31)
7:6	Reserved	R	2	Reserved: 00b
5	LOOK4CON	R	1	0b: the FUSB307B is not looking for connection or indicated a potential connection has been found when transitioned from a 1 to 0 1b: the FUSB307B looking for connection
4	CON_RES	R	1	0b: the FUSB307B is presenting Rp 1b: the FUSB307B is presenting Rd This bit is only valid if the FUSB307B was a DRP and has stopped DRP toggling

3:2	CC2_STAT	R	2	If (ROLE_CONTROL.CC2 = Rp) or (CON_RES = 0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: reserved
				If (ROLE_CONTROL.CC2 = Rd) or (CON_RES = 1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd−Connect)
				10b: SNK.Power1.5 (Above minimum vRd−Connect) Detects Rp 1.5 A
				11b: SNK.Power3.0 (Above minimum vRd−Connect) Detects Rp 3.0 A
				If ROLE_CONTROL.CC2=Ra, this field is set to 00b
				If ROLE_CONTROL.CC2=Open, this field is set to 00b
				This field always returns 00b if (LOOK4CON = 1) or (PWRCTRL.EN_VCONN = 1 and TCPC_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

1:0	CC1_STAT	R	2	If (ROLE_CONTROL.CC1 = Rp) or (CON_RES = 0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: reserved
				If (ROLE_CONTROL.CC1 = Rd) or CON_RES = 1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd−Connect)
				10b: SNK.Power1.5 (Above minimum vRd−Connect) Detects Rp−1.5 A
				11b: SNK.Power3.0 (Above minimum vRd−Connect) Detects Rp−3.0 A
				If ROLE_CONTROL.CC1 = Ra, this field is set to 00b
				If ROLE_CONTROL.CC1 = Open, this field is set to 00b
				This field always returns 00b if (LOOK4CON = 1) or (PWRCTRL.EN_VCONN = 1 and TCPC_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

31. An event change on this register cause an ALERTL.I_CCSTAT Interrupt.

Table 43. PWRSTAT

Address: 1Eh
Reset Value: 08h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Power Status Description (Note 32)
7	DEBUG_ACC	R	1	Debug Accessory Attached 0b: No Debug Accessory Connected 1b: Debug Accessory Connected Reflects the state of the DEBUG_ACC Output if present
6	TCPC_INIT	R	1	FUSB307B Initialization Status 0b: The FUSB307B has completed initialization and all registers are valid 1b: The FUSB307B is still performing internal initialization. Registers 00−0Fh are valid
5	SOURCE_HV	R	1	Sourcing High Voltage. See Transition Flow Charts for details. 0b: vsafe5V 1b: High Voltage
4	SOURCE_VBUS	R	1	Sourcing VBUS. Output SRC asserted. 0b: Sourcing VBUS is disabled 1b: Sourcing VBUS is enabled
3	VBUS_VAL_EN	R	1	VBUS_VAL (below) Detection Circuit Status 0b: VBUS_VAL Detection is Disabled 1b: VBUS_VAL Detection is Enabled
2	VBUS_VAL	R	1	V_{BUS} Present 0b: V_{BUS} disconnected (below 3.5 V) 1b: V_{BUS} connected (Above 4.0 V)
1	VCONN_VAL	R	1	V_{CONN} Present 0b: V_{CONN} is not present or PWRCTRL.EN_VCONN is disabled 1b: This bit is asserted when V_{CONN} is present on CC1 or CC2 Threshold is fixed at 2.4 V
0	SNKVBUS	R	1	Sink VBUS. Output SNK asserted. 0b: Sink is disconnected or not supported 1b: FUSB307B has enabled the sink path

32. An event change on this register cause an ALERTL.I_PWRSTAT Interrupt.

Table 44. FAULTSTAT

Address: 1Fh
Reset Value: 0x80
Type: Read/Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	Fault Status Interrupt Description (Note 33)
7	ALL_REGS_RESET Note	R/WC	1	0b: No reset occurred 1b: POR or unexpected power reset occurred This bit is asserted when the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs
6	Reserved	R	1	Reserved: 0b
5	AUTO_DISCH_FAIL (Note 34)	R/WC	1	0b: No Discharge Failure 1b: VBUS Discharge Failed Asserts when PWRCTRL.AUTO_DISCH is set and FUSB307B fails to discharge VBUS to vSafe5V (max.) within tSafe5V or vSafe0V(max.) within tSafe0V from disconnection is detected
4	FORCE_DISCH_FAIL	R/WC	1	0b: No Discharge Failure 1b: VBUS Discharge Failed
3	Reserved	R	1	Reserved: 0b
2	Reserved	R	1	Reserved: 0b

Table 44. FAULTSTAT (continued)
Address: 1Fh
Reset Value: 0x80
Type: Read/Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	Fault Status Interrupt Description (Note 33)
1	VCONN_OCP	R/WC	1	0b: No VCONN Over−Current Detected 1b: Over current on VCONN Latched. See VCONN_ Registers to set VCONN OCP levels.
0	I2C_ERROR	R/WC	1	0b: No Error 1b: I2C Error has occurred Asserts when: or SINK_TRANSMIT has been sent with TRANSMIT_BUFFER empty (TXBYTECNT < 2). COMMAND.DisableVbusDetect is issued while sinking or sourcing VBUS.COMMAND.SinkVbus is issued while sourcing VBUSCOMMAND.SourceVbusDefaultVoltage is issued while sinking VBUS COMMAND.SourceVbusHighVoltage is issued when device is not already sourcing 5 V, is sinking, or is not capable of sourcing high voltage Connect_Invalid State is reached

33. Fault Status are latched and cleared when a 1 is written to the corresponding bit.
34. ALL_REGS_RESET do not get set on SW_RST.

Table 45. COMMAND

Address: 23h

Reset Value: 0x00

Type: Read/Write (Auto−Clear)

Bit #	Name	R/W/C	Size (Bits)	Register Settings	COMMAND Description
7:0	Command	R/W	8	0001 0001b	WakeI2C (no action is taken other than to wake the I2C interface)
				0010 0010b	DisableVbusDetect. Disable Vbus present detection: PWRSTAT.VBUS_VAL. The FUSB307B will ignore this command and assert the FAULTSTAT.I2C_ERR if it has sourcing or sinking power over Vbus enabled
				0011 0011b	EnableVbusDetect. Enable Vbus present detection
				0100 0100b	DisableSinkVbus. Disable sinking power over Vbus. This COMMAND does not disable PWRSTAT.VBUS_VAL detection
				0101 0101b	SinkVbus. Enable sinking power over Vbus and enable Vbus present detection. The FUSB307B will ignore this command and assert the FAULTSTAT.I2C_ERR if it has sourcing power over Vbus enabled
				0110 0110b	DisableSourceVbus. Disable sourcing power over Vbus. This COMMAND does not disable PWRSTAT.VBUS_VAL detection
				0111 0111b	SourceVbusDefaultVoltage. Enable sourcing vSafe5V over Vbus and enable Vbus present detection. Source shall transition to vSafe5V if at a high voltage. The FUSB307B will ignore this command and assert the FAULTSTAT.I2C_ERR if it has sinking power over Vbus enabled
				1000 1000b	SourceVbusHighVoltage. Execute sourcing high voltage over Vbus. FUSB307B will ignore this command and assert the FAULTSTAT.I2C_ERR
				1001 1001b	LOOK4CON. Start DRP Toggling if ROLECTRL.DRP = 1b. If ROLECTRL.CC1/CC2 = 01b start with Rp, if ROLECTRL.CC1/CC2 =10b start with Rd. If ROLE_CONTROL.CC1/CC2 are not either 01b/01b or 10b/10b, then do not start toggling. The TCPM shall issue . COMMAND.LOK4CON to enable the device to restart Connection Detection in cases where the ROLECTRL contents will not change. An example of this is when a potential connection as a Source occurred but was further debounced by the TCPM to find the Sink disconnected. In this case a Source Only or DRP should go back to its Unattached.Src state. This would result in ROLECTRL staying the same
				1010 1010b	RxOneMore. Configure the receiver to automatically clear the RXDETECT register after sending the next GoodCRC. This is used to shutdown reception of packets at a known point regardless of packet separation or the depth of the receive FIFO in the device
				1100 1100b 1101 1101b 1110 1110b	Reserved. No Action
				1111 1111b	I2CIdle, Enter I2C Idle

Table 46. DEVCAP1L

Address: 24h
Reset Value: FUSB307B: DDh
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 1 L Description
7:5	ROLES_SUPPORT	R	3	Roles Supported: 000b: Type−C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only 011b: Sink with accessory support 100b: DRP Only 101b: Source, Sink, DRP, Adapter/Cable all supported 110b: Source, Sink, DRP 110..111b: Not valid
4	SOP_SUPPORT	R	1	0b: All SOP* except SOP'_DBG/SOP"_DBG 1b: All SOP* messages are supported
3	SWITCH_VCONN	R	1	Supply VCONN: 0b: Not capable of switching VCONN 1b: Capable of switching VCONN Support for PWRSTAT.VCONN_VAL and PWRCTRL.EN_VCONN implemented
2	SNK_VBUS	R	1	Sink VBUS: 0b: Not Capable of controlling the sink path to the system load 1b: Capable of controlling the sink path to the system load Support for PWRSTAT.SNKVBUS and COMMAND.SinkVbus implemented
1	SRC_HV	R	1	Source Higher than vSafe5V on VBUS 0b: Not capable of controlling High Voltage Path on VBUS 1b: capable of controlling High Voltage Path on VBUS Support for PWRSTAT.SOURCE_HV and COMMAND.SourceVbusHighVoltage implemented
0	SRC_VBUS	R	1	Source vSafe5V on VBUS 0b: Not of controlling the source path to VBUS 1b: Capable of controlling the source path to VBUS Support for PWRSTAT.SOURCE_VBUS, COMMAND.SourceVbusDefaultVoltage, COMMAND.DisableSourceVbus, COMMAND.EnableVbusDetect, and COMMAND.DisableVbusDetect implemented

Table 47. DEVCAP1H

Address: 25h
Reset Value: 0x1E
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 1 H Description
7:5	Reserved	R	3	Reserved : 000b
4	BLEED_DIS	R	1	0b: No Bleed Discharge 1b: Bleed Discharge implement Support for PWRCTRL.EN_BLEED_DISCH implemented.
3	FORCE_DIS	R	1	0b: No Force Discharge 1b: Force Discharge implement Support for PWRCTRL.FORCE_DISCH, FAULTSTAT.FORCE_DISCH_FAIL, and VBUS_STOP_DISCL implemented

Table 47. DEVCAP1H (continued)
Address: 25h
Reset Value: 0x1E
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 1 H Description
2	VBUS_MEAS_ALRM	R	1	0b: No V_{BUS} voltage measurement or VBUS Alarms 1b: V_{BUS} voltage measurement and VBUS Alarms Support for VBUS_VOLTAGE_L, VALARMHCFGL and VALARMLCFGL implemented
1:0	RP_SUPPORT	R	2	Source Power Supported: 00b: Rp default only 01b: Rp 1.5 A and default 10b: Rp 3.0A, 1.5 A and default 11b: Reserved

Table 48. DEVCAP2L
Address: 26h
Reset Value: 0xD7
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 2 L Description
7	SNK_DISC_DETECT	R	1	0b: VBUS_SNK_DISCL not implemented 1b: VBUS_SNK_DISCL implemented
6	STOP_DSICH	R	1	0b: VBUS_STOP_DISCL not implemented 1b: VBUS_STOP_DISCL implemented
5:4	VBUS_ALRM_LSB	R	2	VBUS Voltage Alarm LSB Support 01b: Voltage Alarm Supports 50 mV LSB Bit 0 of VALARMHCFGL and VALARMLCFGL are ignored
3:1	VCONN_POWER_CAP	R	3	VCONN Power Supported 000b: 1.0 W 001b: 1.5 W 010b: 2.0 W 011b: 3 W (at VCONN = 5.5 V) 100b: 4 W 101b: W 110b: 6 W 111b: External
0	VCONN_FAULT_CAP	R	1	VCONN OCP Fault Capable 110b: FUSB307B is not capable of detecting a VCONN fault 1b: FUSB307B is capable of detecting a VCONN fault

Table 49. DEVCAP2H
Address: 27h
Reset Value: 0x01
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 2 H Description
7:1	Reserved	R	7	Reserved: 000_0000b
0	Watchdog Timer	R	1	1b: Watchdog Timer Implemented

Table 50. STD_OUT_CAP
Address: 29h
Reset Value: FUSB307B: 0x41
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Standard Outputs Capabilities Description
7	Reserved	R	1	Reserved: 00b
6	DEBUG_ACC	R	1	0b: Debug Accessory Indicator Not Present 1b: Debug Accessory Indicator Present
5	VBUS_MON	R	1	0b: VBUS Present Monitor Not Present
4	AUDIO_ACC	R	1	0b: Audio Adapter Accessory Indicator Not Present
3	ACTIVE_CABLE	R	1	0b: Active Cable Indicator not Present
2	MUX_CTRL	R	1	0b: Mux Control Not Present
1	CON_PRESENT	R	1	0b: Connection Present indicator not implemented
0	ORIENT	R	1	1b: Connector Orientation Present

Table 51. MSGHEADR
Address: 2Eh
Reset Value: 0x02 for FUSB307B
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Message Header Info Description
7:5	Reserved	R	3	Reserved: 000b
4	CBL_PLUG	R/W	1	Cable Plug 0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug
3	DATA_ROLE	R/W	1	Data Role 0b: SINK 1b: SOURCE
2:1	USBPD_REV	R/W	2	USB−PD Specification Revision 00b: Revision 1.0 01b: Revision 2.0 10b − 11b: Reserved
0	POWER_ROLE	R/W	1	Power Role 0b: Sink 1b: Source

Table 52. RXDETECT
RXDETECT enables the types of messages and/or signaling to be detected. SOP* enabling also turns on auto−GoodCRC response. This register is reset when: A Hard Reset is received or sent; after the GoodCRC transmission due to RxOneMore; on a disconnect detection; SW_RST or POR.
Address: 2Fh
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Receive Detect Description (Note 35)
7	Reserved	R	1	Reserved: 0b
6	EN_CABLE_RST	R	1	0b: Do not detect Cable Reset signaling
5	EN_HRD_RST	R/W	1	0b: Do not detect Hard Reset signaling (default) 1b: Detect Hard Reset signaling
4	EN_SOP2_DBG	R/W	1	0b: Do not detect SOP_DBG” message (default) 1b: Detect SOP_DBG” message
3	EN_SOP1_DBG	R/W	1	0b: Do not detect SOP_DBG’ message (default) 1b: Detect SOP_DBG’ message

Table 52. RXDETECT (continued)
RXDETECT enables the types of messages and/or signaling to be detected. SOP* enabling also turns on auto−GoodCRC response. This register is reset when: A Hard Reset is received or sent; after the GoodCRC transmission due to RxOneMore; on a disconnect detection; SW_RST or POR.
Address: 2Fh
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Receive Detect Description (Note 35)
2	EN_SOP2	R/W	1	0b: Do not detect SOP” message (default) 1b: Detect SOP” message
1	EN_SOP1	R/W	1	0b: Do not detect SOP’ message (default) 1b: Detect SOP’ message
0	EN_SOP	R/W	1	0b: Do not detect SOP message (default) 1b: Detect SOP message

35. Writing all 0s to this register disables PD.

Table 53. RXBYTECNT
Address: 30h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Received Byte Count Description
7:0	RXBYTECNT	R	8	Number of Bytes Received. This is the number of bytes in RXDATA plus 3 (RXSTAT and RXHEADL, H)

Table 54. RXSTAT
This register indicates the status of the received SOP* message in RXHEADL,RXHEADH, and RXDATA registers.
Address: 31h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Receive Status Description
7:3	Reserved	R	5	Reserved: 00000b
2:0	RXSOP	R	3	Received SOP 000b: Received SOP 001b: Received SOP’ 010b: Received SOP” 011b: Received SOP’_DBG 100b: Received SOP”_DBG 110b: Received Cable Reset All others are reserved.

Table 55. RXHEADL
Received Header Low byte is stored here. Expected GoodCRC messages are not stored.
Address: 32h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Receive Header Low Description
7:0	RXHEADL	R	8	Rx Header Data Low

Table 56. RXHEADH

Received Header High byte is stored here. Expected GoodCRC messages are not stored.
Address: 33h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Receive Header High Description
7:0	RXHEADH	R	8	Rx Header Data High

Table 57. RXDATA

Address: 34h–4Fh
Reset Value: 0x00
Type: Read

Byte #	Name	R/W/C	Size (Bits)	Receive Payload Description
27:0	RXDATA0..27	R	8	Rx Payload

Table 58. TRANSMIT

Writing this register will start a PD transmission. If Cable Reset, Hard Reset or BIST Carrier Mode 2 is written, RETRY_CNT is ignored and signaling is not retried.
Address: 50h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Description
7:6	Reserved	R	2	Reserved: 00b
5:4	RETRY_CNT	R/W	2	Retry Counter 00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times
3	Reserved	R	1	Reserved: 0b
2:0	TXSOP	R/W	3	Transmit SOP Message 000b: Transmit SOP 001b: Transmit SOP’ 010b: Transmit SOP” 011b: Transmit SOP_DBG’ 100b: Transmit SOP_DBG” 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (Enabled for *tBISTContMode*)

Table 59. TXBYTECNT

Address: 51h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Byte Count Description
7:0	TXBYTECNT	R/W	8	Number of bytes to be transmitted

Table 60. TXHEADL

Address: 52h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Header Low Description
7:0	TXHEADL	R/W	8	Transmit Header Low

Table 61. TXHEADH
Address: 53h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Header High Description
7:0	TXHEADH	R/W	8	Transmit Header High

Table 62. TXDATA
Addresses: 54−6Fh
Reset Value: 0x00
Type: Read/Write

Byte #	Name	R/W/C	Size (Bits)	Transmit Payload Description
27:0	TXDATA0..27	R/W	8	Tx Payload

Table 63. VBUS_VOLTAGE_L
Address: 70h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	VBUS Voltage Low Description (Note 36)
7	VBUS_V_BIT7	R	1	Bit 7 of VBUS Measurement
6	VBUS_V_BIT6	R	1	Bit 6 of VBUS Measurement
5	VBUS_V_BIT5	R	1	Bit 5 of VBUS Measurement
4	VBUS_V_BIT4	R	1	Bit 4 of VBUS Measurement
3	VBUS_V_BIT3	R	1	Bit 3 of VBUS Measurement
2	VBUS_V_BIT2	R	1	Bit 2 of VBUS Measurement
1	VBUS_V_BIT1	R	1	Bit 1 of VBUS Measurement
0	VBUS_V_BIT0	R	1	Bit 0 of VBUS Measurement

36. TCPM must read VBUS_VOLTAGE_L before reading VBUS_VOLTAGE_H to guarantee ADC output and I^2C are properly synchronized.

Table 64. VBUS_VOLTAGE_H

Address: 71h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	VBUS Voltage High Description (Note 37)
7:4	Reserved	R	4	Reserved: 0000b
3:2	VBUS_SCALE	R	2	00b: VBUS Measurement not scaled 01b: VBUS Measurement divided by 2 10b: VBUS Measurement divided by 4 11b: Reserved
1	VBUS_V_BIT9	R	1	Bit 9 of VBUS Measurement
0	VBUS_V_BIT8	R	1	Bit 8 of VBUS Measurement

37. VBUS_V_BIT[9:0] is the measured VBUS voltage divided by VBUS_SCALE factor.

Table 65. VBUS_SNK_DISCL

Address: 72h
Reset Value: 0xA0 (< vSafe5V: 4.0 V)
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS SINK Disconnect Threshold Low (Note 36)
7:0	VBUS_SNK_DISC	R/W	8	Bits 7:0 of Sink Disconnect threshold

38. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

Table 66. VBUS_SNK_DISCH

Address: 73h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS SINK Disconnect Threshold High
7:2	Reserved	R	6	Reserved: 000000b
1:0	VBUS_SNK_DISC	R/W	2	Bits 9:8 of Sink Disconnect threshold

Table 67. VBUS_STOP_DISCL

Address: 74h
Reset Value: 0x1C (< vSafe0V: 700 mV)
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS Stop Discharge Threshold Low (Note 39)
7:0	VBUS_VTH_LO	R/W	8	Bits 7:0 of Stop Discharge threshold

39. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

Table 68. VBUS_STOP_DISCH

Address: 75h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS Stop Discharge Threshold High
7:2	Reserved	R	6	Reserved: 000000b
1:0	VBUS_VTH_LO	R/W	2	Bits 9:8 of Stop Discharge threshold

Table 69. VALARMHCFGL

Address: 76h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Voltage Alarm High Trip Point Configuration Low Description (Note 40)
7:0	VBUS_VTH_HI	R/W	8	Bits 7:0 of High trip point alarm

40. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

Table 70. VALARMHCFGH

Address: 77h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Voltage Alarm High Trip Point Configuration High Description
7:2	Reserved	R	6	Reserved: 000000b
1:0	VBUS_VTH_HI	R/W	2	Bits 9:8 of High trip point alarm

Table 71. VALARMLCFGL

Address: 78h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Voltage Alarm Low Trip Point Configuration Low Description (Note 41)
7:0	VBUS_VTH_LO	R/W	8	Bits 7:0 of Low trip point alarm

41. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

Table 72. VALARMLCFGH

Address: 79h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Voltage Alarm Low Trip Point Configuration High Description
7:2	Reserved	R	6	Reserved: 000000b
1:0	VBUS_VTH_LO	R/W	2	Bits 9:8 of Low trip point alarm

Table 73. VCONN_OCP
Address: A0h
Reset Value: 0x0F
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VCONN Current Limit Description (Note 42)
7:4		R	4	Reserved: 0b
3	OCP_RANGE	R/W	1	0b: OCP Range between 10 mA − 80 mA (max_range = 80 mA) 1b: OCP Range between 100 mA − 800 mA (max_range = 800 mA)
2:0	OCP_CUR	R/W	3	000b: max_range/8 001b: 2 × max_range/8 010b: 3 × max_range/8 011b: 4 × max_range/8 100b: 5 × max_range/8 101b: 6 × max_range/8 110b: 7 × max_range/8 111b: max_range (see OCP_RANGE definition above)

42. Only used if VCONN_OCP Register PWRCTRL.EN_VCONN is set to 1.

Table 74. RESET
Address: A2h
Reset Value: 0x00
Type: ReadW/Write (Self Clearing)

Bit #	Name	R/W/C	Size (Bits)	Reset Description
7:2	Reserved	R	6	Reserved:000000b
1	PD_RST	R/W	1	0b: No Action 1b: Reset PD−PHY and PD−FSMs
0	SW_RST	R/W	1	0b: No Action 1b: Reset all registers to default

Table 75. GPIO1_CFG
Address: A4h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	General Purpose I/O 1 Configuration
7:3	Reserved	R	5	Reserved:00000b
2	GPO1_VAL	R/W	1	If GPO1_EN = 1 0b: Set output = 0 1b: Set output = 1
1	GPI1_EN	R/W	1	0b: Input buffer disabled 1b: Input Buffer enabled (Input state can be read in GPIO_STAT Register)
0	GPO1_EN	R/W	1	0b: GPO is High−Z 1b: GPO is enabled

Table 76. GPIO2_CFG
Address: A5h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	General Purpose I/O 2 Configuration
7:4	Reserved	R	4	Reserved:0000b
3	FR_SWAP_FN	R/W	1	Enable Fast Role Swap I/O function for GPIO2 0b: FR_SWAP I/O function disabled 1b: FR_SWAP I/O function enabled
2	GPO2_VAL	R/W	1	Generic GPIO Function If GPO2_EN = 1 & FR_SWAP_FN = 0 0b: Set output = 0 1b: Set output = 1 Initial Hub Sink Fast Role Swap Function If GPO2_EN = 1 & FR_SWAP_FN = 1, Set GPO2_VAL = 1. When a VBUS disconnect is detected, the GPIO2 pin is automatically set low
1	GPI2_EN	R/W	1	Generic GPIO Function If FR_SWAP_FN = 0 0b: Input buffer disabled 1b: Input Buffer enabled (Input state can be read in GPIO_STAT Register) Initial Hub Source Fast Role Swap Function If FR_SWAP_FN = 1 & GPO2_EN = 0 0b: Input buffer disabled 1b: Monitor Input for a High to Low transition and initiate the Fast Role Swap within tTCPCSendFRSwap
0	GPO2_EN	R/W	1	0b: GPO is High−Z 1b: GPO is enabled

Table 77. GPIO_STAT
Address: A6h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	General Purpose I/O Input Status
7:2	Reserved	R	6	Reserved: 000000b
1	GPI2_VAL	R	1	If GPI2_EN 0b: GPIO2 Input is Low 1b: GPIO2 Input is High
0	GPI1_VAL	R	1	If GPI1_EN 0b: GPIO1 Input is Low 1b: GPIO1 Input is High

Table 78. DRPTOGGLE
Address: A7h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	DRP Toggle Timing
7:3	Reserved	R	6	Reserved:00000b
1:0	DRPTOGGLE	R/W	2	00b: tToggleSrc = 15 ms to 30 ms; tToggleSnk = 35 ms to 70 ms 01b: tToggleSrc = 20 ms to 40 ms; tToggleSnk = 30 ms to 60 ms 10b: tToggleSrc = 25 ms to 50 ms; tToggleSnk = 25 ms to 50 ms 11b: tToggleSrc = 30 ms to 60 ms; tToggleSnk = 20 ms to 40 ms

Table 79. SINK_TRANSMIT

Writing this register as a Sink will start a PD transmission when the Source Rp has transitioned from 1.5 A to 3.0 A. If Cable Reset, Hard Reset or BIST Carrier Mode 2 is written, RETRY_CNT is ignored and signaling is not retried.
After initial message transmission, the TCPM will monitor CCSTAT for changes in Rp.
Writing to this register as a Source is not allowed.
Address: B0h
Reset Value: 0x40
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Sink Transmit Description
7	Reserved	R	1	Reserved: 0b
6	DIS_SNK_TX	R/W	1	0b: Sink Transmit is enabled 1b: Sink Transmit is disabled
5:4	RETRY_CNT	R/W	2	Retry Counter 00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times
3	Reserved	R	1	Reserved: 0b
2:0	TXSOP	R/W	3	Transmit SOP Message 000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP" 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG" 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (Enabled for *tBISTContMode*)

Table 80. SRC_FRSWAP

Address: B1h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Source Fast Role Swap
7:4	Reserved	R	4	Reserved:0000b
3:2	FRSWAP_SNK_DELAY	R/W	2	If MANUAL_SNK_EN is set to 0, enable SNK gate after delay below: 00: 0 μs (Same time FR_SWAP bit is set). 01: 150 μs (After FR_SWAP signaling is complete) 10: 300 μs 11: 600 μs
1	MANUAL_SNK_EN	R/W	1	0b: Automatic SNK enable according to FRSWAP_SNK_DELAY 1b: SNK enabled by TCPM
0	FR_SWAP (Note 43)	R/WC	1	0b: No action 1b: Initiates Fast Role Swap process

43. Auto−Clear.

Table 81. SNK_FRSWAP

Address: B2h
Reset Value: 0x00
Type: Read/Write (Auto−Clear on detect)

Bit #	Name	R/W/C	Size (Bits)	Sink Fast Role Swap
7:1	Reserved	R	7	Reserved:000000b
0	EN_FRSWAP_DTCT (Note 44)	R/WC	1	0b: No action 1b: Enables Fast Role Swap detection

44. Auto−Clear on detect.

Table 82. ALERT_VD
Address: B3h
Reset Value: 0x00
Type: Read/Write 1 to clear

Bit #	Name	R/W/C	Size (Bits)	Vendor Defined Alert
7	Reserved	R	1	Reserved: 0b
6	I_DISCH_SUCC	R/WC	1	0b: No Interrupt 1b: Auto Discharge or Force Discharge Successful
5	I_GPI2	R/WC	1	0b: No Interrupt 1b: Input GPI2 change occurred
4	I_GPI1	R/WC	1	0b: No Interrupt 1b: Input GPI1 change occurred
3	I_VDD_DTCT	R/WC	1	0b: No Interrupt 1b: VDD detection change occurred (read VD_STAT)
2	I_OTP	R/WC	1	0b: No Interrupt 1b: OTP condition occurred
1	I_SWAP_TX	R/WC	1	0b: No Interrupt 1b: Fast role Swap sent due to GPIO input set low
0	I_SWAP_RX	R/WC	1	0b: No Interrupt 1b: Fast Role Swap request received

Table 83. ALERT_VD_MSK
Address: B4h
Reset Value: 0x7F
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Vendor Defined Alert Masks
7	Reserved	R	1	Reserved:0b
6	M_DISCH_SUCC	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
5	M_GPI2	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
4	M_GPI1	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
3	M_VDD_DTCT	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
2	M_OTP	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
1	M_SWAP_TX	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
0	M_SWAP_RX	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked

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ISSUE O

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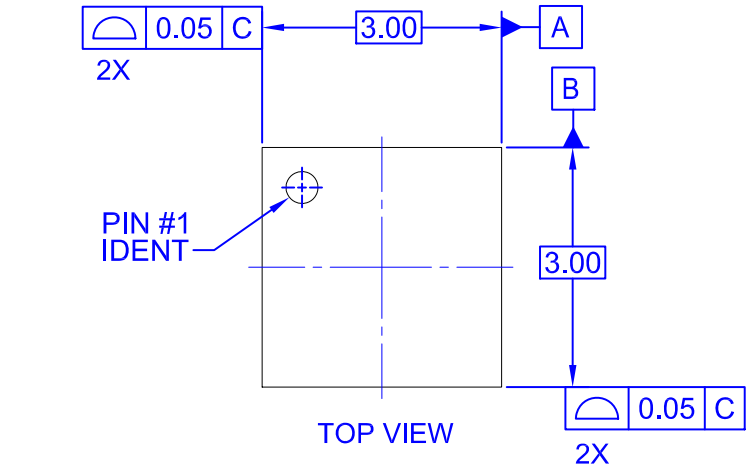

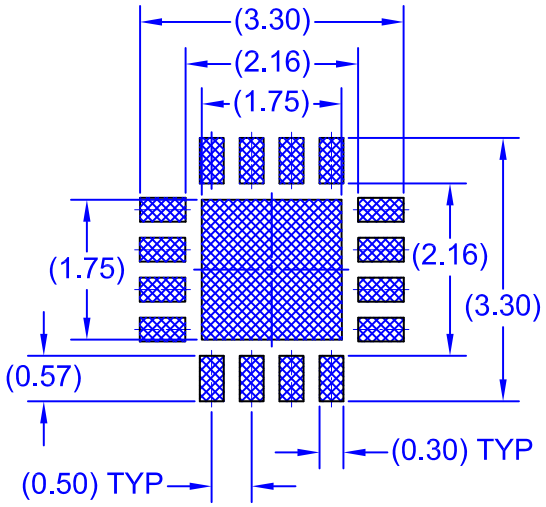

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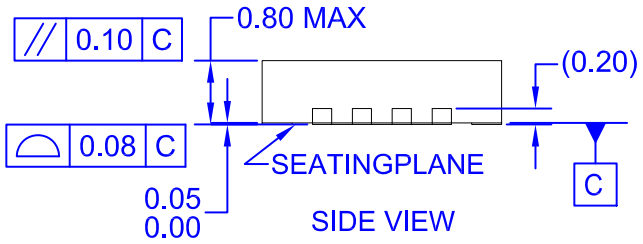
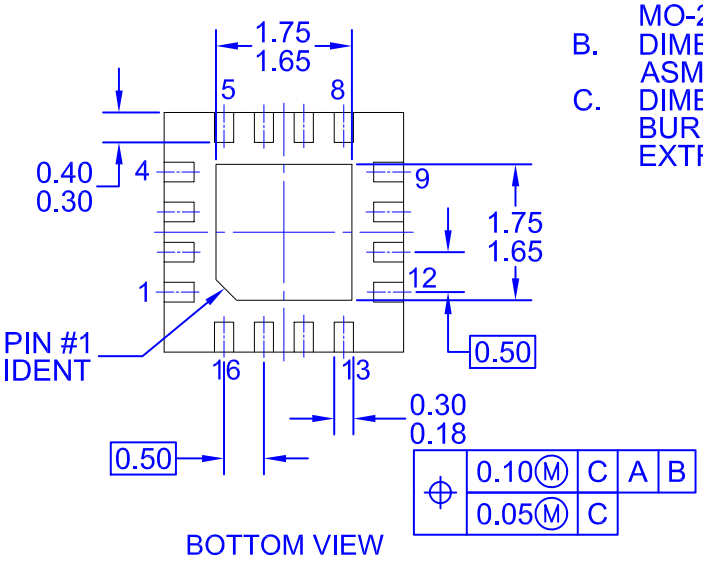


NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-220
B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



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