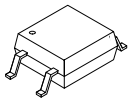
High Noise Immunity, 3.3V/5V, 10 Mbit/sec Logic Gate Output (Open Collector) Optocoupler

FODM8061



MFP5 4.1X4.4, 2.54P
CASE 100AM

Description

The FODM8061 is a 3.3 V/5 V high−speed logic gate output (open collector) optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes **onsemi**'s patented coplanar packaging technology, OPTOPLANAR®, and optimized IC design to achieve high noise immunity, characterized by high common mode transient immunity specifications.

This optocoupler consists of an AlGaAS LED at the input, optically coupled to a high speed integrated photo−detector logic gate. The output of the detector IC is an open collector schottky−clamped transistor. The coupled parameters are guaranteed over the wide temperature range of −40°C to +110°C. A maximum input signal of 5mA will provide a minimum output sink current of 13 mA (fan out of 8).

Features

- High Noise Immunity Characterized by Common Mode Transient Immunity (CMTI)
  - 20 kV/μs Minimum CMTI
- High Speed
  - 10 Mbit/sec Date Rate (NRZ)
  - 80 ns Max. Propagation Delay
  - 25 ns Max. Pulse Width Distortion
  - 40 ns Max. Propagation Delay Skew
- 3.3 V LVTTL/LVCMOS Compatibility
- Specifications Guaranteed over 3 V to 5.5 V Supply Voltage and −40°C to +110°C Temperature Range
- Safety and Regulatory Approvals
  - UL1577, 3750 VAC_{RMS} for 1 min.
  - DIN EN/IEC60747−5−5

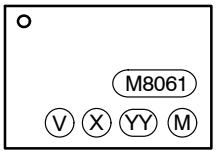
Applications

- Microprocessor System Interface
  - SPI, I^2C
- Industrial Fieldbus Communications
  - DeviceNet, CAN, RS485
- Programmable Logic Control
- Isolated Data Acquisition System
- Voltage Level Translator
- Isolating MOSFET/IGBT Gate Drivers

Related resources

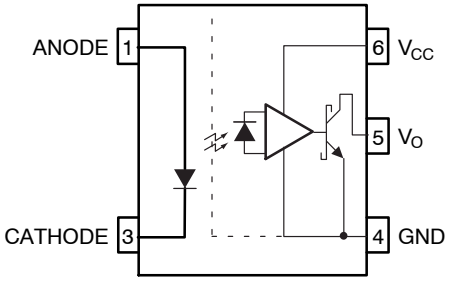
www.onsemi.com/products
www.onsemi.com/FODM611
www.onsemi.com/FODM8071

MARKING DIAGRAM



M8061 = Device Number
V = DIN EN/IEC60747−5−5 Option (Note: Only Appears on Parts Ordered with This Option)
X = One Digit Year Code, e.g., '9'
YY = Two Digit Work Week Ranging from '01' to '53'
M = Assembly Package Code

FUNCTIONAL SCHEMATIC



TRUTH TABLE

LED	Output
Off	High
On	Low

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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PIN DEFINITIONS

Number	Name	Function Description
1	ANODE	Anode
3	CATHODE	Cathode
4	GND	Output Ground
5	V_O	Output Voltage
6	V_{CC}	Output Supply Voltage

SAFETY AND INSULATION RATINGS FOR MINI−FLAT PACKAGE (SO5 PIN)

(As per IEC60747−5−5. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Symbol	Parameter	Min	Typ	Max	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1	–	–	–	
	For Rated Main Voltage <150 Vrms	–	I−IV	–	
	For Rated Main Voltage <300 Vrms	–	I−III	–	
	Climatic Classification	–	40/110/21	–	
	Pollution Degree (DIN VDE 0110/1.89)	–	2	–	
CTI	Comparative Tracking Index	175	–	–	
V_{PR}	Input to Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge <5 pC	1060	–	–	
V_{PR}	Input to Output Test Voltage, Method a, V_{IORM} x 1.5 = V_{PR}, Type and Sample Test with t_m = 60 s, Partial Discharge <5 pC	848	–	–	
V_{IORM}	Max Working Insulation Voltage	565	–	–	V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	4000	–	–	V_{peak}
	External Creepage	5.0	–	–	mm
	External Clearance	5.0	–	–	mm
	Insulation Thickness	0.5	–	–	mm
T_{Case}	Safety Limit Values, Maximum Values Allowed in the Event of a Failure, Case Temperature	150	–	–	°C
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9	–	–	Ω

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +110	°C
T_J	Junction Temperature	−40 to +125	°C
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 s	°C
I_F	Forward Current	50	mA
V_R	Reverse Voltage	5.0	V
V_{CC}	Supply Voltage	0 to 7.0	V
V_O	Output Voltage	−0.5 to V_{CC}+0.5	V
I_O	Average Output Current	50	mA
PD_I	Input Power Dissipation (Note 1), (Note 2)	100	mW
PD_O	Output Power Dissipation (Note 1), (Note 2)	85	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. No derate required to 110°C.
2. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	−40	+110	°C
V_{CC}, V_{DD}	Supply Voltages (Note 3)	3.0	5.5	V
V_{FL}	Logic Low Input Voltage	0	0.8	V
I_{FH}	Logic High Input Current (Note 4)	6.3	15	mA
I_{FL}	Logic Low Input Current	–	250	μA
N	Fan Out (at R_L = 1 kΩ)	–	5	TTL Loads
R_L	Output Pull−up Resistor	330	4k	Ω

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. 0.1 μF bypass capacitor must be connected between pins 4 and 6.
4. Recommended I_{FH} is 9.3 mA for operation above T_A =100°C.

ISOLATION CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{ISO}	Input−Output Isolation Voltage	f = 60 Hz, t = 1.0 min, $I_{I-O} \le$ 10 μA (Note 5), (Note 6)	3750	–	–	VAC_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 5)	–	10^{12}	–	Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V f = 1.0 Mhz (Note 5)	–	0.6	–	pF

5. Device is considered a two terminal device: Pins 1 and 3 are shorted, and Pins 4, 5, and 6 are shorted together.
6. 3,750 VAC_{RMS} for 1 minute duration is equivalent to 4,500 VAC_{RMS} for 1 second duration.

ELECTRICAL CHARACTERISTICS (Apply over all recommended conditions)
(T_A = −40°C to +110°C, 3.0 V ≤ V_{CC} ≤ 5.5 V, unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ*	Max	Unit
INPUT CHARACTERISTICS							
V_F	Forward Voltage	I_F = 10 mA (Figure 1)		1.05	1.45	1.8	V
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA		5.0	–	–	V
I_{FHL}	Threshold Input Current	V_O = 0.6 V, I_{OL} (sinking) = 13 mA	T_A < 85°C, (Figure 2)	–	3.4	5.0	mA
			T_A = 85°C to 110 °C	–	4.2	7.5	
OUTPUT CHARACTERISTICS							
V_{OL}	Logic LOW Output Voltage	I_F = rated I_{FHL}, I_{OL} (sinking) = 13 mA (Figure 3)		–	0.4	0.6	V
I_{OH}	Logic HIGH Output Current	I_F = 250 μA, V_O = 3.3 V, (Figure 4)		–	8.0	50.0	μA
		I_F = 250 μA, V_O = 5.0 V, (Figure 4)		–	2.1	30.0	μA
I_{CCL}	Logic LOW Output Supply Current	I_F = 10 mA, V_{CC} = 3.3 V, (Figure 5), (Figure 7)		–	6.0	8.5	mA
		I_F = 10 mA, V_{CC} = 5.0 V, (Figure 5), (Figure 7)		–	7.5	10.0	mA
I_{CCH}	Logic HIGH Output Supply Current	I_F = 0 mA, V_{CC} = 3.3 V, (Figure 6), (Figure 7)		–	4.0	7.0	mA
		I_F = 0 mA, V_{CC} = 5.0 V, (Figure 6), (Figure 7)		–	6.0	9.0	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Typical value is measured at T_A = 25°C and V_{CC} = 3.3 V.

SWITCHING CHARACTERISTICS (Apply over all recommended conditions)
(T_A = −40°C to +110°C, 3.0 V ≤ V_{CC} ≤ 5.5 V, I_F = 7.5 mA, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ*	Max	Unit
Date Rate		R_L = 350 Ω	–	–	10	Mbps
t_{PHL}	Propagation Delay Time to Logic Low Output	R_L = 350 Ω, C_L = 15 pF, (Figure 8), (Figure 11)	–	43	80	ns
t_{PLH}	Propagation Delay Time to Logic High Output	R_L = 350 Ω, C_L = 15 pF, (Figure 8), (Figure 11)	–	50	80	ns
PWD	Pulse Width Distortion, $\|t_{PHL} - t_{PLH}\|$	R_L = 350 Ω, C_L = 15 pF, (Figure 9)	–	7	25	ns
t_{PSK}	Propagation Delay Skew	R_L = 350 Ω, C_L = 15 pF, (Note 7)	–	–	40	ns
t_R	Output Rise Time, (10% to 90%)	R_L = 350 Ω, C_L = 15 pF, (Figure 10), (Figure 11)	–	20	–	ns
t_F	Output Fall Time, (90% to 10%)	R_L = 350 Ω, C_L = 15 pF, (Figure 10), (Figure 11)	–	10	–	ns
$\|CM_H\|$	Common Mode Transient Immunity at Output High	I_F = 0 mA, V_O > 0.8 x V_{CC}, V_{CM} = 1000 V (Note 8), (Figure 12)	20	40	–	kV/μs
$\|CM_L\|$	Common Mode Transient Immunity at Output Low	I_F = 7.5 mA, V_O < 0.8 V, V_{CM} = 1000 V (Note 8), (Figure 12)	20	40	–	kV/μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Typical value is measured at T_A = 25°C and V_{CC} = 3.3 V.

7. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between any two units from the same manufacturing date code that are operated at same case temperature (±5°C), at same operating conditions, with equal loads (R_L = 350 Ω and C_L = 15 pF), and with an input rise time less than 5 ns.
8. Common mode transient immunity at output high is the maximum tolerable positive dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative dVcm/dt on the trailing edge of the common pulse signal, Vcm, to assure that the output will remain low.

TYPICAL PERFORMANCE CURVES

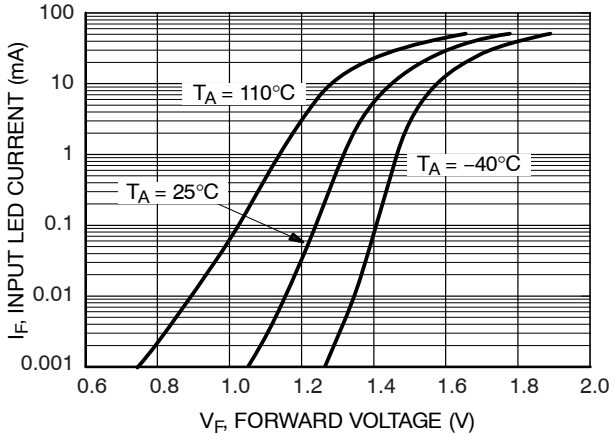


Figure 1. Input LED Current vs. Forward Voltage

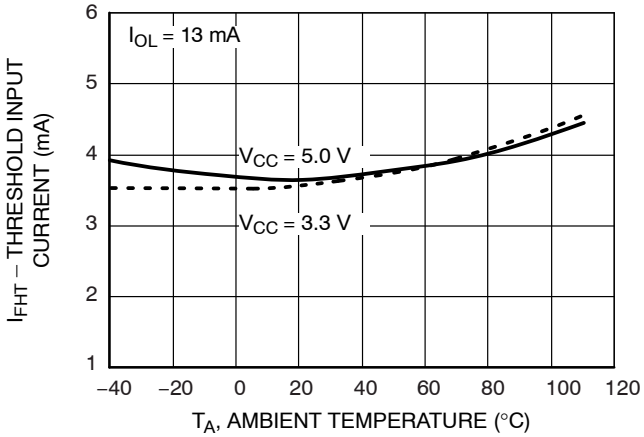


Figure 2. Threshold Input Current vs. Ambient Temperature

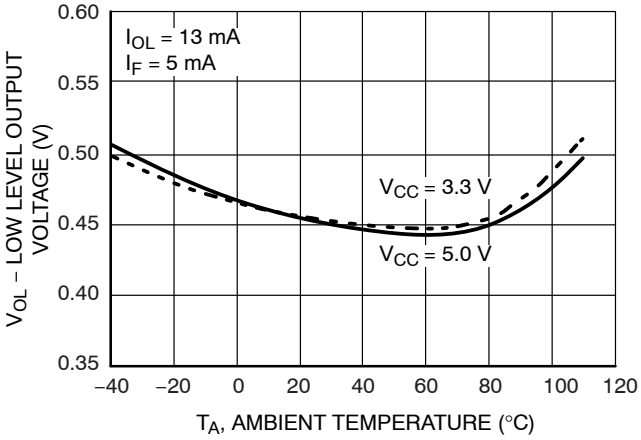


Figure 3. Low Level Output Voltage vs. Ambient Temperature

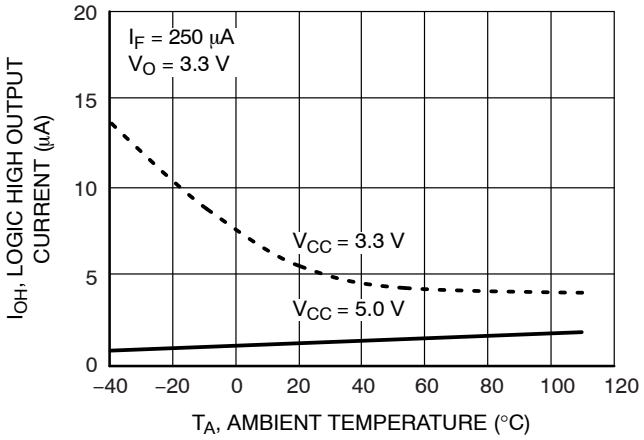


Figure 4. Logic High Output Current vs. Ambient Temperature

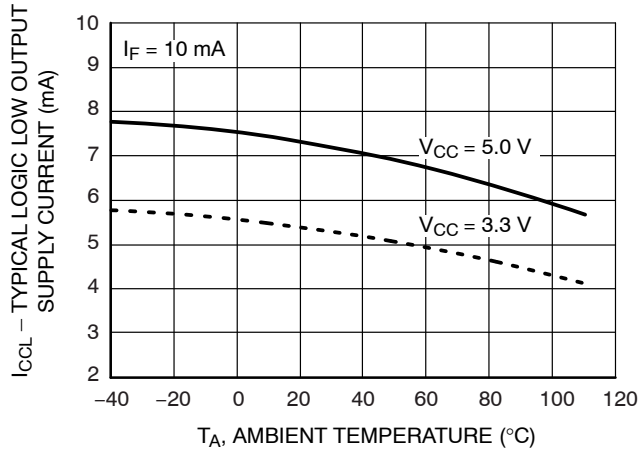


Figure 5. Typical Logic Low Output Supply Current vs. Ambient Temperature

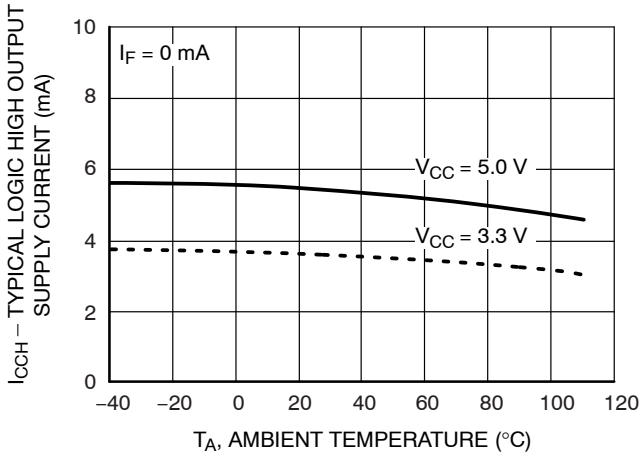


Figure 6. Typical Logic High Output Supply Current vs. Ambient Temperature

TYPICAL PERFORMANCE CURVES (CONTINUED)

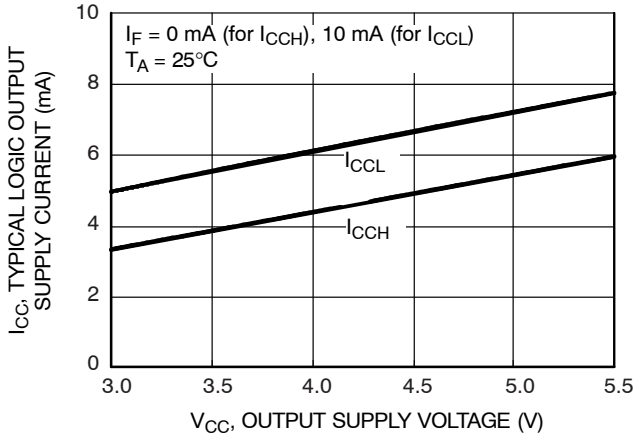


Figure 7. Typical Logic Output Supply Current vs. Output Supply Voltage

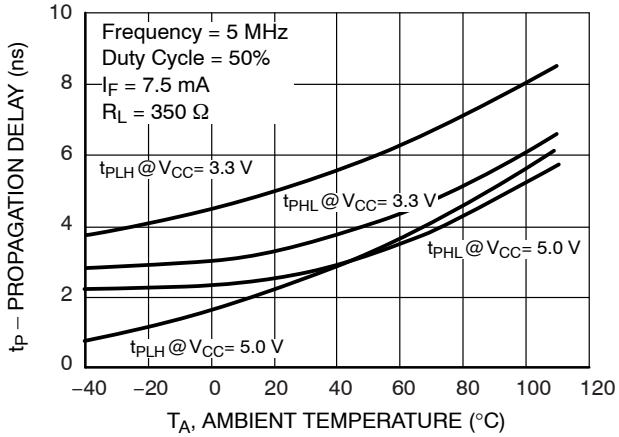


Figure 8. Typical Propagation Delay vs. Ambient Temperature

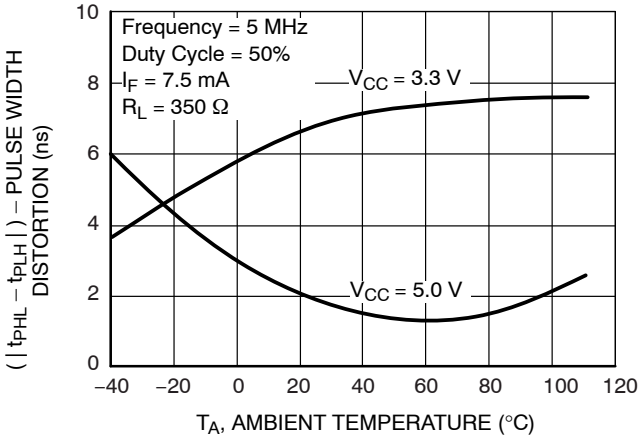


Figure 9. Typical Pulse Width Distortion vs. Ambient Temperature

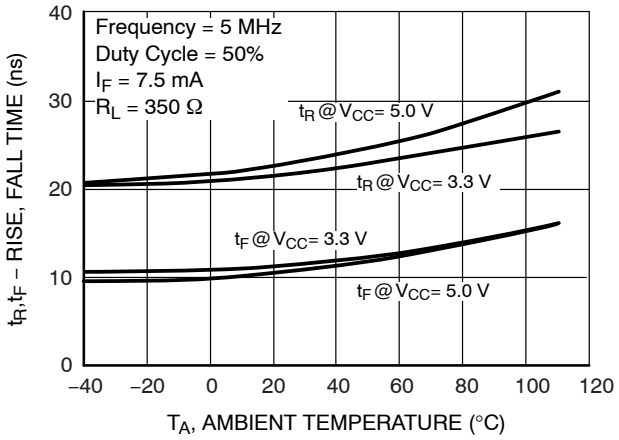


Figure 10. Typical Rise and Fall Time vs. Ambient Temperature

SCHEMATICS

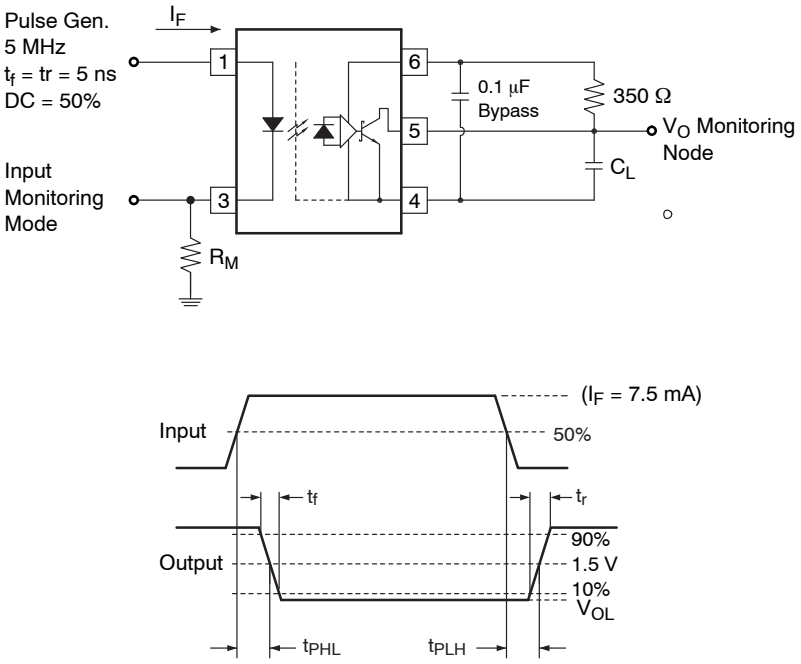


Figure 11. Test Circuit for Propagation Delay Time, Rise Time and Fall Time

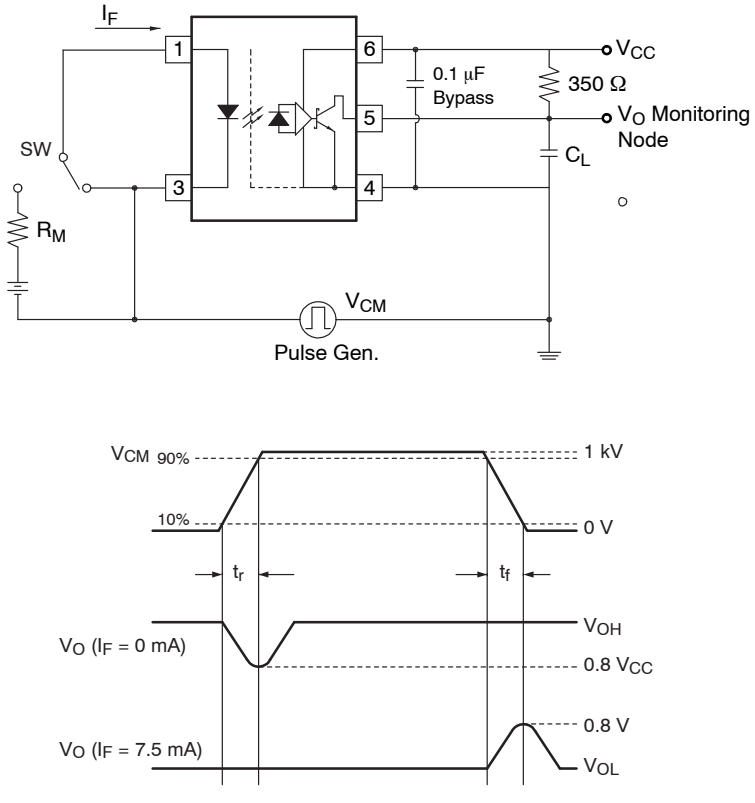


Figure 12. Test Circuit for Instantaneous Common Mode Rejection Voltage

REFLOW PROFILE

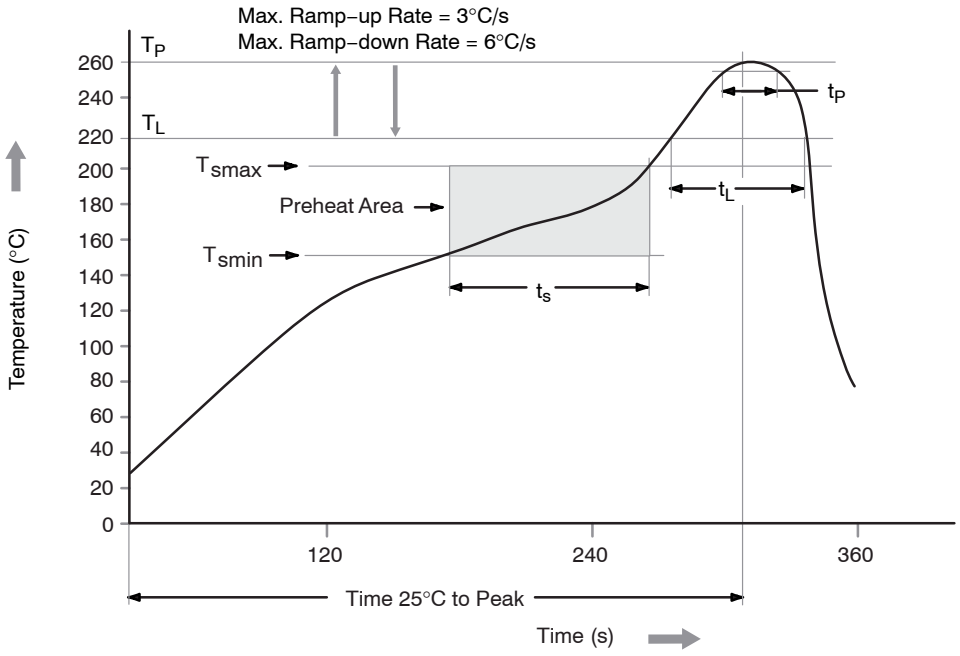


Figure 13. Reflow Profile

Table 1. REFLOW PROFILE

Profile Feature	Pb−Free Assembly Profile
Temperature Minimum (T_{smin})	150°C
Temperature Maximum (T_{smax})	200°C
Time (t_S) from (T_{smin} to T_{smax})	60 – 120 seconds
Ramp−up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 – 150 seconds
Peak Body Package Temperature	260°C +0°C / −5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp−down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

ORDERING INFORMATION

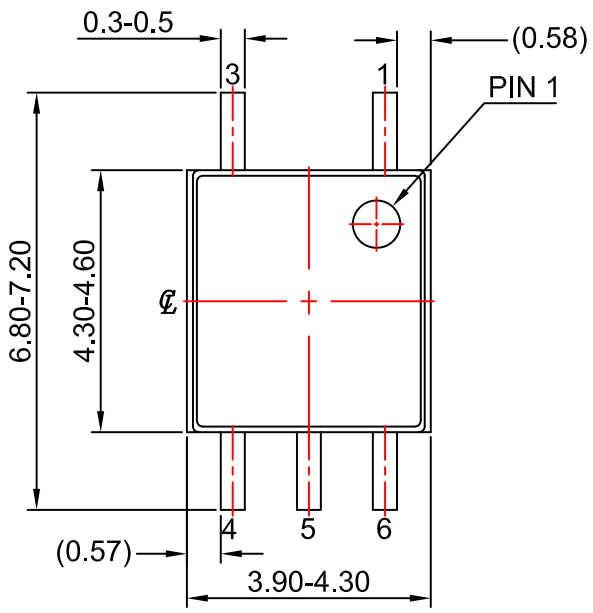
Part Number	Package	Shipping†
FODM8061	MFP5 4.1X4.4, 2.54P (Pb−Free)	100 Units / Tube
FODM8061R2	MFP5 4.1X4.4, 2.54P (Pb−Free)	2500 / Tape & Reel
FODM8061V	MFP5 4.1X4.4, 2.54P IEC60747−5−5 (Pb−Free)	100 Units / Tube
FODM8061R2V	MFP5 4.1X4.4, 2.54P IEC60747−5−5 (Pb−Free)	2500 / Tape & Reel

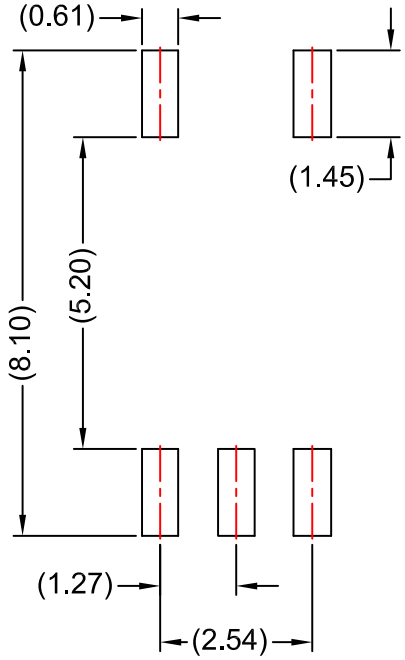
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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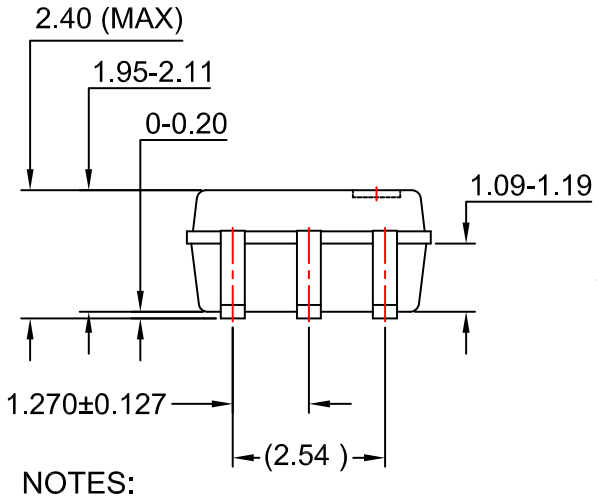
MFP5 4.1X4.4, 2.54P
CASE 100AM
ISSUE O

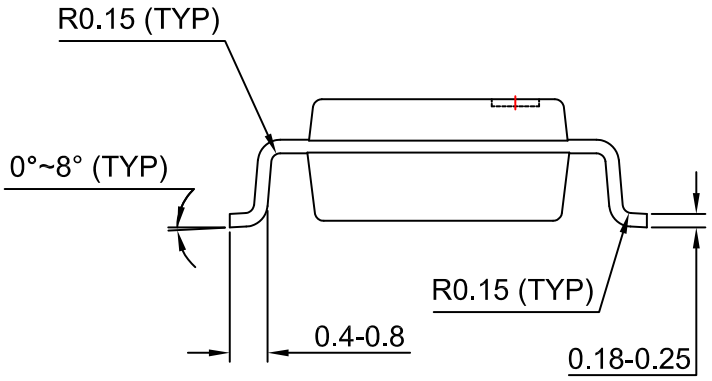
DATE 31 AUG 2016





LAND PATTERN RECOMMENDATION





NOTES:

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