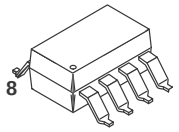
Gate Drive Optocoupler, High Noise Immunity, 1.0 A Output Current

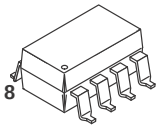
FOD3150

ON Semiconductor®

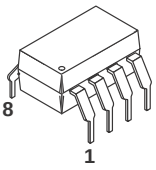
www.onsemi.com



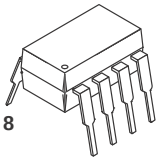
PDIP8 GW
CASE 709AD



PDIP8 GW
CASE 709AC



PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.6, 2.54P
CASE 646CQ

Description

The FOD3150 is a 1.0 A Output Current Gate Drive Optocoupler, capable of driving most 800 V / 20 A IGBT / MOSFET. It is ideally suited for fast switching driving of power IGBT and MOSFETs used in motor control inverter applications, and high performance power system.

It utilizes ON Semiconductor patented coplanar packaging technology, Optoplanar®, and optimized IC design to achieve high noise immunity, characterized by high common mode rejection.

It consists of a gallium aluminum arsenide (AlGaAs) light emitting diode optically coupled to an integrated circuit with a high−speed driver for push−pull MOSFET output stage.

Features

- High Noise Immunity characterized by 20 kV/μs minimum Common Mode Rejection
- Use of P−channel MOSFETs at Output Stage Enables Output Voltage Swing close to the Supply Rail
- Wide Supply Voltage Range from 15 V to 30 V
- Fast Switching Speed
  - 500 ns maximum Propagation Delay
  - 300 ns maximum Pulse Width Distortion
- Under Voltage LockOut (UVLO) with Hysteresis
- Extended Industrial Temperate Range, −40°C to 100°C Temperature Range
- Safety and Regulatory Approvals
  - UL1577, 5000 V_{RMS} for 1 minute
  - DIN EN/IEC60747−5−5
- >8.0 mm Clearance and Creepage Distance (Option ‘T’)
- This is a Pb−Free Device

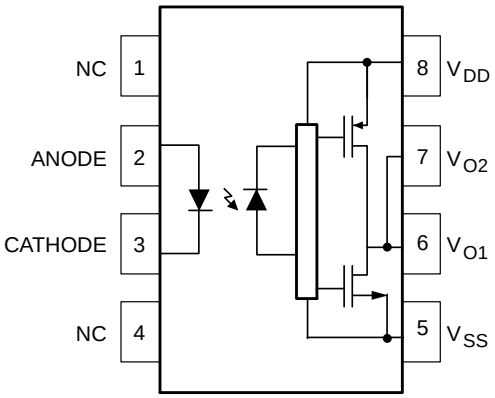
Applications

- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

Related Resources

- FOD3120, 2.5 A Output Current, Gate Drive Optocoupler Datasheet
- www.onsemi.com/products/opto/

FUNCTIONAL BLOCK DIAGRAM



Note: A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

© Semiconductor Components Industries, LLC, 2018

Table 1. TRUTH TABLE

LED	V_{DD} – V_{SS} "Positive Going" (Turn−on)	V_{DD} – V_{SS} "Negative Going" (Turn−off)	V_O
Off	0 V to 30 V	0 V to 30 V	Low
On	0 V to 11 V	0 V to 9.7 V	Low
On	11 V to 14 V	9.7 V to 12.7 V	Transition
On	14 V to 30 V	12.7 V to 30 V	High

Table 2. PIN DEFINITIONS

Pin #	Name	Description
1	NC	Not Connected
2	Anode	LED Anode
3	Cathode	LED Cathode
4	NC	Not Connected
5	V_{SS}	Negative Supply Voltage
6	V_{O2}	Output Voltage 2 (internally connected to V_{O1})
7	V_{O1}	Output Voltage 1
8	V_{DD}	Positive Supply Voltage

Table 3. SAFETY AND INSULATION RATINGS

As per IEC 60747−5−2. This optocoupler is suitable for "safe electrical insulation" only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 For Rated Main Voltage < 150 Vrms		I–IV		
	For Rated Main Voltage < 300 Vrms		I–IV		
	For Rated Main Voltage < 450 Vrms		I–III		
	For Rated Main Voltage < 600 Vrms		I–III		
	Climatic Classification		55/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V_{PR}	Input to Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with tm = 1 s, Partial Discharge < 5 pC	1669			
	Input to Output Test Voltage, Method a, V_{IORM} x 1.5 = V_{PR}, Type and Sample Test with tm = 60 s, Partial Discharge < 5 pC	1335			
V_{IORM}	Max Working Insulation Voltage	890			Vpeak
V_{IOTM}	Highest Allowable Over Voltage	6000			Vpeak
	External Creepage	8			mm
	External Clearance	7.4			mm
	External Clearance (for Option T−0.4" Lead Spacing)	10.16			mm
	Insulation Thickness	0.5			mm
T_{Case}	Safety Limit Values – Maximum Values Allowed in the Event of a Failure Case Temperature	150			°C
$I_{S,INPUT}$	Input Current	25			mA
$P_{S,OUTPUT}$	Output Power (Duty Factor ≤ 2.7 %)	250			mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9			Ω

Table 4. ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	−55 to +125	°C
T_{OPR}	Operating Temperature	−40 to +100	°C
T_J	Junction Temperature	−40 to +125	°C
T_{SOL}	Lead Wave Solder Temperature (refer to page 12 for reflow solder profile)	260 for 10 sec	°C
$I_{F(AVG)}$	Average Input Current	25	mA
V_R	Reverse Input Voltage	5	V
$I_{O(PEAK)}$	Peak Output Current (1)	1.5	A
$V_{DD} – V_{SS}$	Supply Voltage	0 to 35	V
$V_{O(PEAK)}$	Peak Output Voltage	0 to V_{DD}	V
$t_{R(IN)}$, $t_{F(IN)}$	Input Signal Rise and Fall Time	500	ns
PD_I	Input Power Dissipation (2) (4)	45	mW
PD_O	Output Power Dissipation (3) (4)	250	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum pulse width = 10 μs, maximum duty cycle = 0.2 %.
2. Derate linearly above 87°C, free air temperature at a rate of 0.77 mW/°C.
3. No derating required across temperature range.
4. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Units
T_A	Ambient Operating Temperature	−40 to +100	°C
$V_{DD} – V_{SS}$	Power Supply	15 to 30	V
$I_{F(ON)}$	Input Current (ON)	7 to 16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	0 to 0.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ISOLATION CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at T_A = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input−Output Isolation Voltage	T_A = 25°C, R.H.< 50 %, t = 1.0 minute, $I_{I–O} \le 10$ μA, 50 Hz (5) (6)	5000			V_{RMS}
R_{ISO}	Isolation Resistance	$V_{I–O}$ = 500 V (5)		10^{11}		Ω
C_{ISO}	Isolation Capacitance	$V_{I–O}$ = 0 V, Frequency = 1.0 MHz (5)		1		pF

5. Device is considered a two terminal device: pins 2 and 3 are shorted together and pins 5, 6, 7 and 8 are shorted together.
6. 5,000 V_{RMS} for 1 minute duration is equivalent to 6,000 VAC_{RMS} for 1 second duration.

Table 7. ELECTRICAL CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_F	Input Forward Voltage	I_F = 10 mA	1.2	1.5	1.8	V
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage			−1.8		mV/°C
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA	5			V

Table 7. ELECTRICAL CHARACTERISTICS (continued)
Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V		60		pF
I_{OH}	High Level Output Current (7)	$V_O = V_{DD} - 0.75$ V	0.2			A
		$V_O = V_{DD} - 4$ V	1.0			
I_{OL}	Low Level Output Current (7)	$V_O = V_{DD} + 0.75$ V	0.2			A
		$V_O = V_{DD} + 4$ V	1.0			
V_{OH}	High Level Output Voltage	I_F = 10 mA, I_O = −1 A	$V_{DD} - 6$ V	$V_{DD} - 4$ V		V
		I_F = 10 mA, I_O = −100 mA	$V_{DD} - 0.5$ V	$V_{DD} - 0.1$ V		
V_{OL}	Low Level Output Voltage	I_F = 0 mA, I_O = 1 A		$V_{SS} + 4$ V	$V_{SS} + 6$ V	V
		I_F = 0 mA, I_O = 100 mA		$V_{SS} + 0.1$ V	$V_{SS} + 0.5$ V	
I_{DDH}	High Level Supply Current	V_O = Open, I_F = 7 to 16 mA		2.8	5	mA
I_{DDL}	Low Level Supply Current	V_O = Open, V_F = 0 to 0.8 V		2.8	5	mA
I_{FLH}	Threshold Input Current Low to High	I_O = 0 mA, V_O > 5 V		2.3	5.0	mA
V_{FHL}	Threshold Input Voltage High to Low	I_O = 0 mA, V_O < 5 V	0.8			V
V_{UVLO+}	Under Voltage Lockout Threshold	I_F = 1 0mA, V_O > 5 V	11	12.7	14	V
V_{UVLO-}		I_F = 10 mA, V_O < 5 V	9.7	11.2	12.7	V
$UVLO_{HYS}$	Under Voltage Lockout Threshold Hysteresis			1.5		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
7. Maximum pulse width = 10 μs, maximum duty cycle = 0.2 %.

Table 8. SWITCHING CHARACTERISTICS
Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Propagation Delay Time to Logic Low Output	I_F = 7 mA to 16 mA, Rg = 20 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50 %	100	275	500	ns
t_{PLH}	Propagation Delay Time to Logic High Output		100	255	500	ns
PWD	Pulse Width Distortion, | $t_{PHL} - t_{PLH}$ |			20	300	ns
PDD (Skew)	Propagation Delay Difference Between Any Two Parts or Channels, ($t_{PHL} - t_{PLH}$) (8)		−350		350	ns
t_r	Output Rise Time (10% – 90%)			60		ns
t_f	Output Fall Time (90% – 10%)			60		ns
$t_{UVLO\ ON}$	UVLO Turn On Delay	I_F = 10 mA , V_O > 5 V		1.6		μs
$t_{UVLO\ OFF}$	UVLO Turn Off Delay	I_F = 10 mA , V_O < 5 V		0.4		μs
| CM_H |	Common Mode Transient Immunity at Output High	T_A = 25°C, V_{DD} = 30 V, I_F = 7 to 16 mA, V_{CM} = 2000 V (9)	20	50		kV/μs
| CM_L |	Common Mode Transient Immunity at Output Low	T_A = 25°C, V_{DD} = 30 V, V_F = 0 V, V_{CM} = 2000 V (10)	20	50		kV/μs

8. The difference between t_{PHL} and t_{PLH} between any two FOD3150 parts under same test conditions.
9. Common mode transient immunity at output high is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, Vcm, to assure that the output will remain high (i.e., V_O > 15.0 V).
10. Common mode transient immunity at output low is the maximum tolerable positive dVcm/dt on the leading edge of the common pulse signal, Vcm, to assure that the output will remain low (i.e., V_O < 1.0 V).

TYPICAL PERFORMANCE CURVES

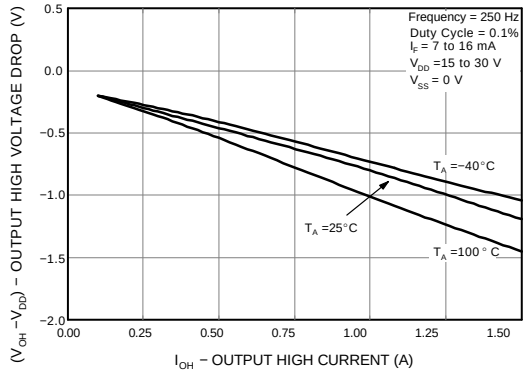


Figure 1. Output High Voltage Drop vs. Output High Current

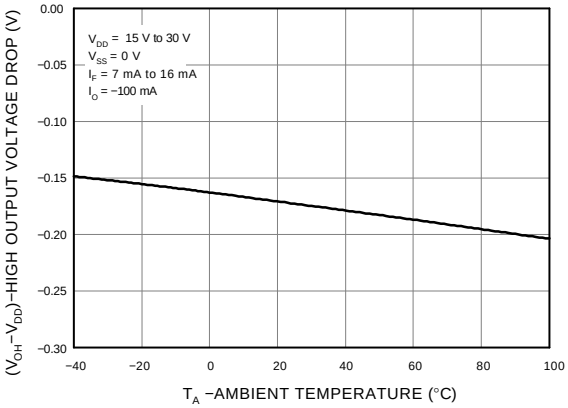


Figure 2. Output High Voltage Drop vs. Ambient Temperature

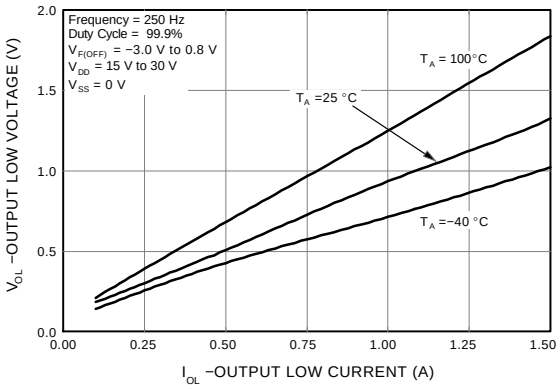


Figure 3. Output Low Voltage vs. Output Low Current

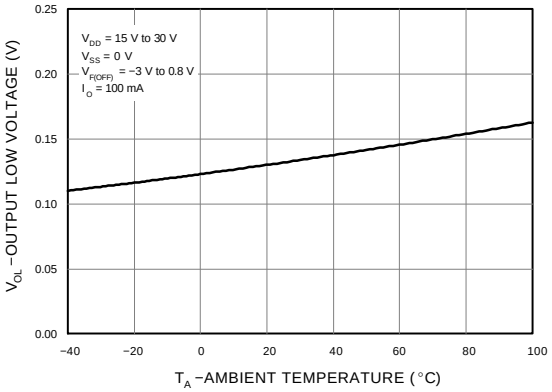


Figure 4. Output Low Voltage vs. Ambient Temperature

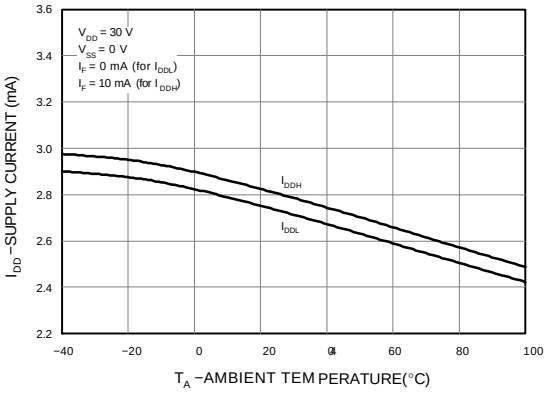


Figure 5. Supply Current vs. Ambient Temperature

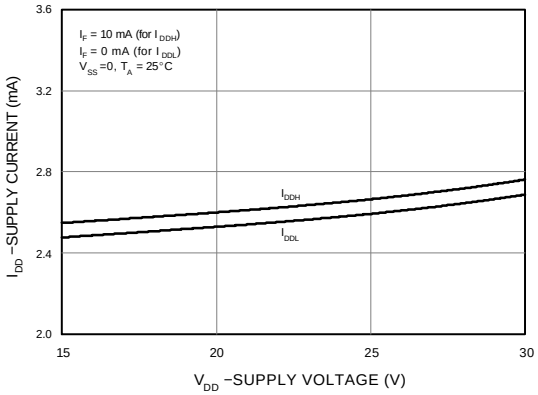


Figure 6. Supply Current vs. Supply Voltage

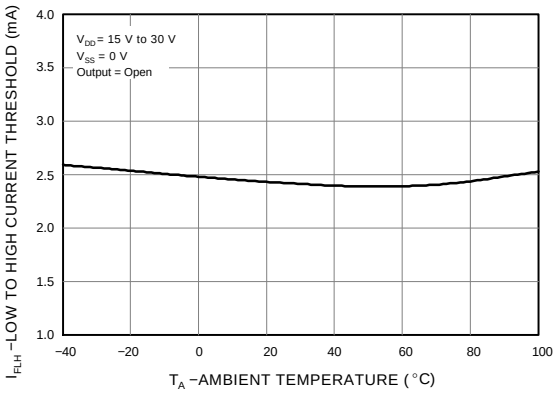


Figure 7. Low to High Input Current Threshold vs. Ambient Temperature

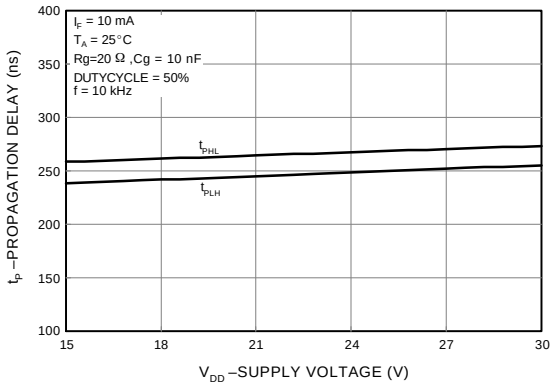


Figure 8. Propagation Delay vs. Supply Voltage

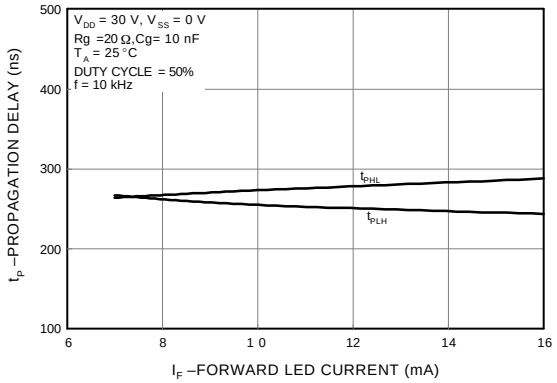


Figure 9. Propagation Delay vs. LED Forward Current

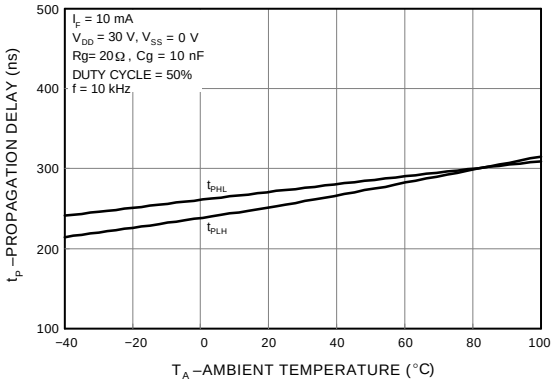


Figure 10. Propagation Delay vs. Ambient Temperature

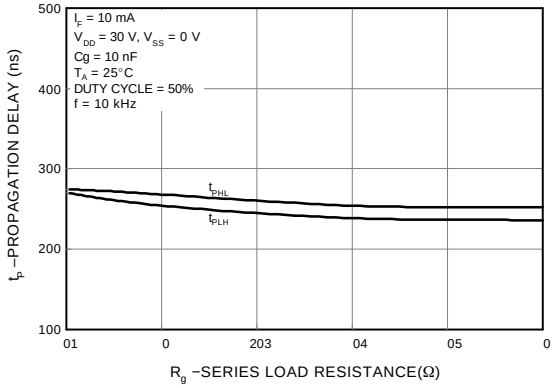


Figure 11. Propagation Delay vs. Series Load Resistance

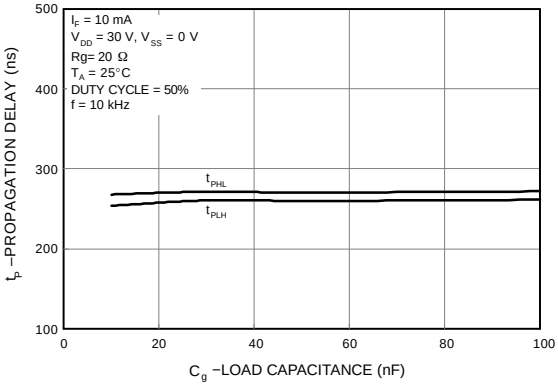


Figure 12. Propagation Delay vs. Load Capacitance

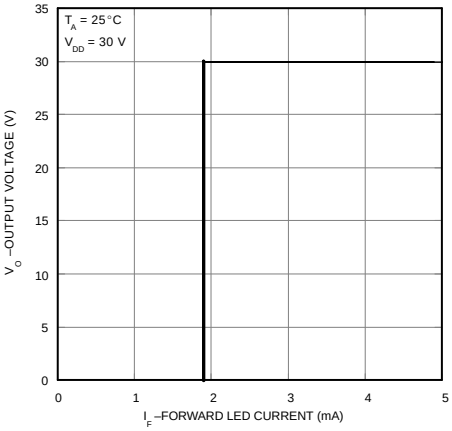


Figure 13. Transfer Characteristics

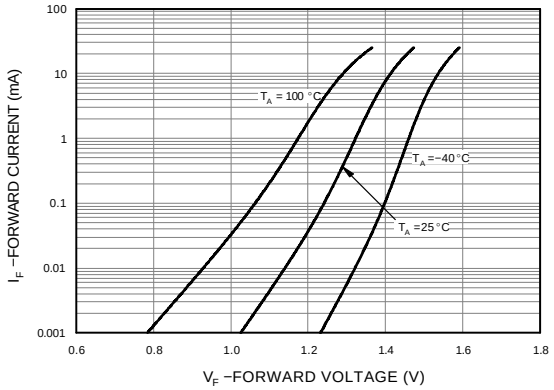


Figure 14. Input Forward Current vs. Forward Voltage

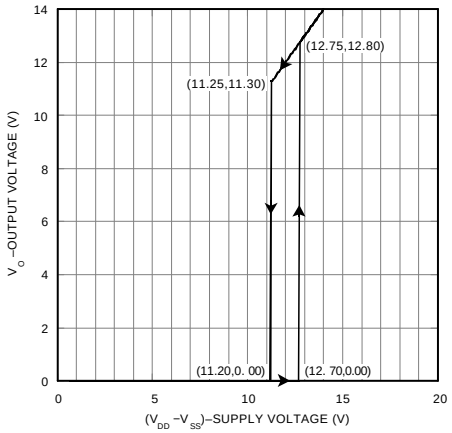


Figure 15. Under Voltage Lockout

TEST CIRCUIT

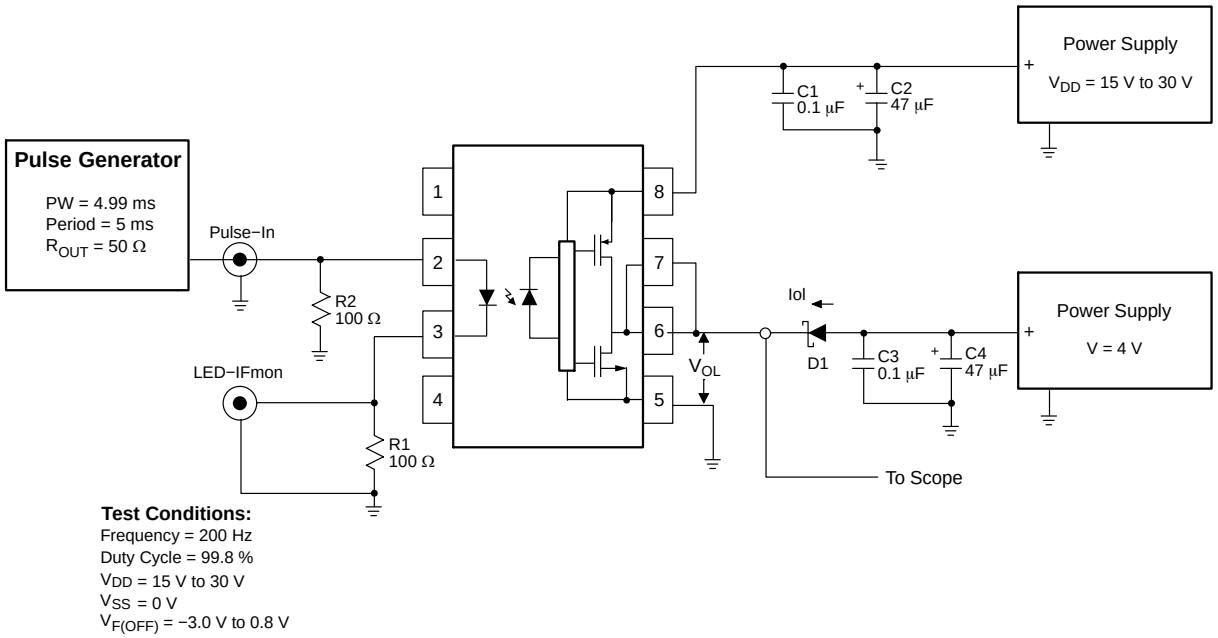


Figure 16. I_{OL} Test Circuit

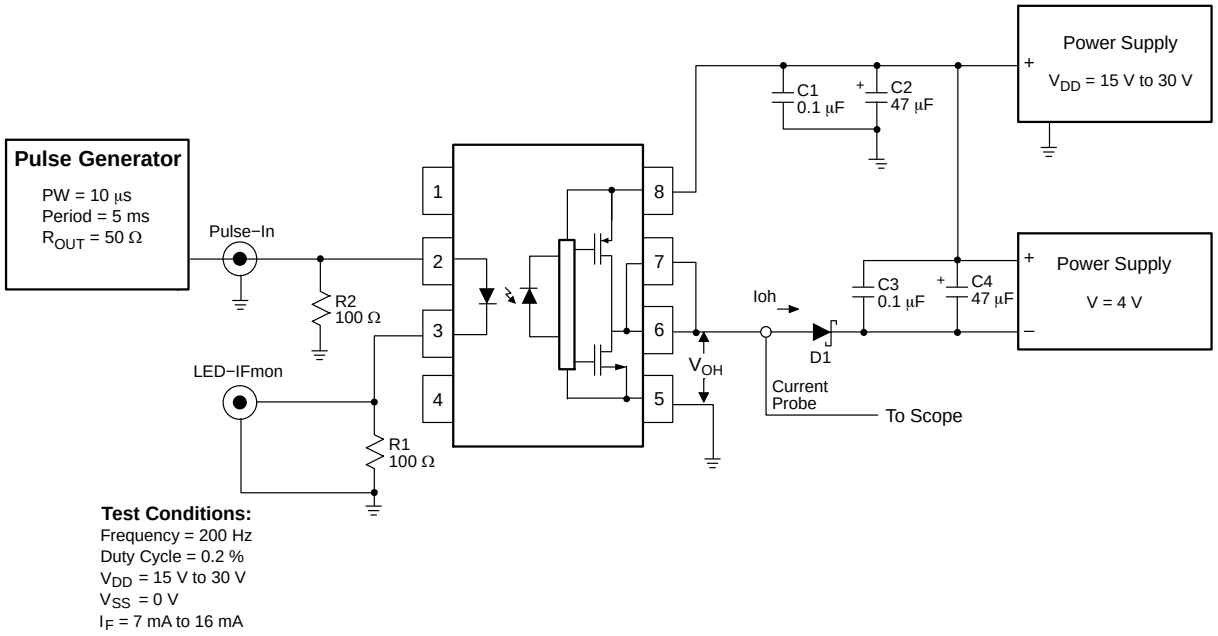


Figure 17. I_{OH} Test Circuit

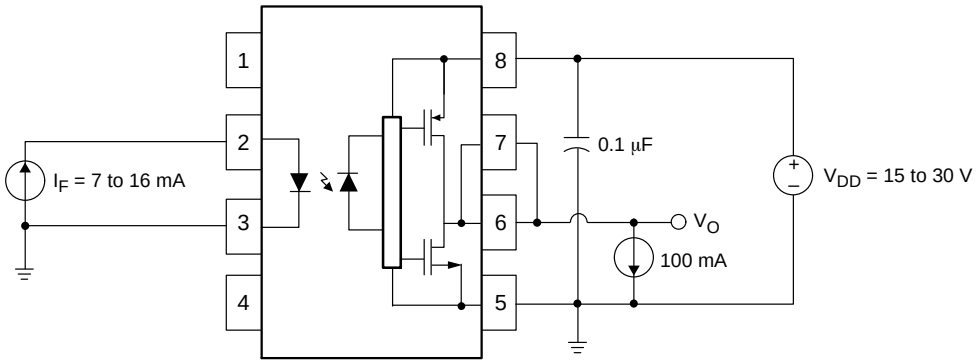


Figure 18. V_{OH} Test Circuit

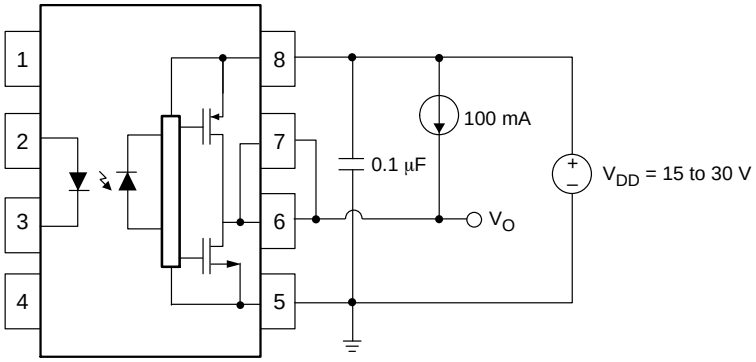


Figure 19. V_{OL} Test Circuit

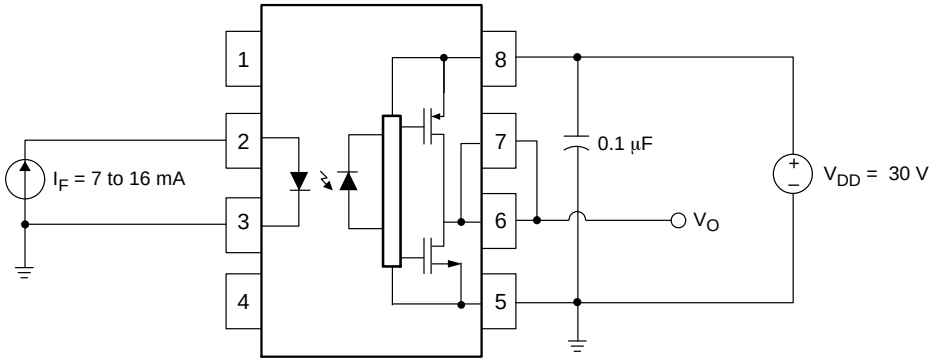


Figure 20. I_{DDH} Test Circuit

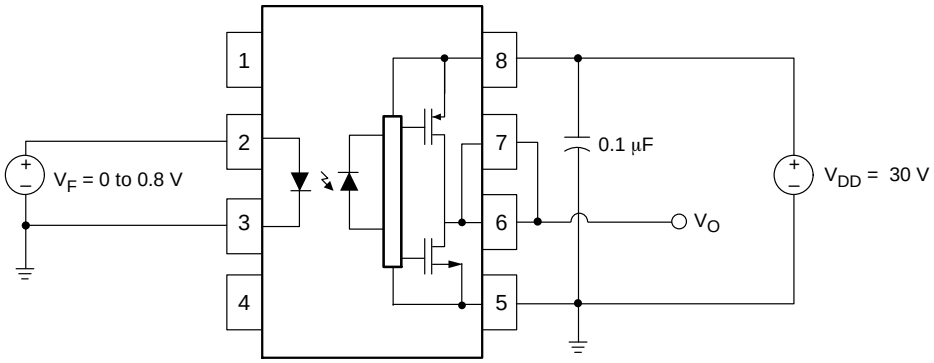


Figure 21. I_{DDL} Test Circuit

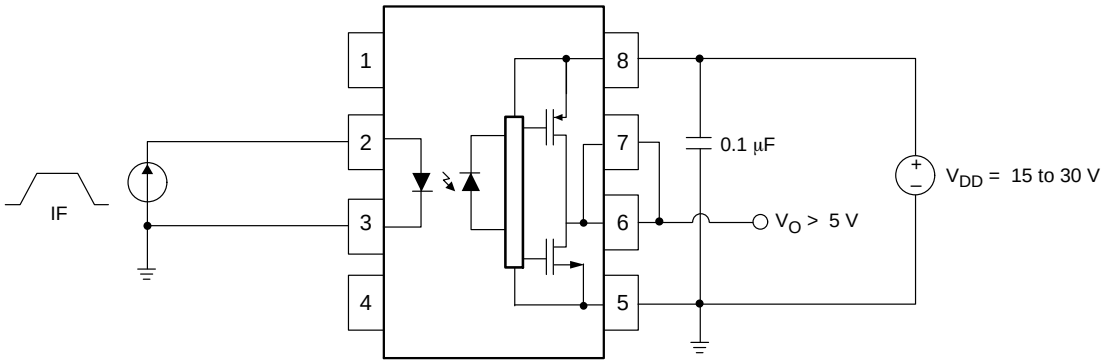


Figure 22. I_{FLH} Test Circuit

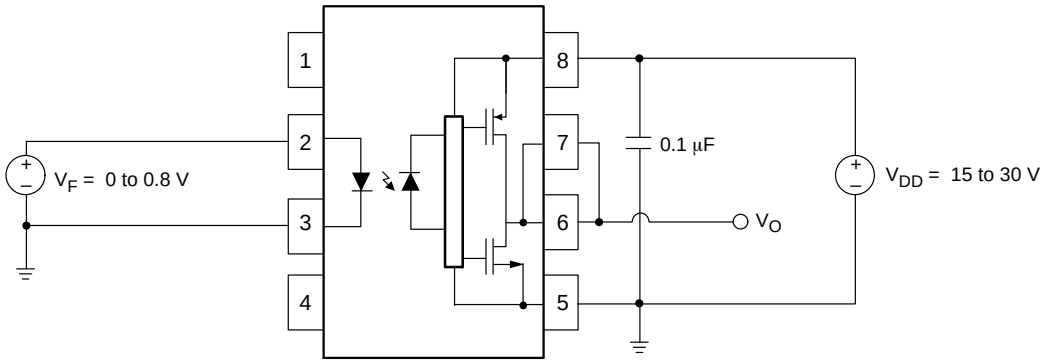


Figure 23. V_{FHL} Test Circuit

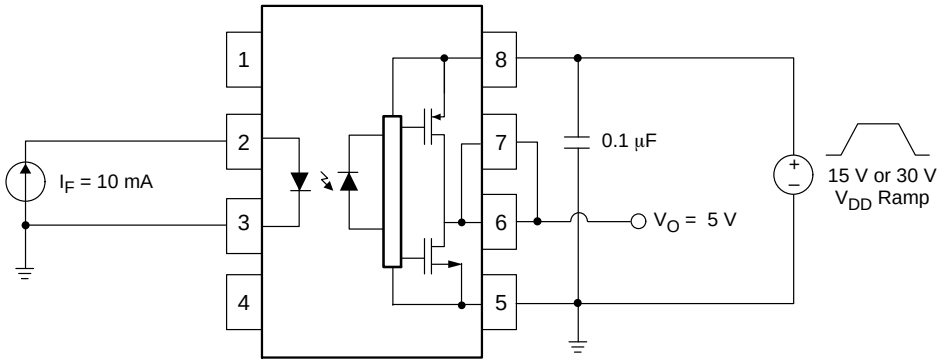


Figure 24. UVLO Test Circuit

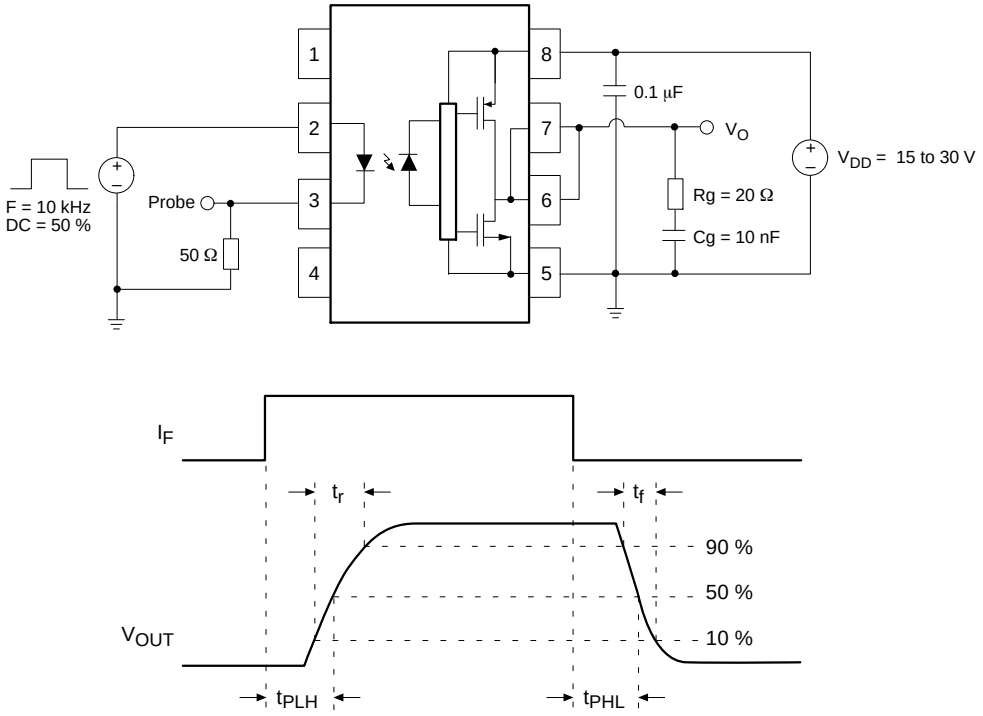


Figure 25. t_{PHL}, t_{PLH}, t_R and t_F Test Circuit and Waveforms

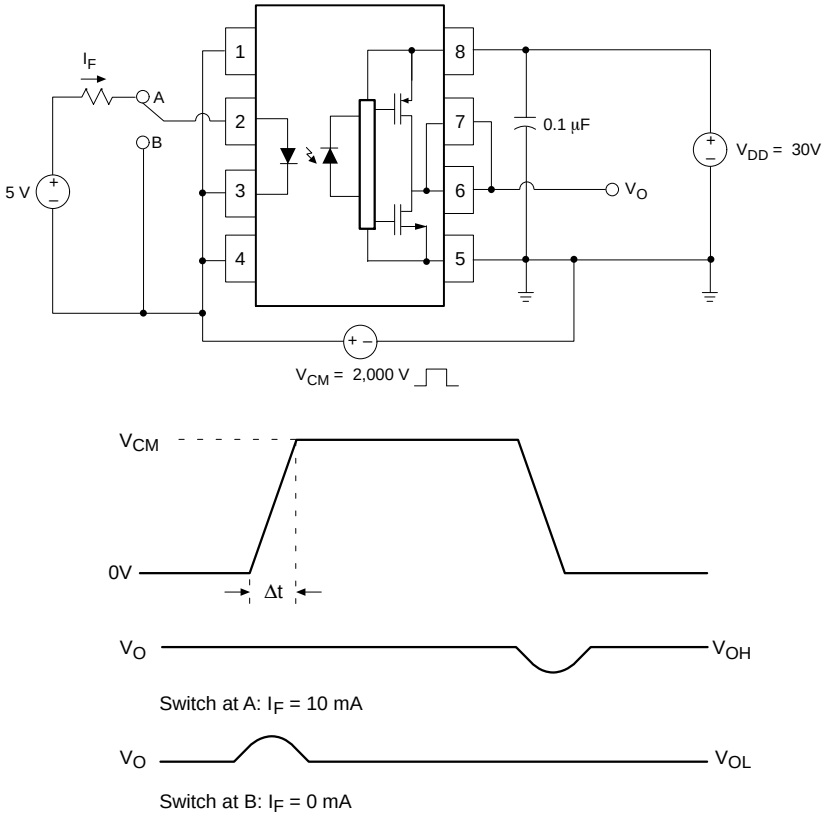
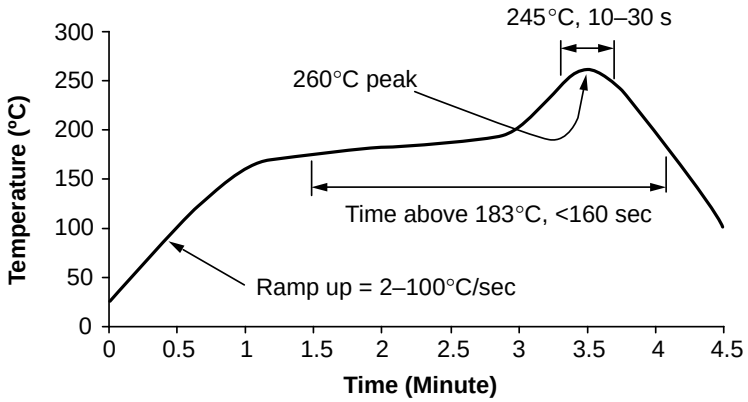


Figure 26. CMR Test Circuit and Waveforms

REFLOW PROFILE



Notes:
- Peak reflow temperature: 260°C (package surface temperature)
- Time of temperature higher than 183°C for 160 seconds or less
- One time soldering reflow is recommended

Figure 27. Reflow Profile

ORDERING INFORMATION

Part Number	Package	Shipping†
FOD3150	DIP 8−Pin	50 / Tube
FOD3150S	SMT 8−Pin (Lead Bend)	50 / Tube
FOD3150SD	SMT 8−Pin (Lead Bend)	1,000 / Tape & Reel
FOD3150V	DIP 8−Pin, IEC60747−5−5 option	50 / Tube
FOD3150SV	SMT 8−Pin (Lead Bend), IEC60747−5−5 option	50 / Tube
FOD3150SDV	SMT 8−Pin (Lead Bend), IEC60747−5−5 option	1,000 / Tape & Reel
FOD3150TV	DIP 8−Pin, 0.4” Lead Spacing, IEC60747−5−5 option	50 / Tube
FOD3150TSV	SMT 8−Pin, 0.4” Lead Spacing, IEC60747−5−5 option	50 / Tube
FOD3150TSR2V	SMT 8−Pin, 0.4” Lead Spacing, IEC60747−5−5 option	700 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

MARKING INFORMATION

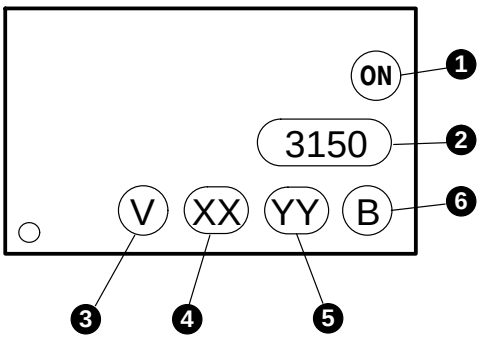


Figure 28. Device Marking

Definitions	
1	ON Semiconductor logo
2	Device number
3	IEC60747−5−5 Option (only appears on component ordered with this option)
4	Two digit year code, e.g., ‘18’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

CARRIER TAPE SPECIFICATIONS

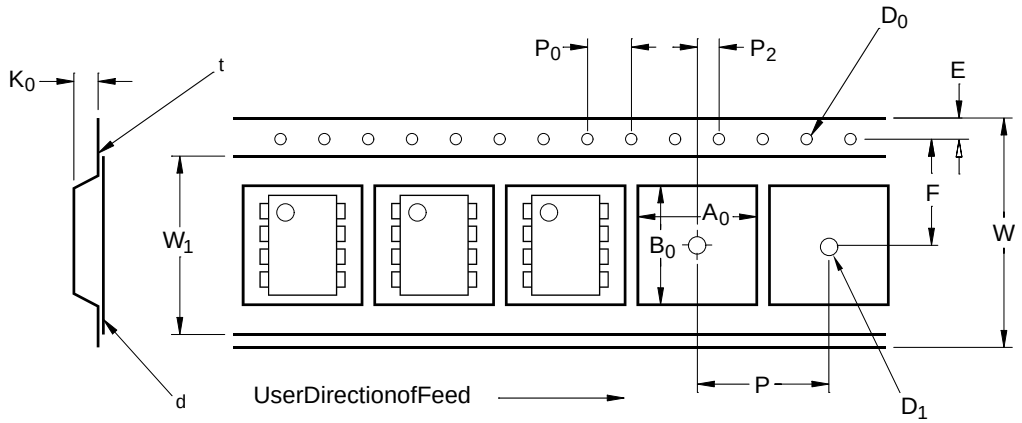


Figure 29. Carrier Tape Specifications

Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A_0	Pocket Dimensions	10.30 ± 0.20
B_0		10.30 ± 0.20
K_0		4.90 ± 0.20
W_1	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

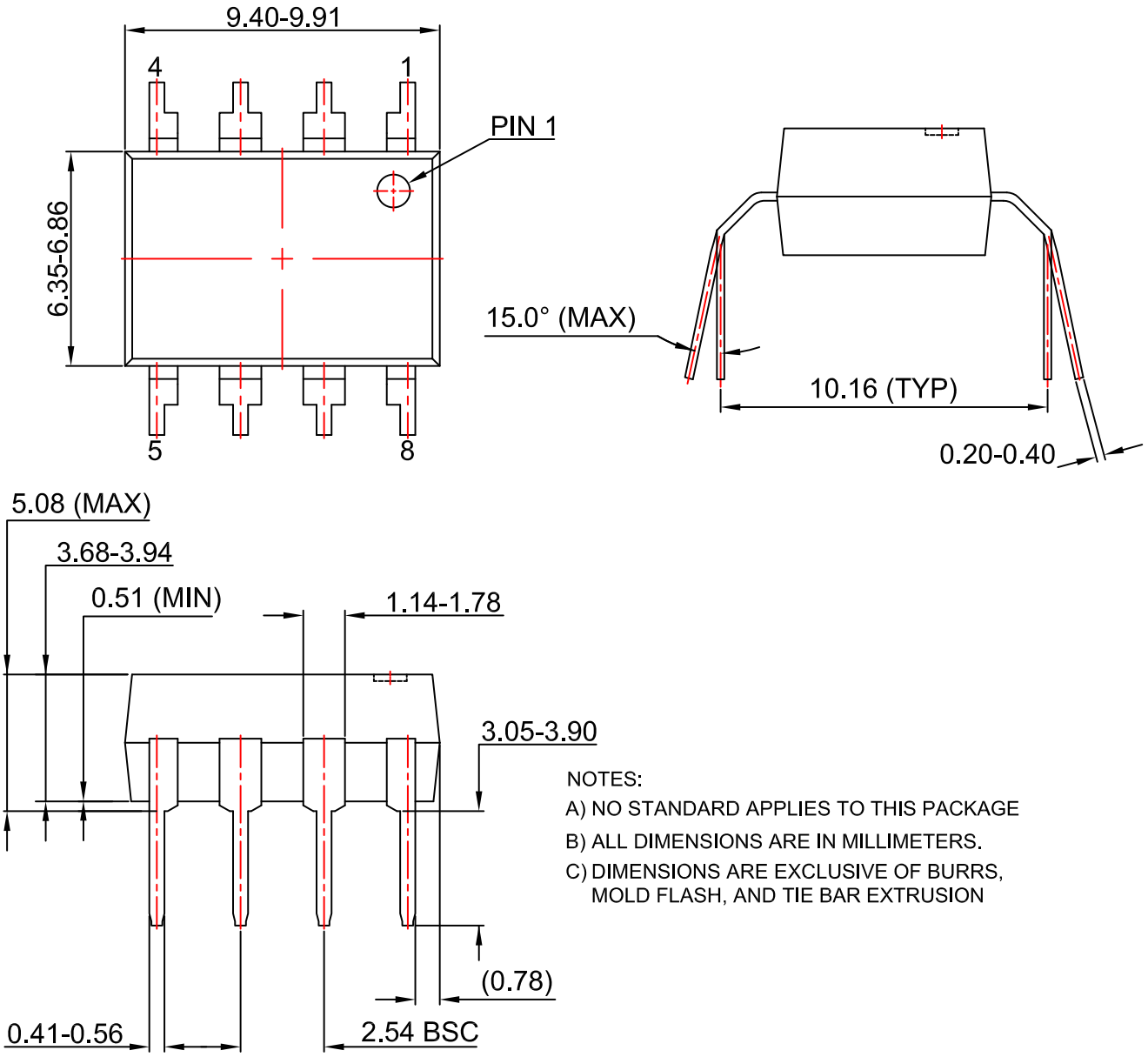
OPTOPLANAR is a registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016



NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

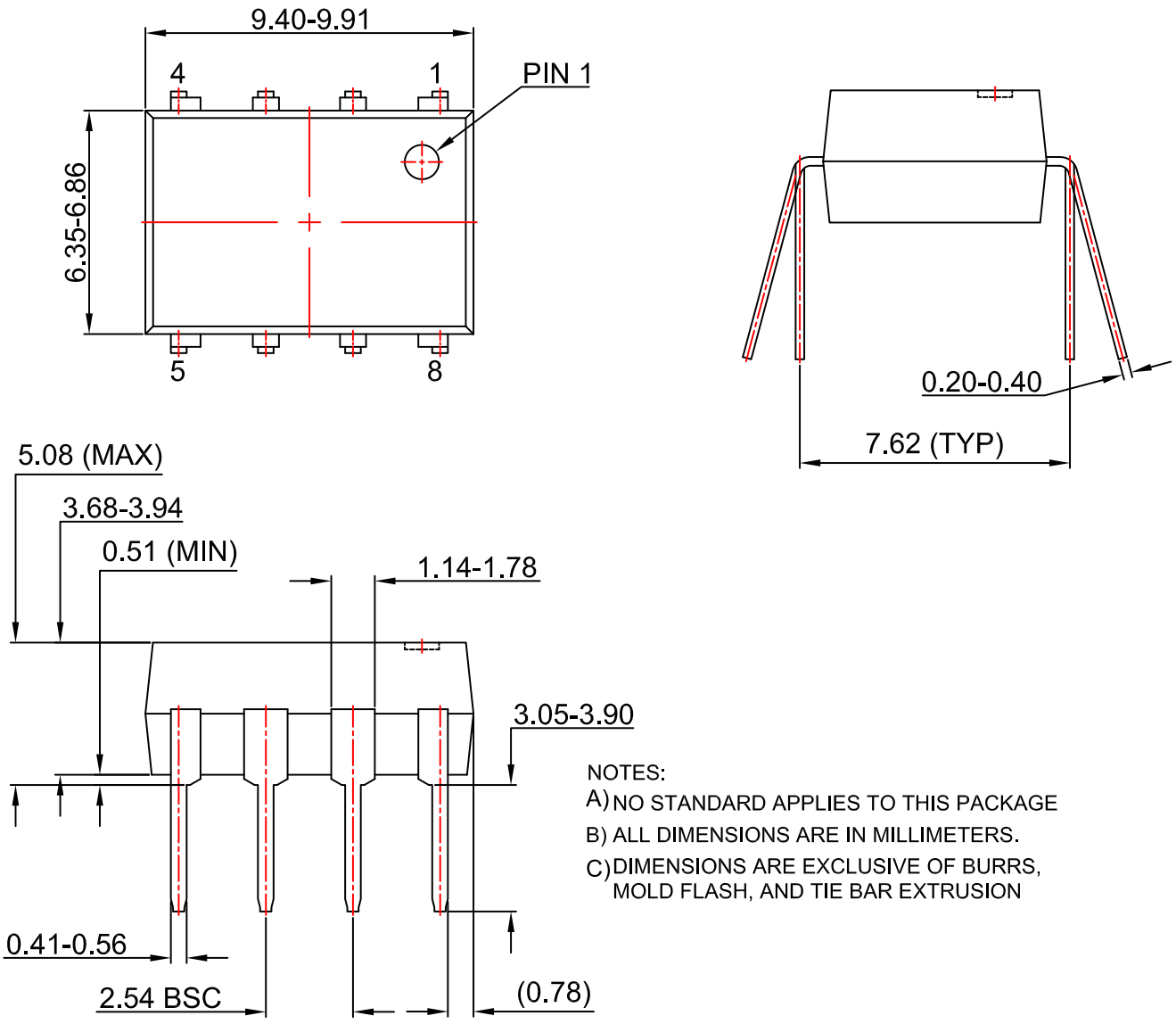
DOCUMENT NUMBER:	**98AON13445G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**PDIP8 6.6X3.81, 2.54P**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	**98AON13446G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**PDIP8 9.655X6.6, 2.54P**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

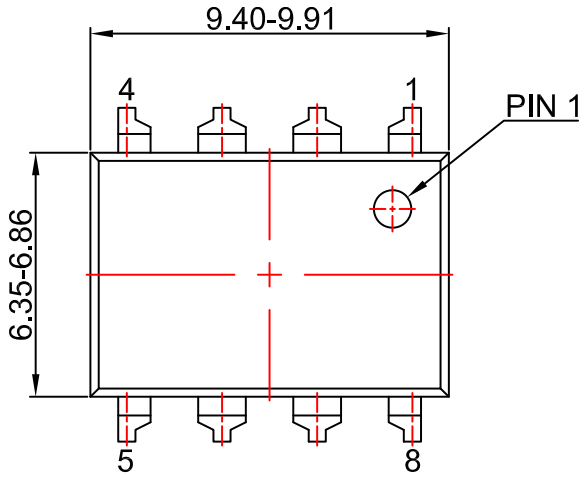
© Semiconductor Components Industries, LLC, 2019

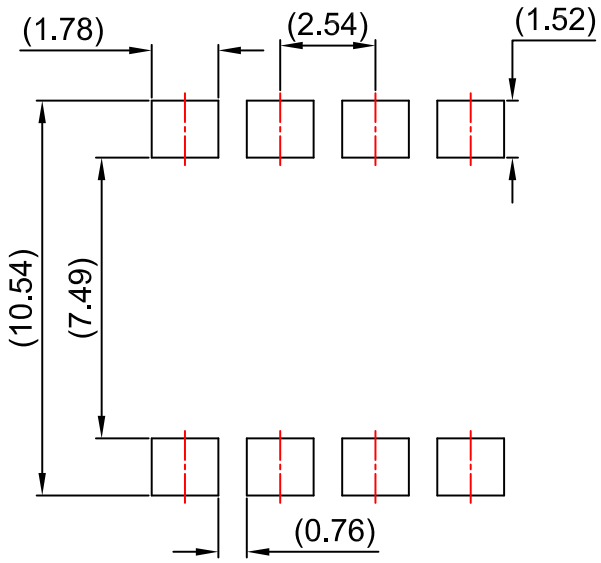
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

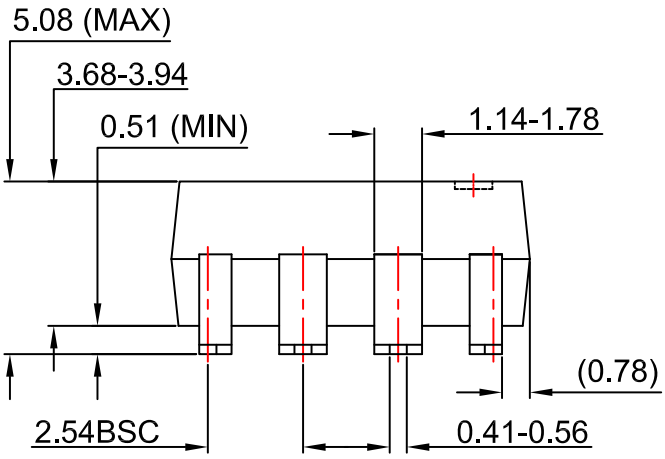
PDIP8 GW
CASE 709AC
ISSUE O

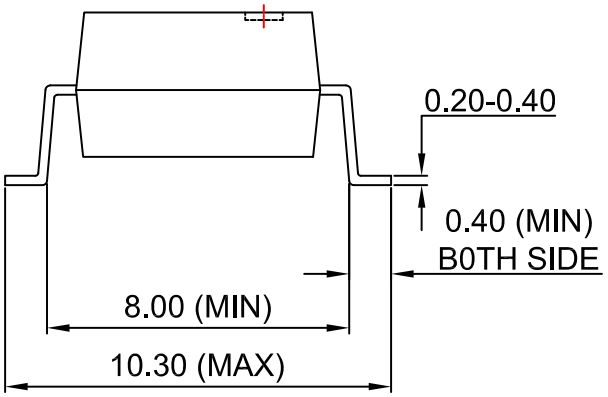
DATE 31 JUL 2016





LAND PATTERN RECOMMENDATION





NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

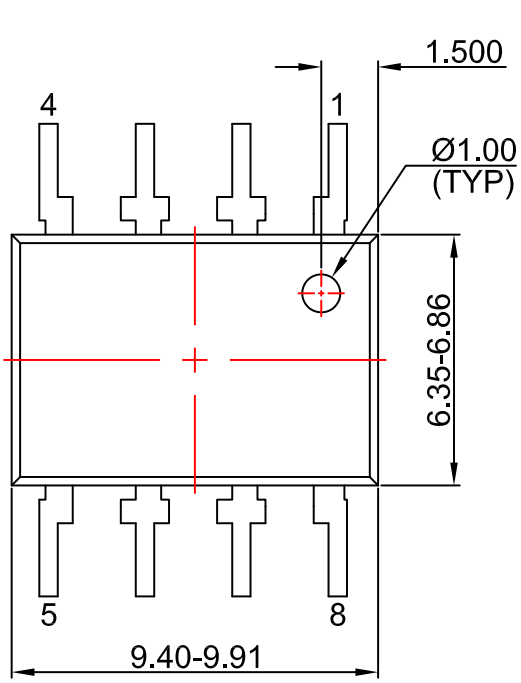
DOCUMENT NUMBER:	**98AON13447G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**PDIP8 GW**	**PAGE 1 OF 1**

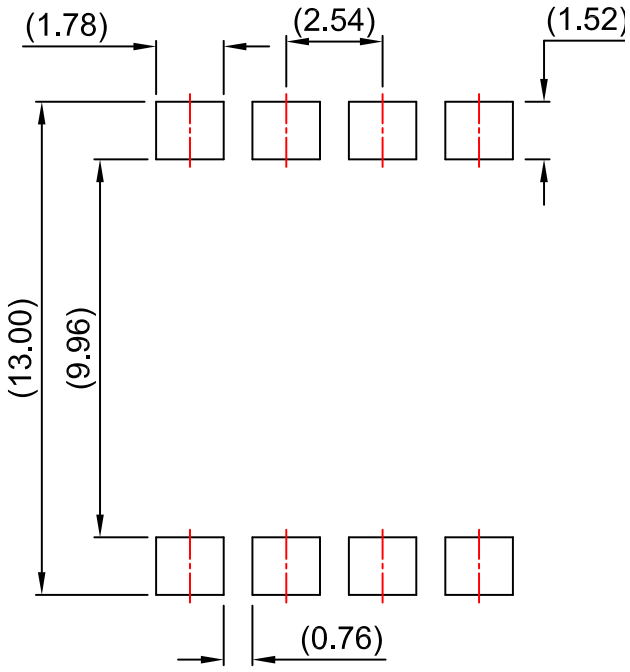
ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

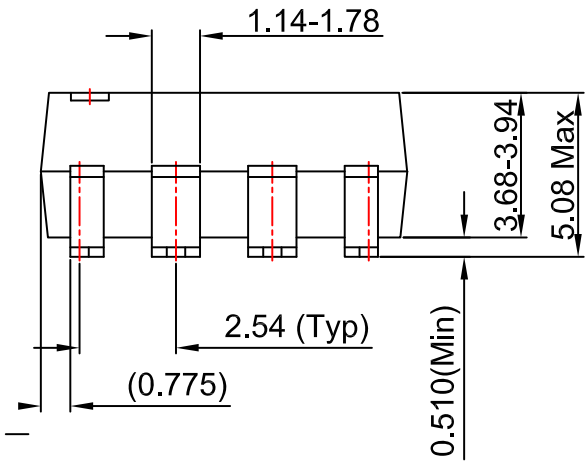
PDIP8 GW
CASE 709AD
ISSUE O

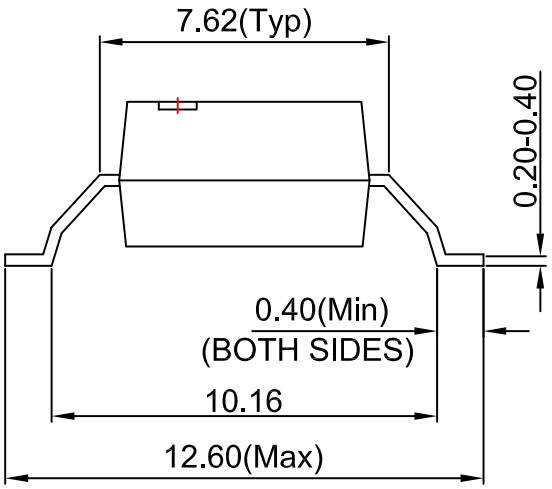
DATE 31 JUL 2016





LAND PATTERN RECOMMENDATION





NOTES:

A) NO STANDARD APPLIES TO THIS PACKAGE

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	**98AON13448G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**PDIP8 GW**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊