# MP4576

## High-Efficiency, 600mA, 60V, Fully Integrated, Synchronous Buck Converter

## DESCRIPTION

The MP4576 is a fully integrated, fixed-frequency, synchronous step-down converter. It can achieve up to 600mA of continuous output current with peak current control for excellent transient response.

The wide 4.5V to 60V input voltage range accommodates a variety of step-down applications in an automotive input environment. The device's 2µA shutdown mode quiescent current makes it ideal for battery-powered applications.

The MP4576 integrates internal high-side and low-side power MOSFETs for high efficiency without an external Schottky diode. It employs advanced asynchronous mode (AAM) to achieve high efficiency under light-load conditions by scaling down the frequency to reduce switching and gate driver losses.

Standard features include built-in soft start, enable control, and power good indication. A high duty cycle and low-dropout mode are provided for automotive cold crank conditions.

The MP4576 provides over-current protection (OCP) with valley current detection to avoid current runaway. It also has hiccup short-circuit protection (SCP), input under-voltage lockout (UVLO), and auto-recovery thermal protection.

With internal compensation, the MP4576 can offer a very compact solution with a minimal number of readily available, standard external components. The MP4576 is available in a QFN-12 (2.5mmx3mm) package.

## FEATURES

- Extends Vehicle Battery Life:
  - Low Quiescent Current in Standby Mode (40µA)
- Cooler Thermals:
  - Less than 8°C $T_J$ Rise at 600mA / 400kHz
  - 91% Efficiency (24V to 5V, 600mA, 400kHz)
  - Low-Ohmic MPS BCD FET Technology
- Low-Noise EMI/EMC:
  - MeshConnect™ Flip Chip Packaging
  - Operates Outside of AM Radio Band
- Additional Features:
  - Clock SYNC Output
  - Power Good Output
  - Internal Soft Start
  - Low-Dropout Mode
  - Hiccup Over-Current Protection
  - Selectable AAM or FCCM
- Reduces Board Size and BOM:
  - Integrated Compensation Network
  - Available in a Small QFN-12 (2.5mmx3mm) Package

## APPLICATIONS

- Infotainment
- Lamps and LEDs
- Industrial Power Systems

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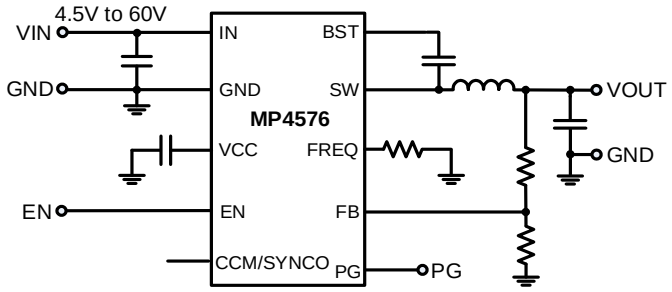
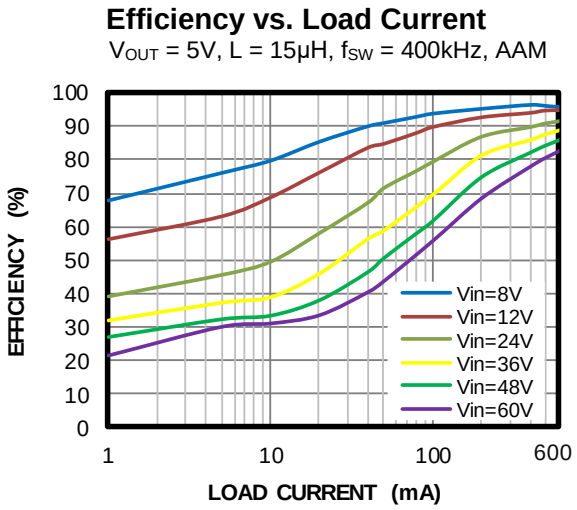
## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating** |
|---|---|---|---|
| MP4576GQBE*** | QFN-12 (2.5mmx3mm) | *See Below* | 1 |

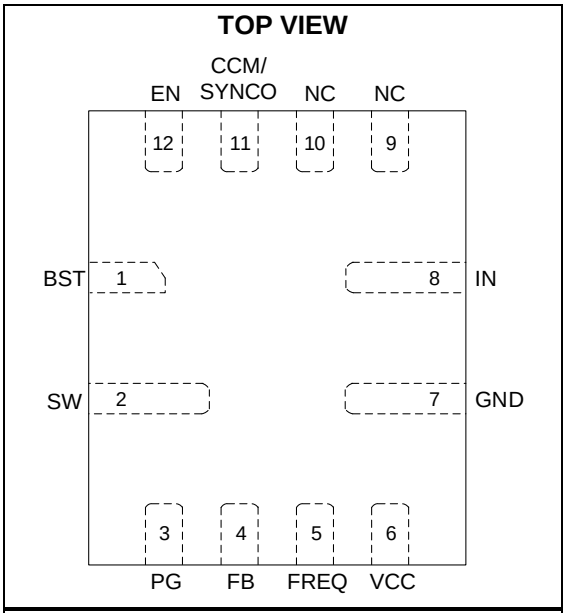
* For Tape & Reel, add suffix -Z (e.g. MP4576GQBE-Z).
** Moisture Sensitivity Level Rating.
*** Wettable Flank Package.

## TOP MARKING

BUK
YWW
LLL

BUK: Product code of MP4576GQBE
Y: Year code
WW: Week code
LLL: Lot number

## PACKAGE REFERENCE




QFN-12 (2.5mmx3mm)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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | BST | **Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. |
| 2 | SW | **Switch output.** SW is the output of the internal power switches. A wide PCB trace is recommended when making the SW connection. |
| 3 | PG | **Power good indicator.** The PG pin is an open drain. Connect PG to the power source with a pull-up resistor. PG is pulled up to the power source if the output voltage is within 90% to 108% of the nominal voltage. PG goes low if the output voltage exceeds 116% or falls below 84% of the nominal voltage. |
| 4 | FB | **Feedback point.** FB is the negative input of the error amplifier (typically 0.8V). To set the regulation voltage, connect FB to the tap of the external resistor divider placed between the output and GND. The power good and under-voltage lockout circuits use the FB pin to monitor the output voltage. |
| 5 | FREQ | **Configurable switching frequency.** Connect a resistor from FREQ to GND to set the switching frequency. |
| 6 | VCC | **Internal bias supply.** The VCC pin supplies power to the internal control circuit and gate drivers. Connect a decoupling capacitor (greater than 1µF) from VCC to ground, and place it as close as possible to VCC. |
| 7 | GND | **IC ground.** Connect the GND pin to larger copper areas at the negative terminals of the input and output capacitors. |
| 8 | IN | **Input supply.** The IN pin supplies all power to the converter. To reduce switching spikes, place a decoupling capacitor from IN to ground, and as close as possible to the IC. |
| 9, 10 | NC | **No connection.** The NC pins can be connected to GND to improve thermal and EMI performance. |
| 11 | CCM/ SYNCO | **Mode selection/synchronization output.** Connect the CCM/SYNCO pin to GND through a resistor (10kΩ to 300kΩ) to force the converter into forced continuous conduction mode (CCM). Float this pin to force the converter into advanced asynchronous mode (AAM) under light-load conditions. CCM/SYNCO is also a synchronization output pin that can output a 180° out-of-phase clock to other devices. |
| 12 | EN | **Enable.** Drive EN above 1.45V to turn on the device; float EN or drive it below 1.12V to turn off the device. |


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## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ .....65V
$V_{SW}$ .....-0.3V to $V_{IN}$ + 0.3V
$V_{BST}$ .....$V_{SW}$ + 6V
All other pins..... -0.3V to +6V
Continuous power dissipation ($T_A$ = 25°C) (2) (4)
QFN-12 (2.5mmx3mm).....2.78W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

### *Electrostatic Discharge (ESD) Ratings*

Human body model (HBM) ..... ±2kV
Charged device model (CDM) .....±750V

### *Recommended Operating Conditions*

Continuous supply voltage ($V_{IN}$)..... 4.5V to 60V
Output voltage ($V_{OUT}$)..... 1V to 90% of $V_{IN}$
Load current range .....0mA to 600mA
Operating junction temp ($T_J$).....-40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| QFN-12 (2.5mmx3mm) | | |
| JESD51-7 (3) | 60 | 13 °C/W |
| EVQ4576-QB-00A (4) | 45 | 11 °C/W |

**Notes:**

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
4) Measured on MPS standard EVB: 8.9cmx8.9cm, 2oz copper thick, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 24V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C [5], typical values are at $T_J$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input Supply and Under-Voltage Lockout (UVLO)** | | | | | | |
| Supply current (quiescent) | $I_Q$ | No load, $V_{FB}$ = 0.85V, AAM | | 40 | 65 | μA |
| Supply current (shutdown) | $I_{SD}$ | $V_{EN}$ = 0V | | 2 | 5 | μA |
| $V_{IN}$ UVLO rising threshold | $INUV_{VTH-R}$ | | 3.8 | 4.0 | 4.2 | V |
| $V_{IN}$ UVLO falling threshold | $INUV_{VTH-F}$ | | 3.3 | 3.5 | 3.7 | V |
| $V_{IN}$ UVLO hysteresis threshold | $INUV_{HYS}$ | | | 500 | | mV |
| **Output and Regulation** | | | | | | |
| Regulated FB reference | $V_{REF}$ | $T_J$ = 25°C | 0.792 | 0.800 | 0.808 | V |
| | | $T_J$ = -40°C to +125°C | 0.784 | | 0.816 | V |
| FB input current | $I_{FB}$ | $V_{FB}$ = 0.85V | | 10 | 50 | nA |
| **Switches and Frequency** | | | | | | |
| High-side switch on resistance | $R_{DS(ON)-H}$ | $V_{BST}$ - $V_{SW}$ = 5V, $T_J$ = 25°C | 150 | 250 | 350 | mΩ |
| | | $V_{BST}$ - $V_{SW}$ = 5V, $T_J$ = -40°C to +125°C | 100 | | 500 | |
| Low-side switch on resistance | $R_{DS(ON)-L}$ | $T_J$ = 25°C | 30 | 45 | 60 | mΩ |
| | | $T_J$ = -40°C to +125°C | 20 | | 90 | |
| SW leakage current | $I_{SW-LKG}$ | $V_{EN}$ = 0V, $V_{SW}$ = 0V or 60V | | 0.1 | 30 | μA |
| Switching frequency | $f_{SW}$ | $R_{FREQ}$ = 76.8kΩ | 300 | 400 | 500 | kHz |
| | | $R_{FREQ}$ = 28kΩ | 750 | 1000 | 1250 | kHz |
| | | $R_{FREQ}$ = 12.1kΩ | 1800 | 2200 | 2700 | kHz |
| Minimum on time [6] | $t_{ON-MIN}$ | | | 90 | | ns |
| Minimum off time [6] | $t_{OFF-MIN}$ | | | 100 | | ns |
| **Power Good (PG)** | | | | | | |
| PG current sink capacity | $V_{PG-SINK}$ | Sink 4mA | | | 300 | mV |
| PG delay time | $t_{PG-DELAY}$ | Rising edge | | 70 | | μs |
| | | Falling edge | | 25 | | μs |
| PG leakage current | $I_{PG-LKG}$ | | | 10 | 1000 | nA |
| PG rising threshold ($V_{FB}$ / $V_{REF}$) | $PG_{RISING}$ | $V_{FB}$ rising | | 90 | | % |
| | | $V_{FB}$ falling | | 108 | | % |
| PG falling threshold ($V_{FB}$ / $V_{REF}$) | $PG_{FALLING}$ | $V_{FB}$ falling | | 84 | | % |
| | | $V_{FB}$ rising | | 116 | | % |
| **Enable (EN)** | | | | | | |
| EN input rising threshold | $V_{EN-RISING}$ | | 1.38 | 1.45 | 1.52 | V |
| EN input falling threshold | $V_{EN-FALLING}$ | | 1.05 | 1.12 | 1.19 | V |
| EN threshold hysteresis | $V_{EN-HYS}$ | | | 330 | | mV |
| EN input current | $I_{EN}$ | $V_{EN}$ = 2V | | 0.7 | | μA |
| EN turn-off delay | $t_{EN-DELAY}$ | | 5 | | | μs |
| **BST** | | | | | | |
| BST-SW UVLO | | | | 1.4 | 2.5 | V |
| BST-SW UVLO hysteresis | | | | 60 | | mV |
| **Soft Start and VCC** | | | | | | |
| Soft-start time | $t_{SS}$ | | | 0.45 | | ms |
| VCC regulator | $V_{CC}$ | $I_{CC}$ = 0mA | 4.6 | 4.9 | 5.2 | V |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C [5], typical values are at $T_J$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Protections** | | | | | | |
| Peak current limit | $I_{PEAK-LIMIT}$ | 20% duty cycle | 1 | 1.7 | 2.2 | A |
| Valley current limit | $I_{VALLEY-LIMIT}$ | | 1 | | | A |
| Zero-cross threshold | $I_{ZCD}$ | AAM | -100 | 140 | +300 | mA |
| Negative current limit | $I_{NEG-LIMIT}$ | FCCM | -2 | -1.3 | -0.8 | A |
| Thermal shutdown [6] | $T_{SD}$ | Temperature rising | | 170 | | °C |
| Thermal shutdown hysteresis [6] | $T_{SD-SYS}$ | | | 25 | | °C |

**Notes:**

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Derived from the bench characterization. Not tested in production.


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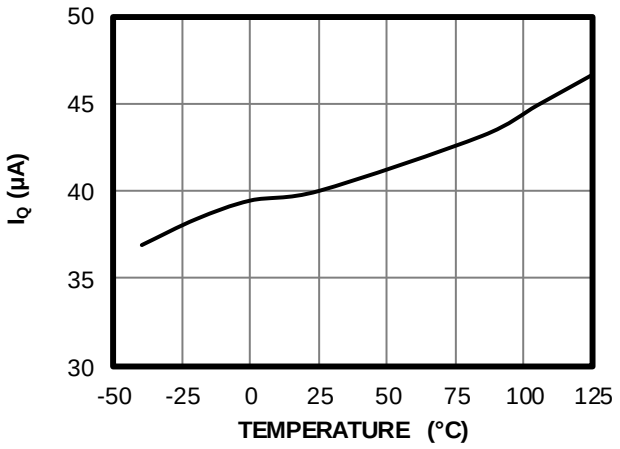
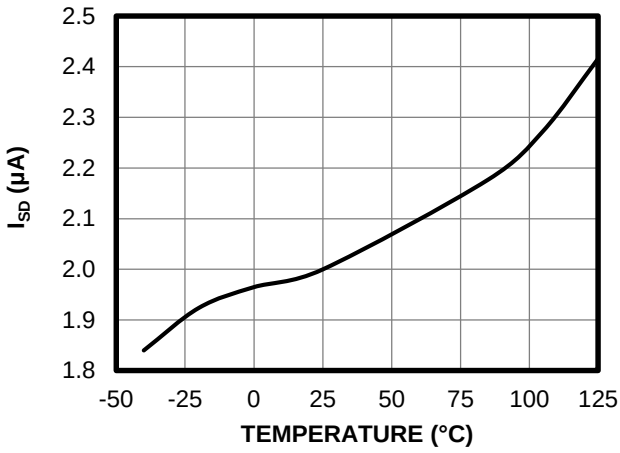
## TYPICAL CHARACTERISTICS

**$V_{IN}$ = 24V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

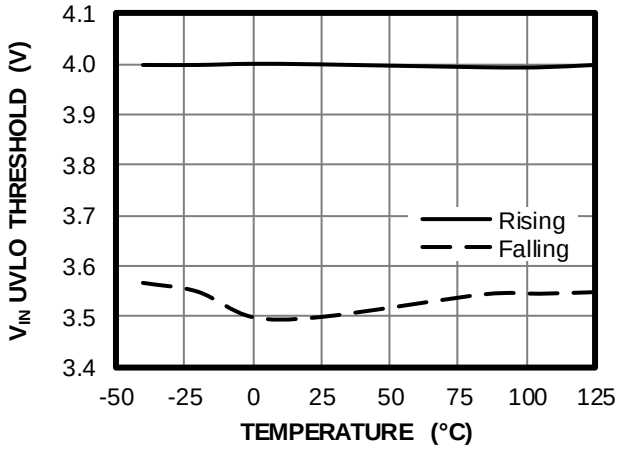
### Quiescent Current vs. Temperature



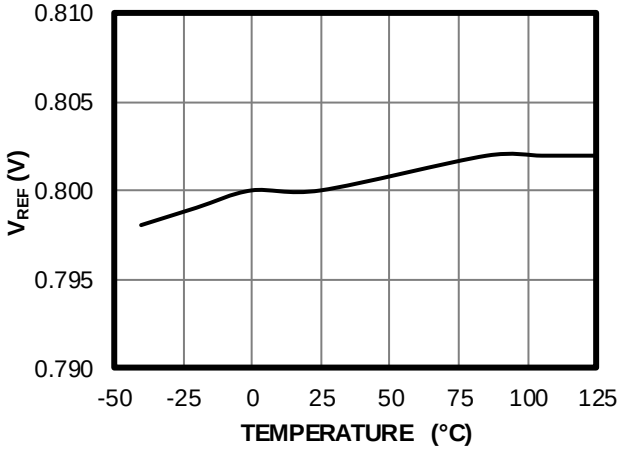

### Shutdown Current vs. Temperature



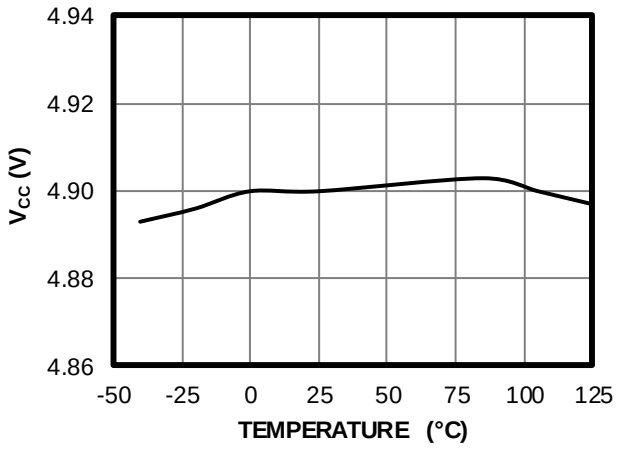

### $V_{IN}$ UVLO Threshold vs. Temperature



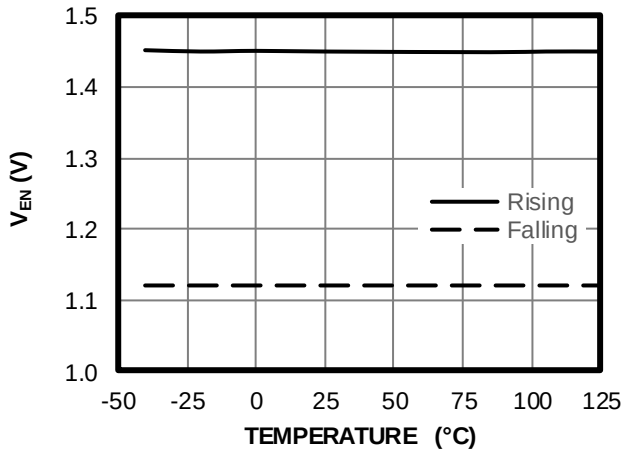

### Reference Voltage vs. Temperature




### $V_{CC}$ vs. Temperature




### EN Threshold vs. Temperature





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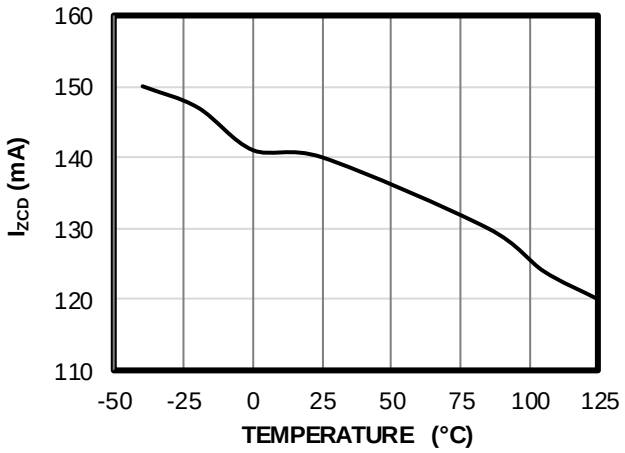
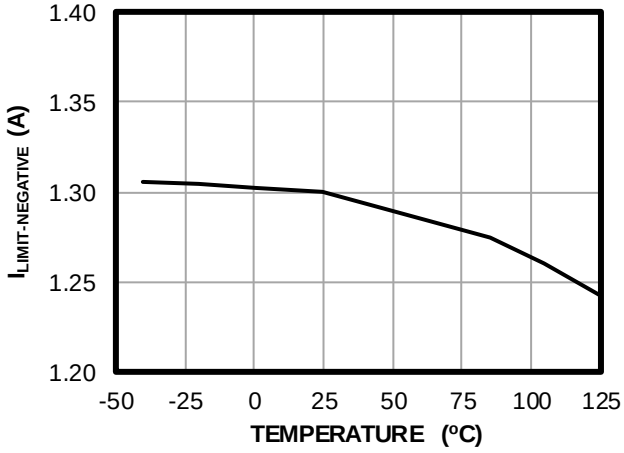
## TYPICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

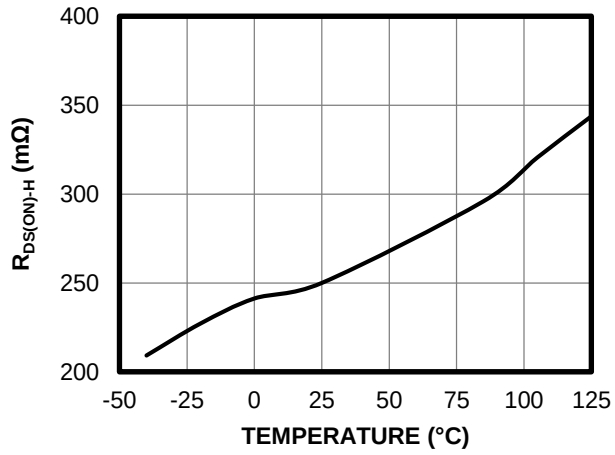
**Zero-Current Detection (ZCD) vs. Temperature**



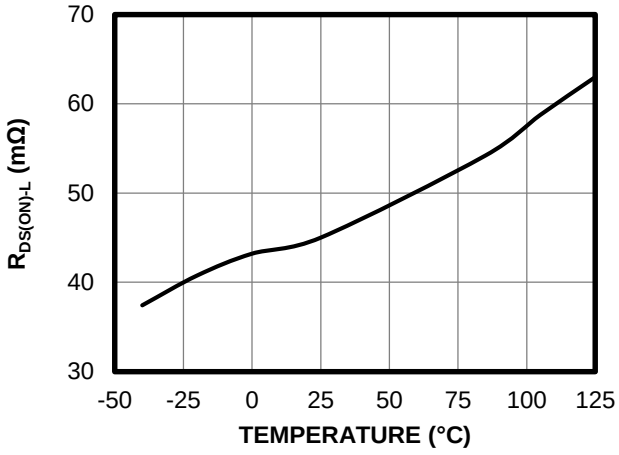

**Negative Current Limit vs. Temperature**



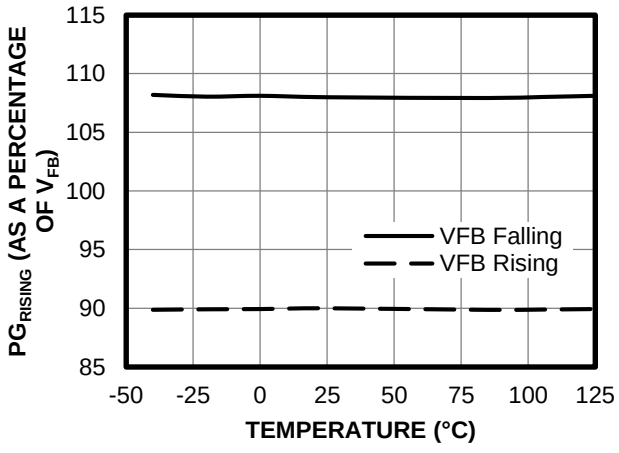

**HS-FET On Resistance vs. Temperature**



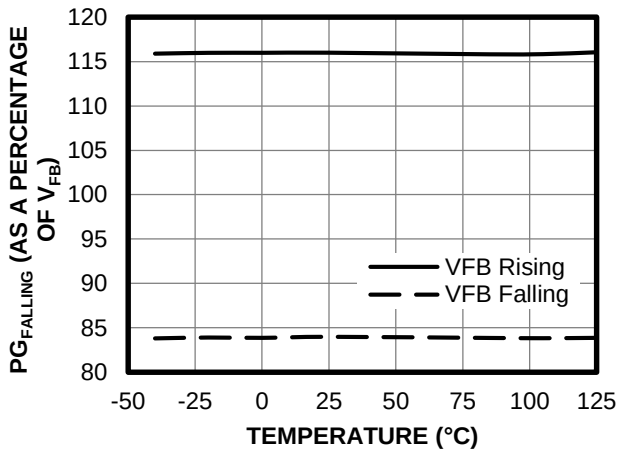

**LS-FET On Resistance vs. Temperature**




**PG Rising Threshold vs. Temperature**




**PG Falling Threshold vs. Temperature**





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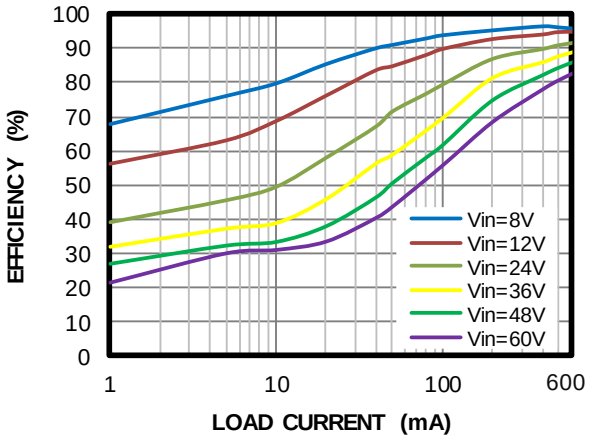
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, AAM, $T_A$ = 25°C, unless otherwise noted.**

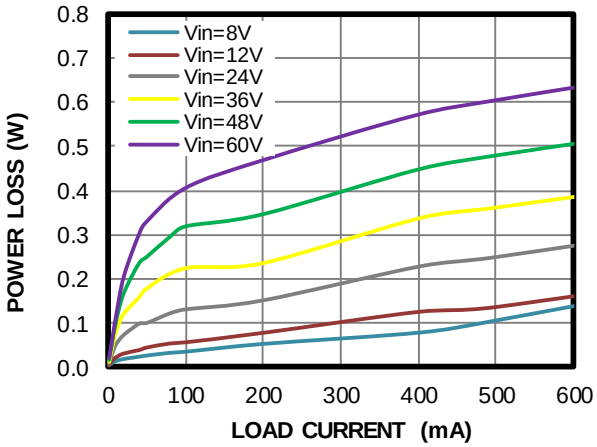
### Efficiency vs. Load Current

$f_{SW}$ = 400kHz, L = 15µH [7], AAM



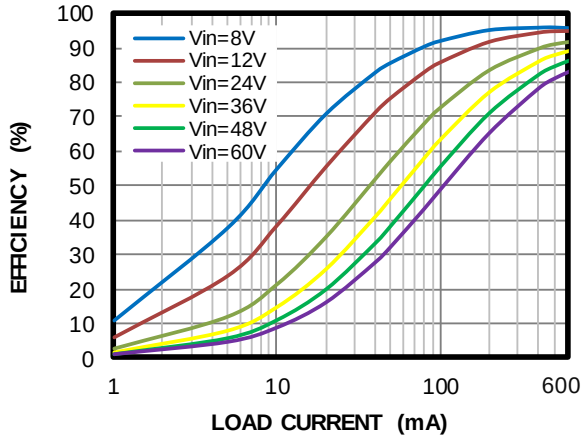

### Power Loss vs. Load Current

$f_{SW}$ = 400kHz, L = 15µH [7], AAM



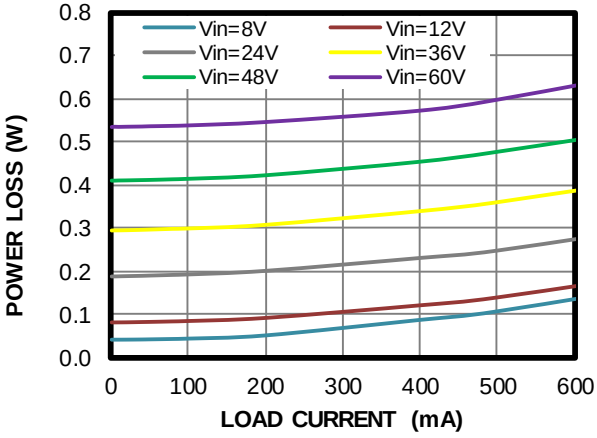

### Efficiency vs. Load Current

$f_{SW}$ = 400kHz, L = 15µH [7], FCCM



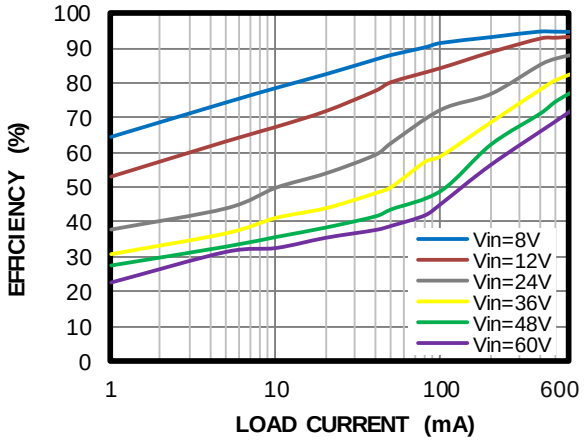

### Power Loss vs. Load Current

$f_{SW}$ = 400kHz, L = 15µH [7], FCCM



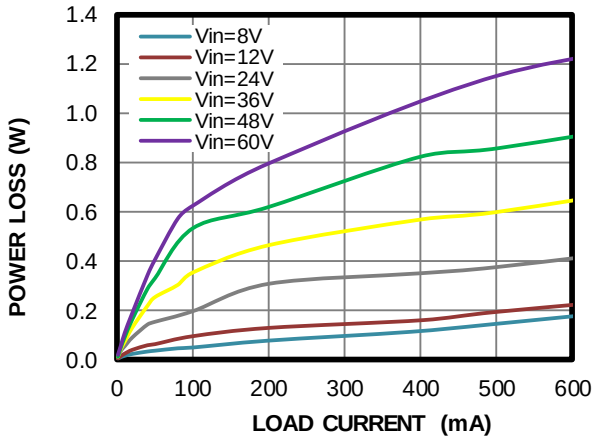

### Efficiency vs. Load Current

$f_{SW}$ = 1MHz, L = 10µH [8], AAM




### Power Loss vs. Load Current

$f_{SW}$ = 1MHz, L = 10µH [8], AAM





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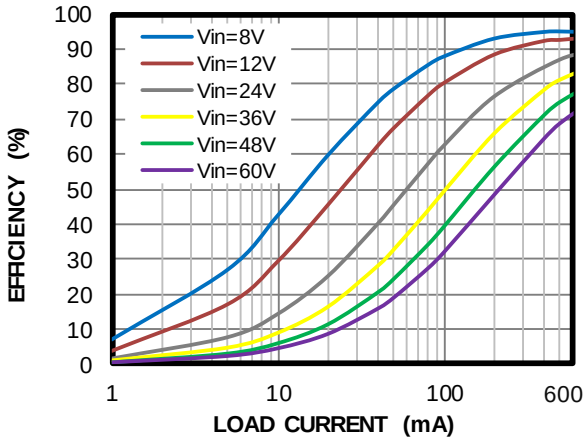
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, AAM, $T_A$ = 25°C, unless otherwise noted.**

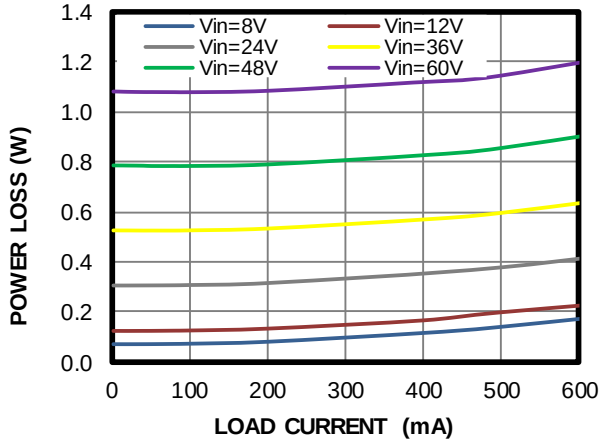
### Efficiency vs. Load Current

$f_{SW}$ = 1MHz, L = 10µH [8], FCCM



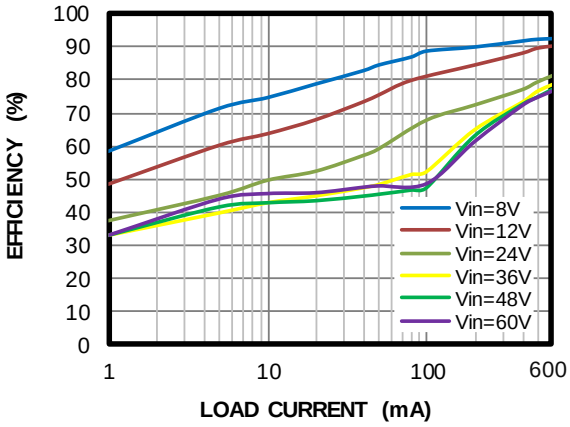

### Power Loss vs. Load Current

$f_{SW}$ = 1MHz, L = 10µH [8], FCCM



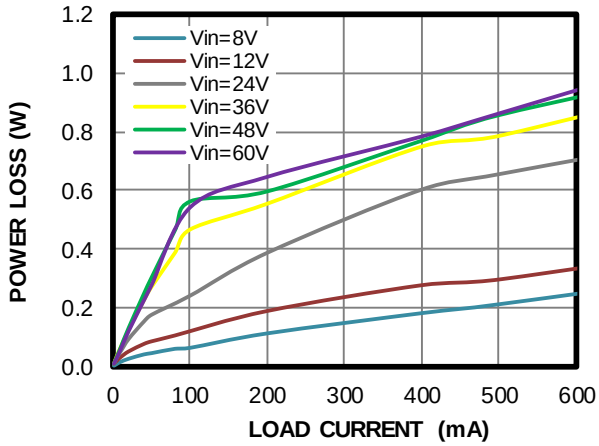

### Efficiency vs. Load Current

$f_{SW}$ = 2.2MHz, L = 4.7µH [9], AAM



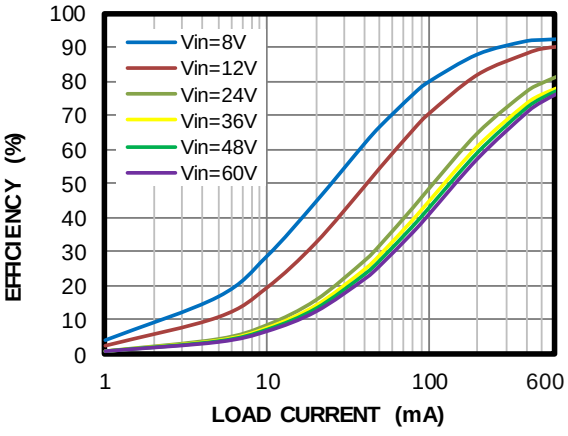

### Power Loss vs. Load Current

$f_{SW}$ = 2.2MHz, L = 4.7µH [9], AAM



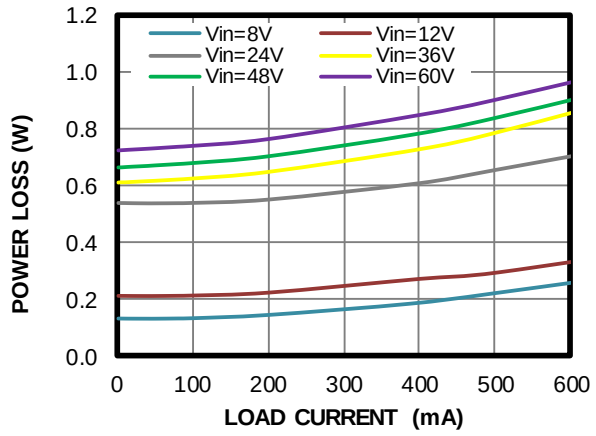

### Efficiency vs. Load Current

$f_{SW}$ = 2.2MHz, L = 4.7µH [9], FCCM




### Power Loss vs. Load Current

$f_{SW}$ = 2.2MHz, L = 4.7µH [9], FCCM





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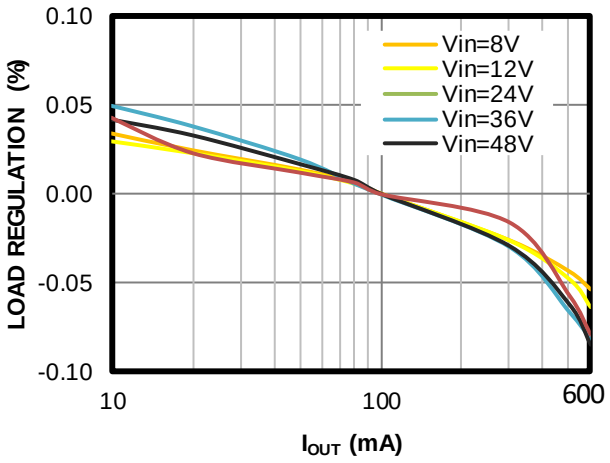
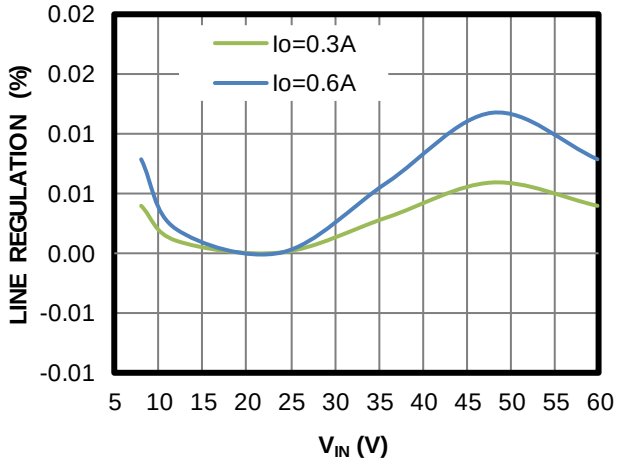
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, AAM, $T_A$ = 25°C, unless otherwise noted.**

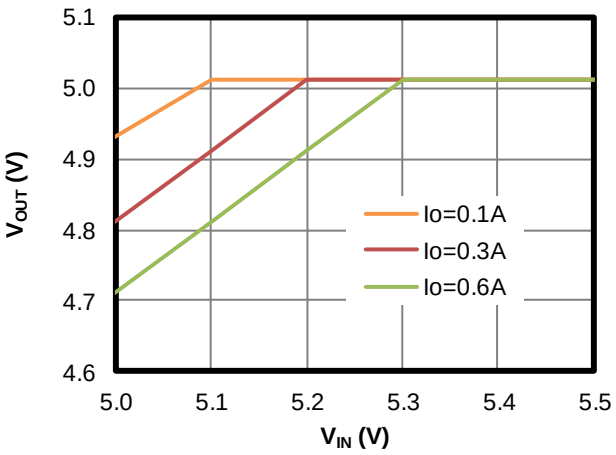
### Load Regulation



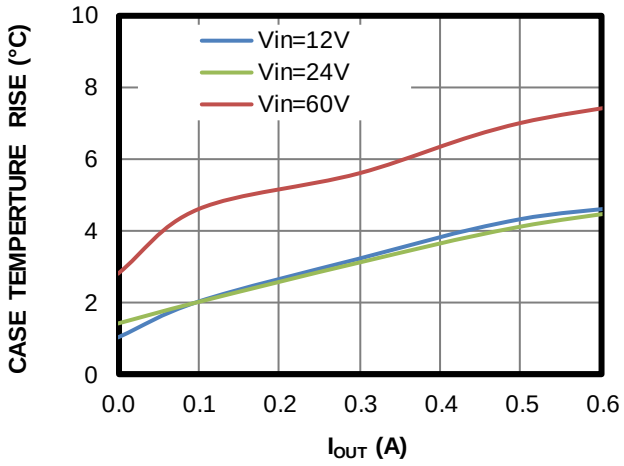

### Line Regulation



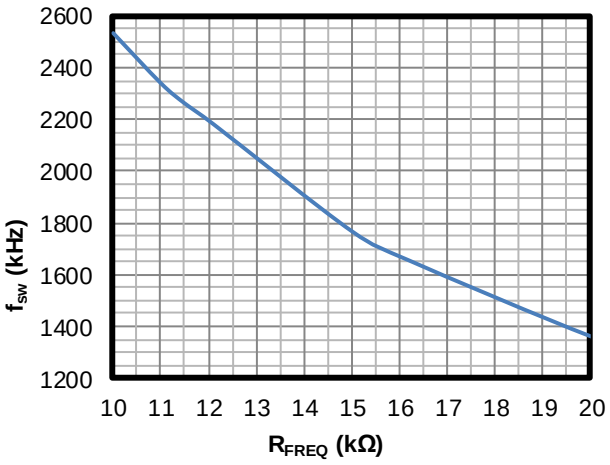

### Dropout vs Input Voltage



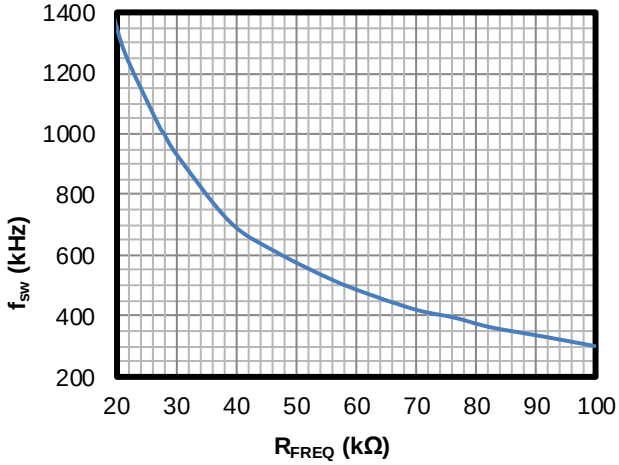

### Case Temperature Rise vs. Load Current




### $f_{SW}$ vs $R_{FREQ}$




### $f_{SW}$ vs $R_{FREQ}$





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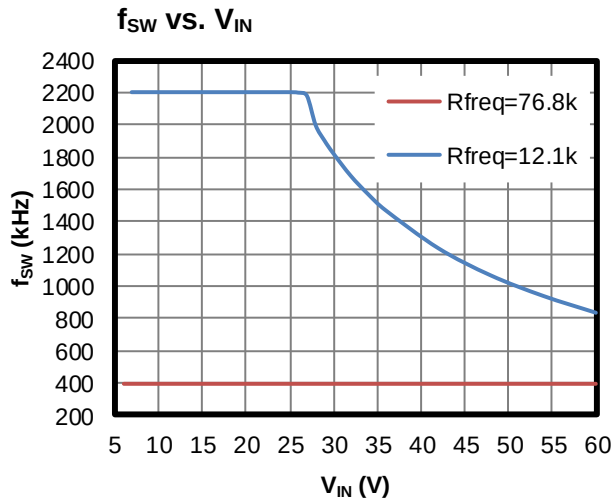
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, AAM, $T_A$ = 25°C, unless otherwise noted.**




**Notes:**

7) Inductor: XAL6060-153MEB/C, DCR = 43.75mΩ.
8) Inductor: XAL6060-103MEB/C, DCR = 29.82mΩ
9) Inductor: XAL5030-472MEB/C, DCR = 36.00mΩ.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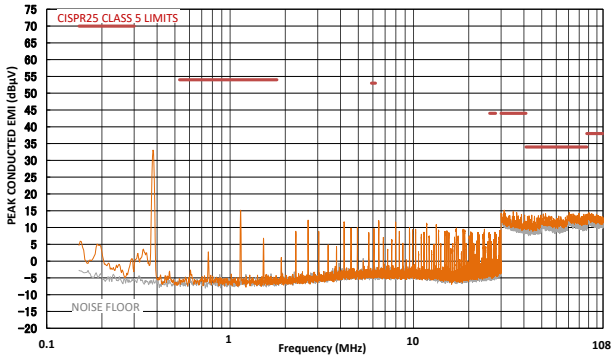
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 600mA, L = 15µH, $f_{SW}$ = 400kHz, AAM, $T_A$ = 25°C, unless otherwise noted.** (10)

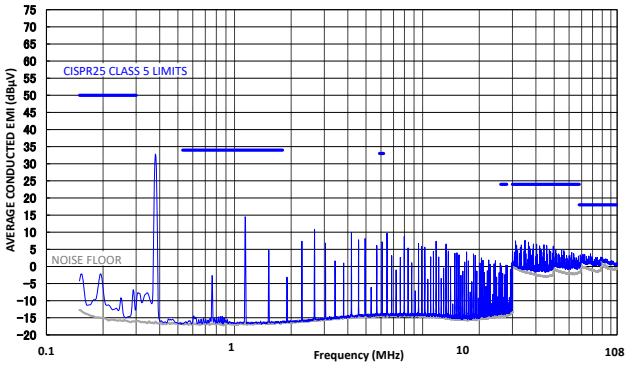
### CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



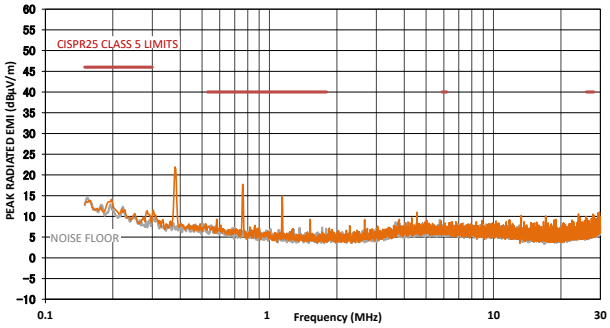

### CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



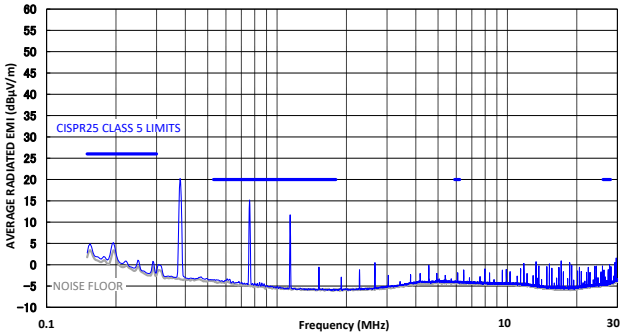

### CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



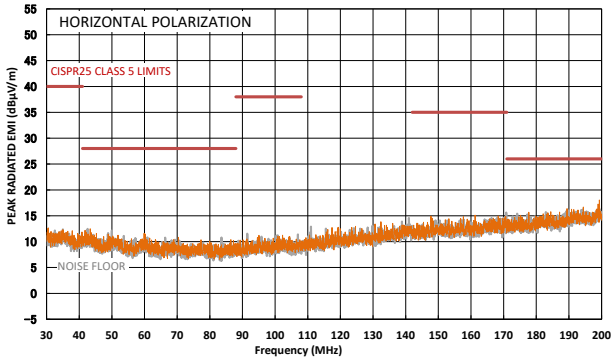

### CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



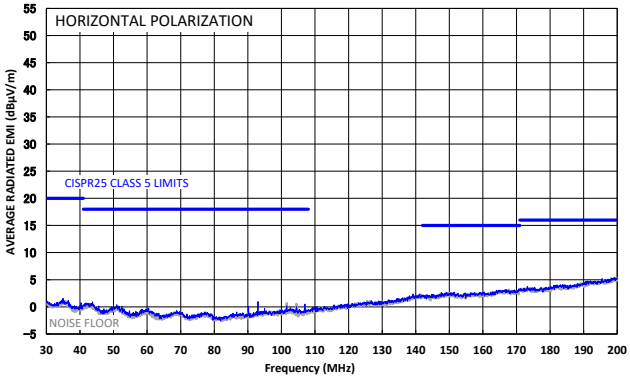

### CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz




### CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz





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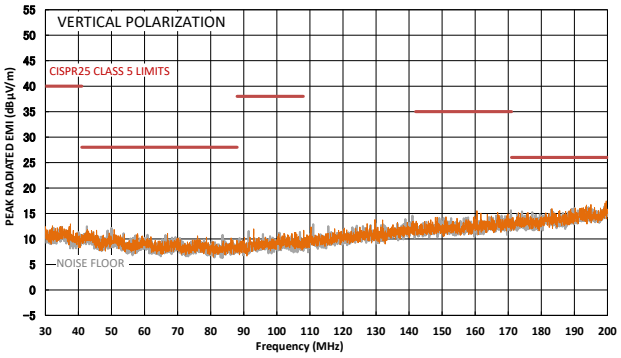
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 600mA, L = 15µH, $f_{SW}$ = 400kHz, AAM, $T_A$ = 25°C, unless otherwise noted.** (10)

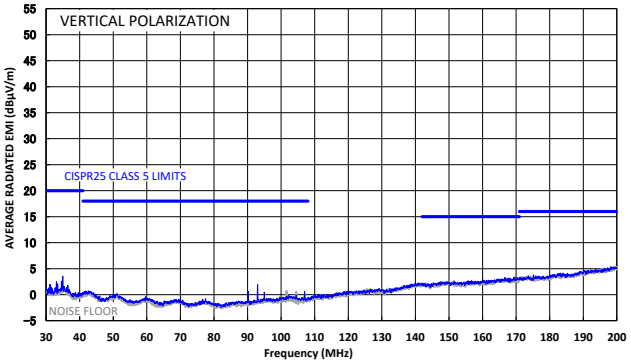
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



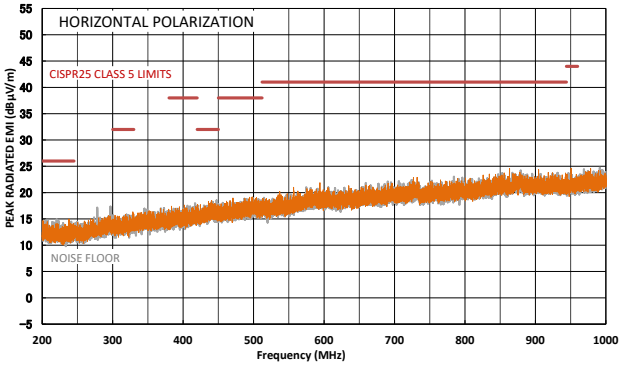

### CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



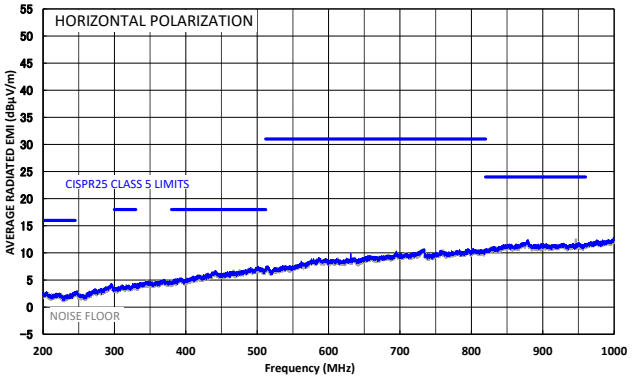

### CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



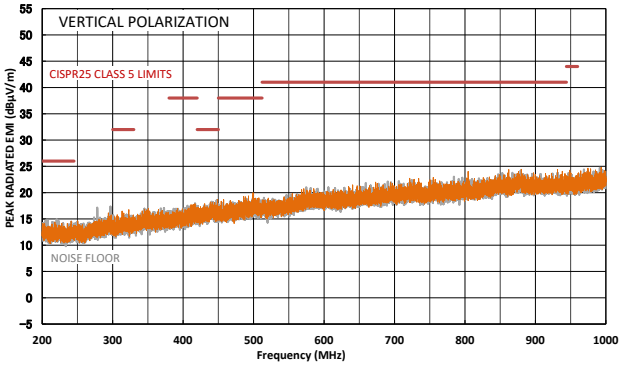

### CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



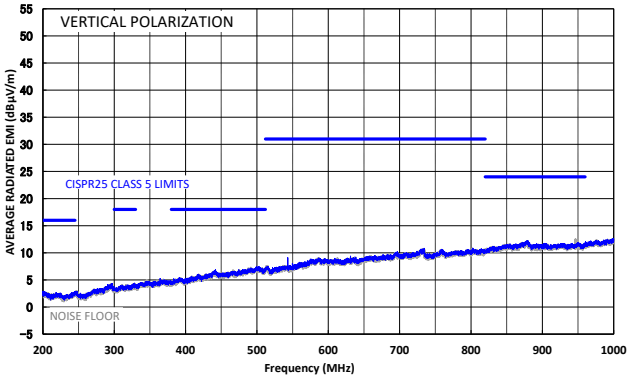

### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz




### CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz




**Note:**

10) The EMC test results are based on the application circuit with an EMI filter (see Figure 9 on page 31) and tested on the EVQ4576-QB-00A. The inductance used in EMI testing is XAL4040-153MEB.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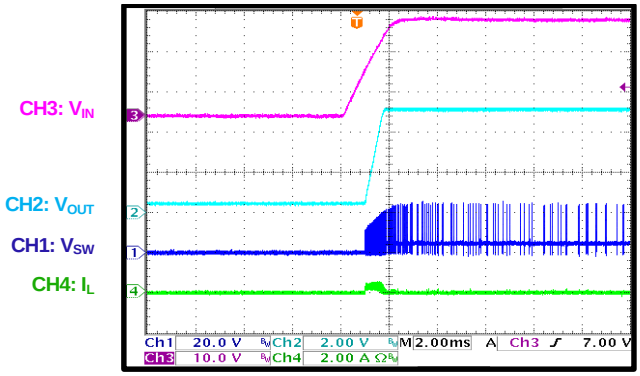
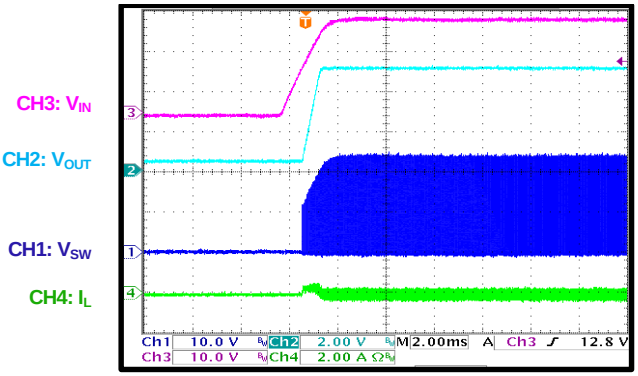
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, $T_A$ = 25°C, unless otherwise noted.**

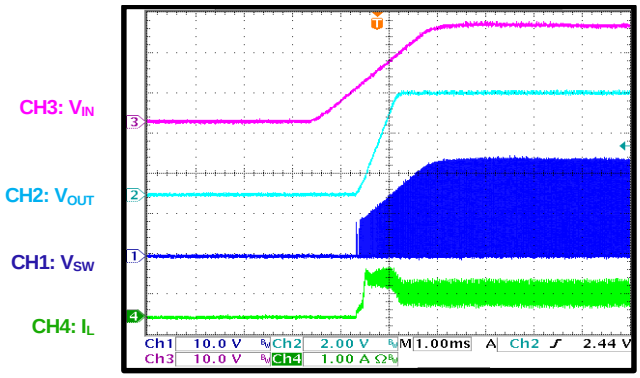
### Start-Up through VIN
$I_{OUT}$ = 0A, AAM



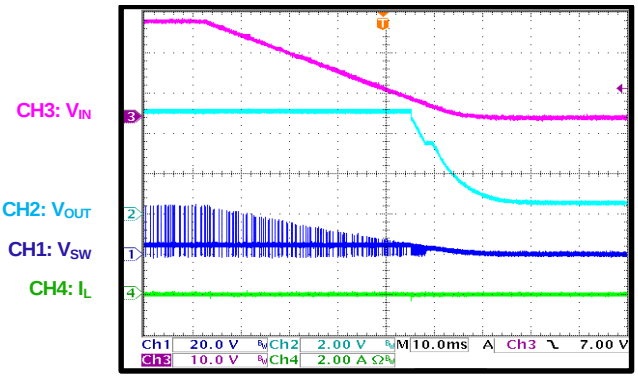

### Start-Up through VIN
$I_{OUT}$ = 0A, FCCM



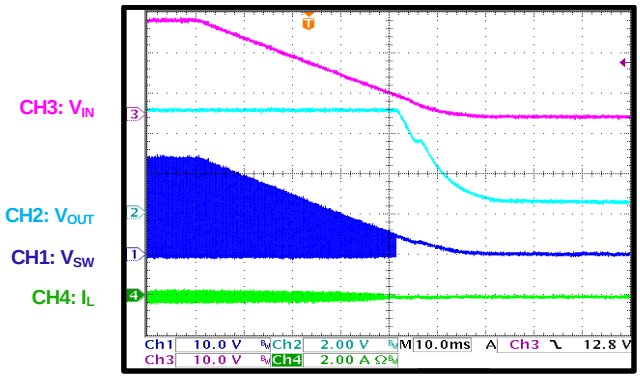

### Start-Up through VIN
$I_{OUT}$ = 600mA



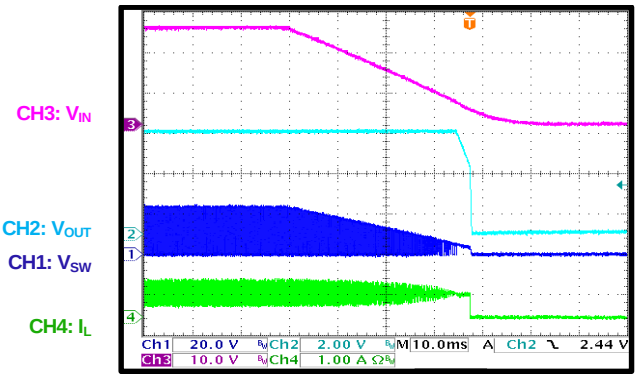

### Shutdown through VIN
$I_{OUT}$ = 0A, AAM




### Shutdown through VIN
$I_{OUT}$ = 0A, FCCM




### Shutdown through VIN
$I_{OUT}$ = 600mA





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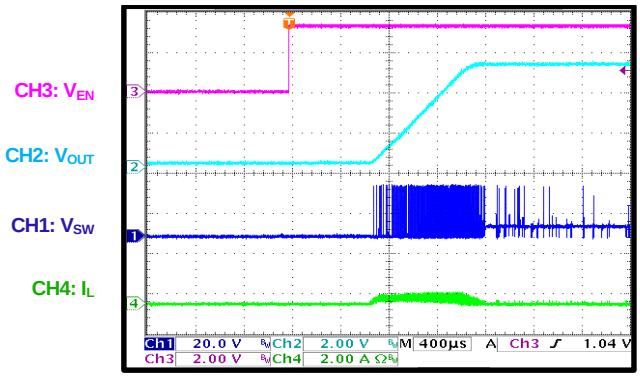
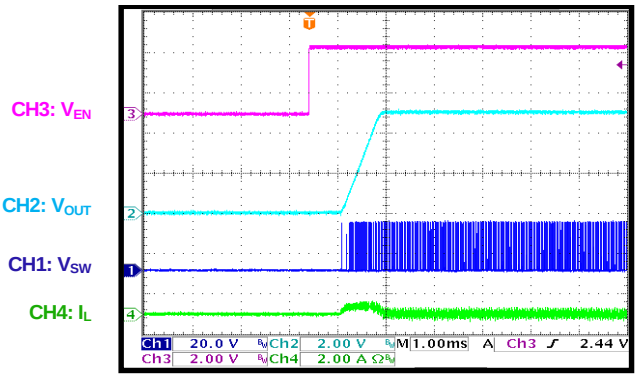
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, $T_A$ = 25°C, unless otherwise noted.**

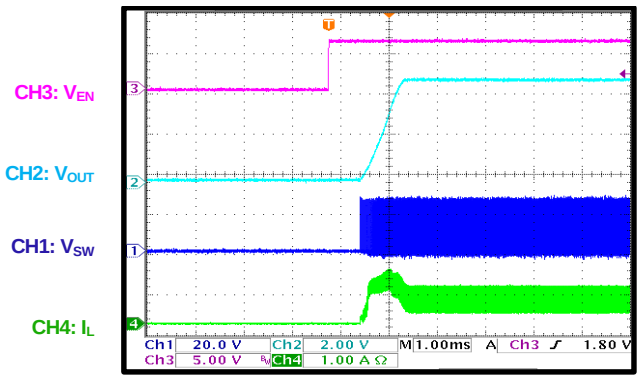
### Start-Up through EN
$I_{OUT}$ = 0A, AAM



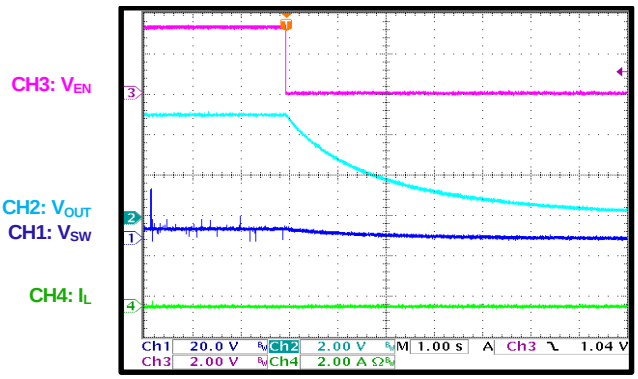

### Start-Up through EN
$I_{OUT}$ = 0A, FCCM



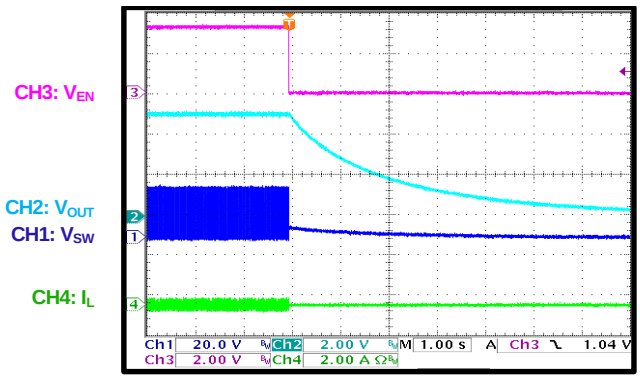

### Start-Up through EN
$I_{OUT}$ = 600mA



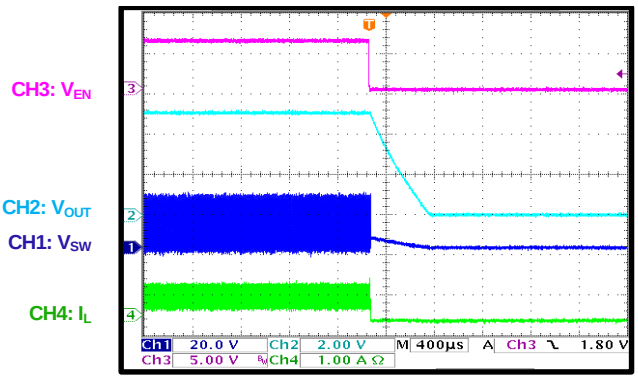

### Shutdown through EN
$I_{OUT}$ = 0A, AAM




### Shutdown through EN
$I_{OUT}$ = 0A, FCCM




### Shutdown through EN
$I_{OUT}$ = 600mA





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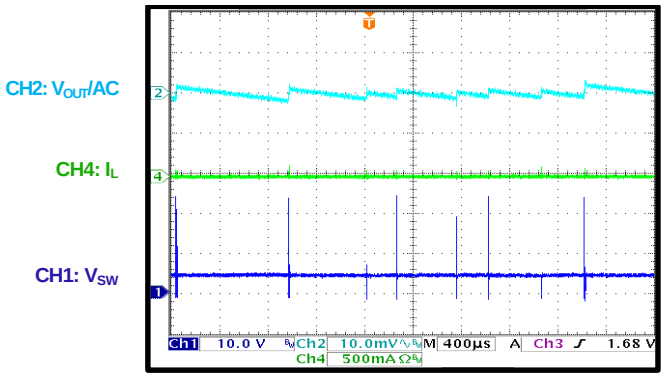
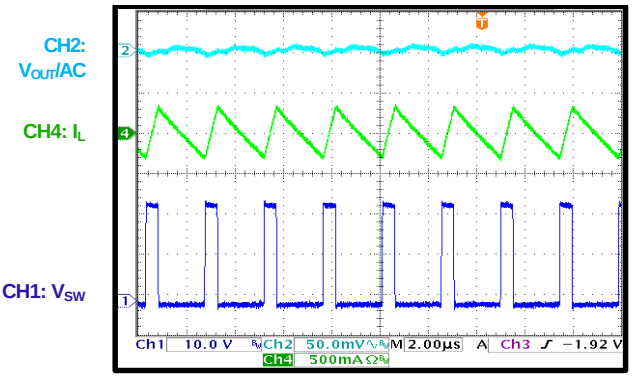
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, $T_A$ = 25°C, unless otherwise noted.**

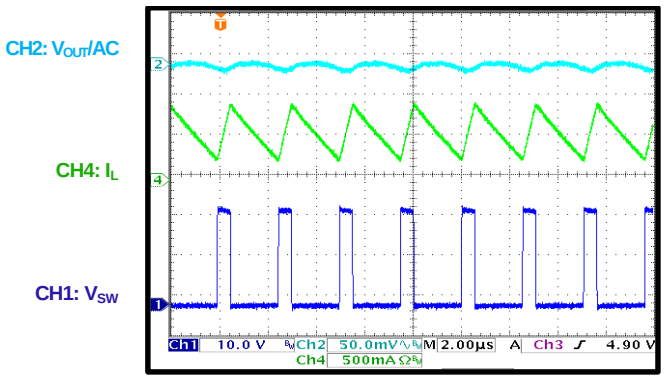
### Output Ripple
$I_{OUT}$ = 0A, AAM



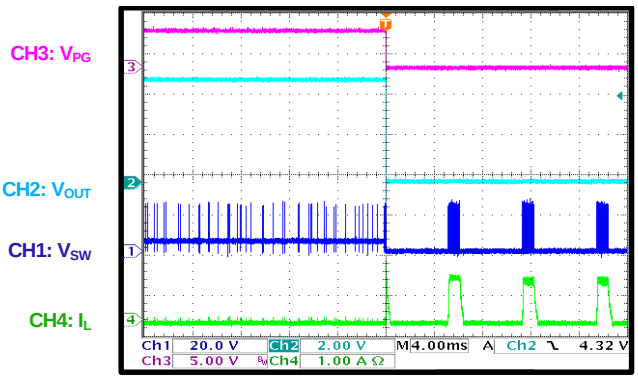

### Output Ripple
$I_{OUT}$ = 0A, FCCM



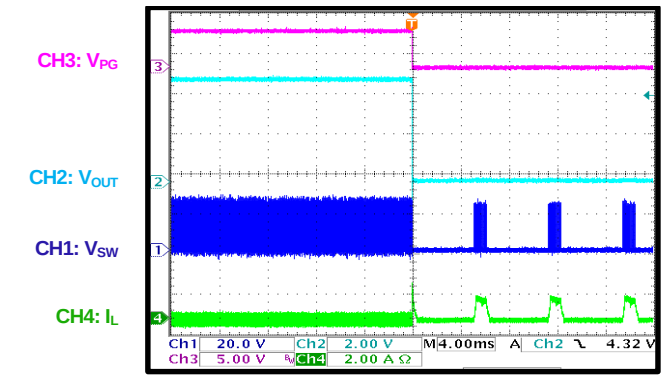

### Output Ripple
$I_{OUT}$ = 600mA



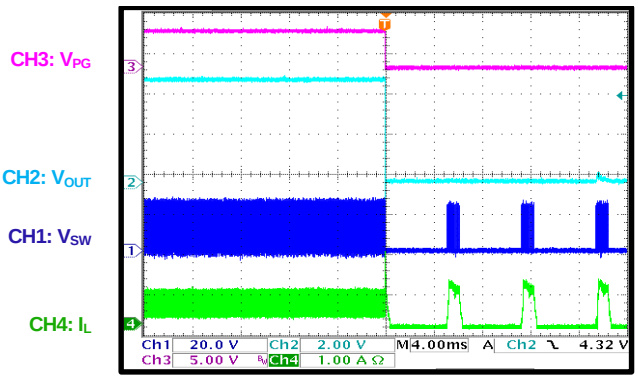

### Short-Circuit Protection (SCP) Entry
$I_{OUT}$ = 0A, AAM




### SCP Entry
$I_{OUT}$ = 0A, FCCM




### SCP Entry
$I_{OUT}$ = 600mA





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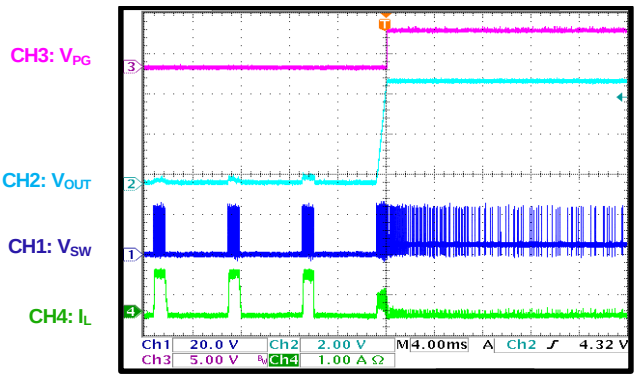
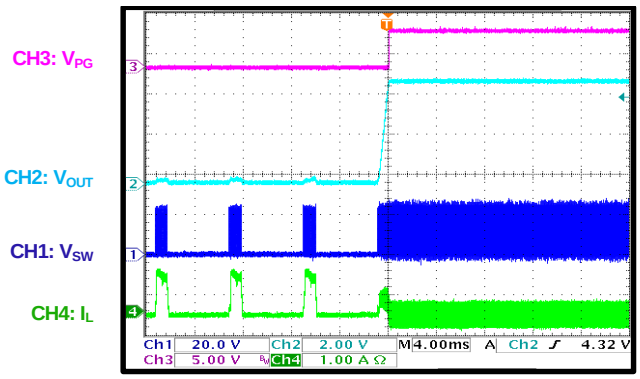
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, $T_A$ = 25°C, unless otherwise noted.**

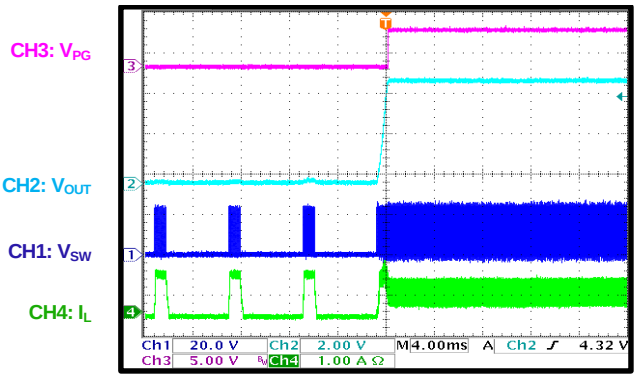
### SCP Recovery
$I_{OUT}$ = 0A, AAM



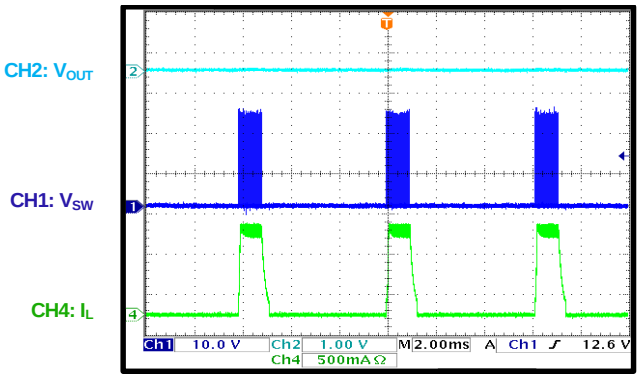

### SCP Recovery
$I_{OUT}$ = 0A, FCCM



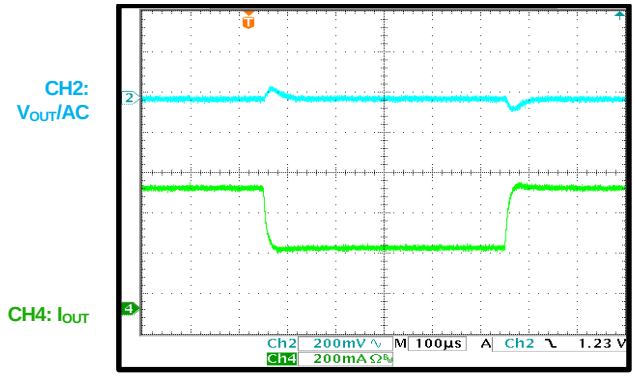

### SCP Recovery
$I_{OUT}$ = 600mA



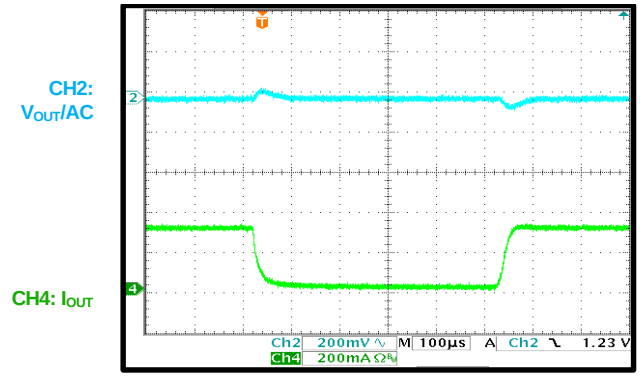

### SCP Steady State




### Load Transient
$I_{OUT}$ = 300mA to 600mA, AAM




### Load Transient
$I_{OUT}$ = 0mA to 300mA, AAM





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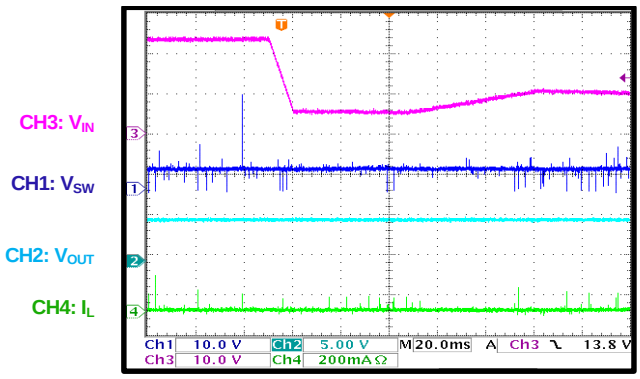
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, L = 15µH, $f_{SW}$ = 400kHz, $T_A$ = 25°C, unless otherwise noted.**

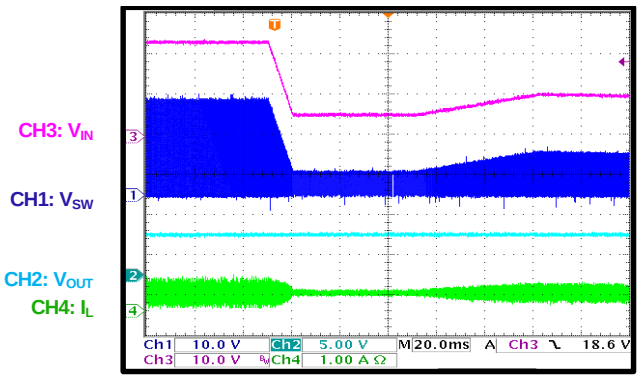
### Cold-Crank Conditions

$V_{IN}$ = 24V to 6V to 10V, $I_{OUT}$ = 0A



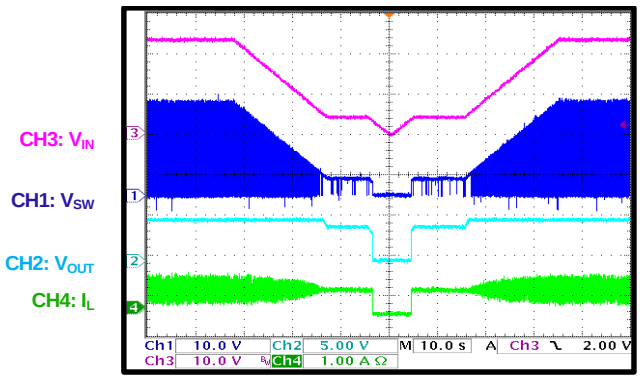

### Cold-Crank Conditions

$V_{IN}$ = 24V to 6V to 10V, $I_{OUT}$ = 600mA



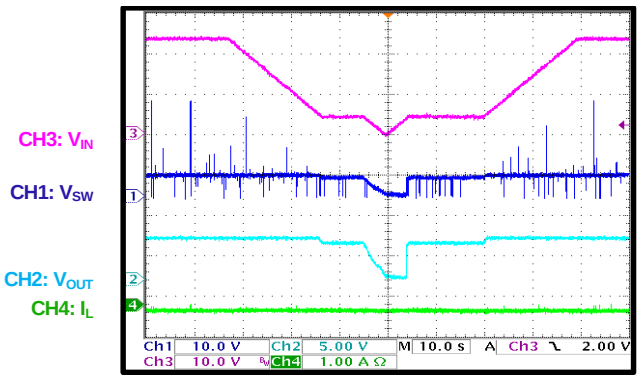

### $V_{IN}$ Ramp Down and Up

$V_{IN}$ = 18V to 4.5V to 0V to 4.5V to 18V,
$I_{OUT}$ = 0A



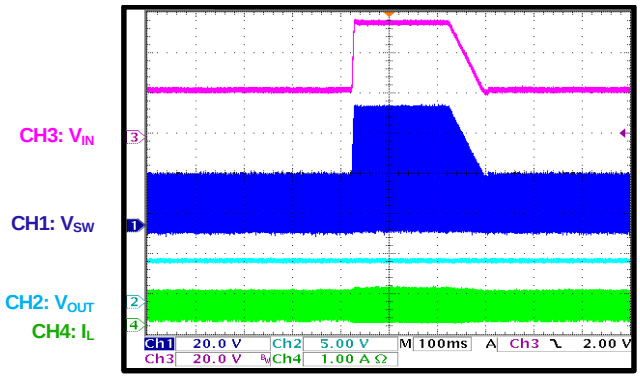

### $V_{IN}$ Ramp Down and Up

$V_{IN}$ = 18V to 4.5V to 0V to 4.5V to 18V,
$I_{OUT}$ = 600mA




### Load Dump

$V_{IN}$ = 24V to 58V to 24V, $I_{OUT}$ = 600mA





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## FUNCTIONAL BLOCK DIAGRAM

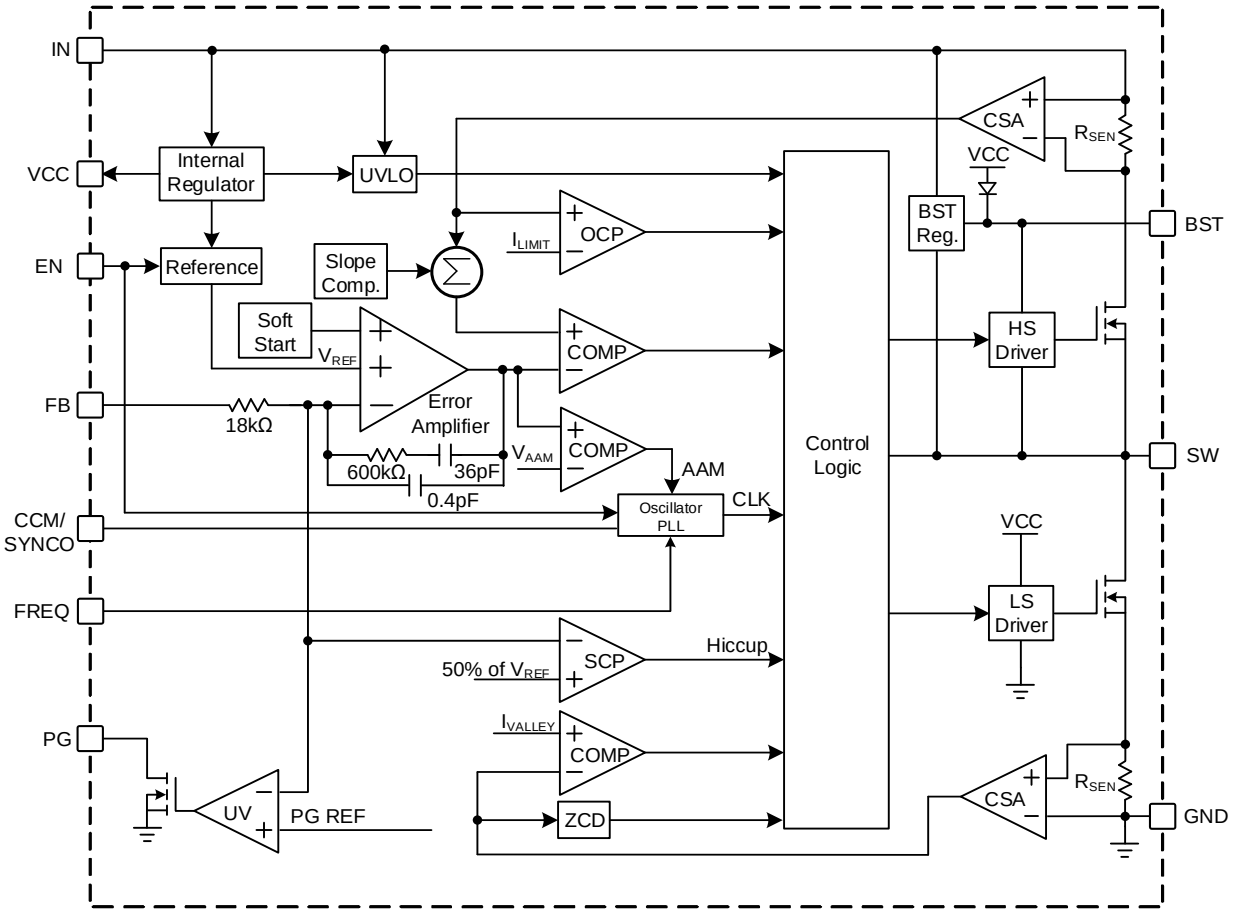


**Figure 1: Functional Block Diagram**


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# OPERATION

The MP4576 is a fully integrated, synchronous, rectified, non-isolated, step-down switch-mode converter. The device has a wide 4.5V to 60V input supply range, and can achieve up to 600mA of continuous output current. It achieves excellent load and line regulation across the -40°C to +125°C ambient temperature range.

### Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MP4576 operates in fixed-frequency, peak current control mode to regulate the output voltage.

An internal clock initiates a PWM cycle. At the rising edge of the clock, the high-side MOSFET (HS-FET) turns on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the value set by the COMP voltage ($V_{COMP}$), which is the output of the internal error amplifier. $V_{COMP}$ is based on the difference between the output feedback voltage and internal high-precision reference. $V_{COMP}$ determines how much energy should be transferred to the load. A higher load current leads to a higher $V_{COMP}$. Once the HS-FET is on, it remains on for at least 90ns.

When the HS-FET is off, the low-side switch (LS-FET) turns on immediately, and stays on until the next clock starts. During this time, the inductor current flows through the LS-FET. Once the LS-FET is on, it remains on for at least 100ns before the next cycle starts. To avoid shoot-through, a dead time is inserted to prevent the HS-FET and LS-FET from turning on simultaneously.

If the current in the HS-FET does not reach the value set by COMP within one PWM period, the HS-FET remains on, saving a turn-off operation.

### Light-Load Operation

The MP4576 features configurable forced continuous conduction mode (FCCM) and light-load advanced asynchronous mode (AAM), which can be set by the CCM/SYNCO pin. FCCM maintains a constant switching frequency and smaller output ripple. However, FCCM has lower efficiency under light-load conditions, when compared with AAM (see Figure 2).

To force the device into FCCM, connect the CCM/SYNCO pin to GND using a 10kΩ to 300kΩ resistor. In FCCM, the converter works with a fixed frequency across a no-load to full-load range. Float the CCM/SYNCO pin to force the device into AAM under light-load conditions. The device cannot change modes while it is operating, so the mode must be selected before start-up.

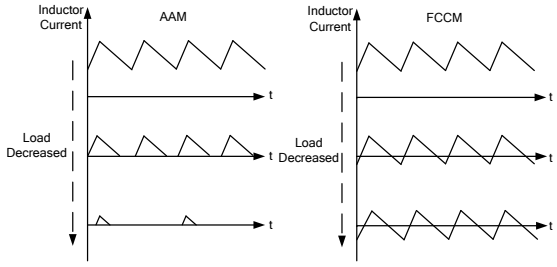


**Figure 2: AAM and FCCM**

When AAM is enabled, the switching frequency is scaled down according to $V_{COMP}$ during light-load conditions. The MP4576 first enters non-synchronous operation while the inductor current approaches zero at light-load. If the load further decreases or is at no-load, $V_{COMP}$ drops below the internally set AAM value ($V_{AAM}$). The MP4576 then enters sleep mode and consumes a low quiescent current to improve light-load efficiency.

In sleep mode, the internal clock is blocked, so the MP4576 skips some pulses. $V_{FB}$ is below $V_{REF}$, so $V_{COMP}$ ramps up until it exceeds $V_{AAM}$. Then the internal clock is reset and the crossover time is used as a benchmark for the next clock. This control scheme helps the device achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As the output current increases from light loads, both $V_{COMP}$ and the switching frequency rise. If the output current exceeds the critical level set by $V_{COMP}$, the MP4576 enters discontinuous conduction mode (DCM) or CCM, which have a constant switching frequency.

### Enable (EN) Control

The MP4576 can be enabled or disabled via a remote EN signal that is referenced to ground. The remote EN control operates with a positive logic that is compatible with common logic devices. A positive logic indicates that when the input voltage exceeds the under-voltage lockout (UVLO) threshold (about 4.0V), the converter is enabled by pulling the EN pin above 1.45V.


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Drive the EN pin below 1.12V to disable the MP4576. An internal resistor ($R_{EN}$) connected from EN to GND allows EN to be floated to shut down the chip ($R_{EN}$ = 2.8MΩ when EN is on; $R_{EN}$ = 1.8MΩ when EN is off).

### SYNC Out (SYNCO)

The MP4576 has a SYNCO pin. During start-up, SYNCO stays low and quickly outputs a 180° phase-shift clock to the internal oscillator once soft start is ready. Note that the falling edge of SYNCO is a 180° phase shift to the rising edge of the internal oscillator. This function allows two devices to operate at the same frequency, but 180° out of phase, which reduces the total input current ripple. This allows a smaller input bypass capacitor to be used.

### Internal Regulator

A 4.9V internal regulator powers most of the internal circuitries. This regulator takes $V_{IN}$ and operates in the full $V_{IN}$ range. When $V_{IN}$ exceeds 4.9V, the output of the regulator is in full regulation. Lower $V_{IN}$ values result in lower output voltages. The regulator is enabled when $V_{IN}$ exceeds its UVLO threshold and EN is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

### Configurable Frequency and Foldback

The oscillating frequency ($f_{SW}$) of the MP4576 is configured by an external frequency resistor. The frequency resistor ($R_{FREQ}$) should be placed between the FREQ pin and GND, as close as possible to the device. Calculate $R_{FREQ}$ with Equation (1):

$$R_{FREQ}(M\Omega) = \frac{30}{f_{sw}(kHz)} \quad (1)$$

The calculated resistance may need fine-tuning with a bench test.

It is not possible to have a high $f_{SW}$ with a high $V_{IN}$, since the minimum on time required for the HS-FET is limited. The MP4576 control loop automatically sets the maximum possible $f_{SW}$ up to the set frequency, which also reduces excessive power loss in the IC. $V_{OUT}$ is regulated by varying the duration of the HS-FET's switch-off time, which results in an automatic reduction of $f_{SW}$.

The MP4576 complies with the HS-FET's minimum on time. An advantage of this method is that the device works at a constant $f_{SW}$ as long as possible, and is only changed at high input voltages. For more details, see the $f_{SW}$ vs. $V_{IN}$ curve on page 12, where $R_{FREQ}$ equals 12.1kΩ.

Table 1 shows the relationship between the oscillator frequency and $R_{FREQ}$.

**Table 1: $f_{SW}$ vs. $R_{FREQ}$**

| $R_{FREQ}$ (kΩ) | $f_{SW}$ (kHz) | $R_{FREQ}$ (kΩ) | $f_{SW}$ (kHz) |
|---|---|---|---|
| 100 | 300 | 24.3 | 1150 |
| 91.9 | 330 | 22 | 1250 |
| 82.5 | 360 | 20 | 1350 |
| 76.8 | 400 | 18.2 | 1500 |
| 68.1 | 430 | 16.2 | 1650 |
| 61.9 | 475 | 15 | 1750 |
| 56 | 520 | 14 | 1900 |
| 47 | 600 | 13 | 2050 |
| 39 | 700 | 12.1 | 2200 |
| 34.8 | 800 | 11.5 | 2250 |
| 30 | 940 | 11 | 2350 |
| 28 | 1000 | 10 | 2500 |

### Internal Soft Start (SS)

To avoid overshoot during start-up, the MP4576 has built-in soft start (SS) that ramps up the output voltage at a controlled slew rate when the EN pin goes high. When the SS voltage ($V_{SS}$) is below the internal reference ($V_{REF}$), $V_{SS}$ overrides $V_{REF}$ as the error amplifier reference. When $V_{SS}$ exceeds $V_{REF}$, $V_{REF}$ acts as the reference. At this point, soft start finishes, and the MP4576 enters steady state operation.

The SS time is internally set to 0.45ms. When the output voltage is shorted to GND, the feedback voltage is pulled low, then $V_{SS}$ is discharged. The MP4576 initiates another soft start when it returns to the normal state.

### Pre-Biased Start-Up

If $V_{FB}$ exceeds $V_{SS}$ during start-up, the output has a pre-biased voltage, and neither the HS-FET nor LS-FET turn on until $V_{SS}$ exceeds $V_{FB}$. Note that this function is only available when the device is set to AAM.


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### Power Good (PG) Indicator

The MP4576 has power good (PG) indication. The PG pin is the open drain of a MOSFET. PG should be connected to a voltage source through a resistor (e.g. 100kΩ). When an input voltage is present, the MOSFET turns on so that the PG pin is pulled to GND before soft start is ready. PG goes high if the output voltage is within 90% to 108% of the nominal voltage after a 70μs delay. PG goes low when the output voltage is above 116% or below 84% of the nominal voltage after a 25μs delay.

### Under-Voltage Lockout (UVLO)

The MP4576 has input under-voltage lockout (UVLO) to ensure reliable output power. Assuming EN is active, the MP4576 starts up when the input voltage exceeds the UVLO rising threshold. The device shuts down when the input voltage drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient voltage. UVLO is a non-latch protection.

### Over-Current Protection (OCP)

The MP4576 has a 1.7A peak current limit. Once the inductor current reaches the current limit, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor current drops below a current threshold (the valley current limit). This protection prevents the inductor current from rising too high and damaging the components.

### Short-Circuit Protection (SCP)

If a short-circuit condition occurs, the MP4576 reaches its current limit immediately. Meanwhile, the output voltage drops until $V_{FB}$ falls below 50% of $V_{REF}$. The device considers this an output dead short, and triggers hiccup short-circuit protection (SCP) to periodically restart the part.

In hiccup mode, the MP4576 disables its output power stage, slowly discharges the soft-start capacitor, then initiates a soft start. If the short-circuit condition remains after soft start ends, the device repeats this operation until the short circuit disappears and the output returns to the regulation level. This protection greatly reduces the average short-circuit current to alleviate thermal issues and protect the regulator.

### Negative Current Protection

The MP4576 has a -1.3A negative current limit. If the inductor current reaches the current limit, the LS-FET immediately turns off and the HS-FET turns on. The current limit prevents the negative current from dropping too low and damaging the components.

### Thermal Shutdown

For thermal protection, the MP4576 monitors the IC temperature internally. Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the junction temperature exceeds the threshold value (about 170°C), the whole chip shuts down. This is a non-latch protection. There is a 25°C hysteresis. Once the junction temperature drops to about 145°C, the device resumes normal operation by initiating a soft start.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating HS-FET driver. There are two methods to charge the bootstrap capacitor (see Figure 3).

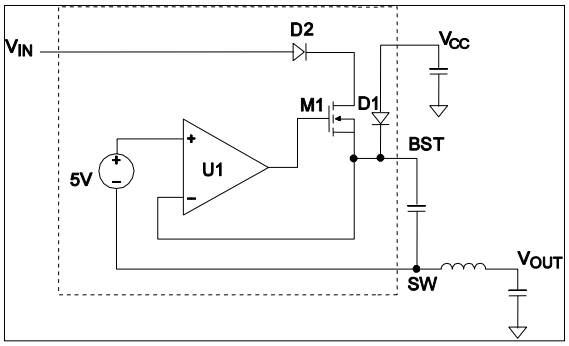


**Figure 3: Internal Bootstrap Charging Circuit**

The first method is through the main charging circuit from VCC through a diode. When the HS-FET is on, $V_{SW}$ is about equal to $V_{IN}$ but exceeds $V_{CC}$, and the bootstrap capacitor is not charged. The optimal charging period occurs when the LS-FET is on, and the difference between $V_{CC}$ and $V_{SW}$ is at its greatest. When there is no current in the inductor, $V_{SW}$ equals $V_{OUT}$, so $V_{CC}$ can only charge the BST capacitor when $V_{OUT}$ is small.

The second method is through the auxiliary charging circuit from VIN. When the voltage difference between BST and SW is below the internal 5V bootstrap regulator, a P-channel


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MOSET pass transistor (M1) turns on to charge the bootstrap capacitor. The charging current is much smaller than that from VCC, but as long as $V_{IN}$ exceeds $V_{SW}$, the BST capacitor can be charged. This function is useful in sleep mode, when there is not always a switch.

### Low-Dropout Operation (BST Refresh)

To improve dropout, the MP4576 is designed to operate at close to 100% duty cycle as long as the BST-to-SW voltage exceeds 1.4V. When the BST-to-SW voltage drops below 1.34V, the HS-FET turns off using a UVLO circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. When the input voltage drops close to the output voltage, the HS-FET remains on and close to 100% duty cycle to maintain output regulation, until the BST-to-SW voltage falls below 1.34V.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. The means the effective duty cycle of the switching regulator is high.

The effective duty cycle during regulator dropout is mostly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

### Start-Up and Shutdown

If both $V_{IN}$ and $V_{EN}$ exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank the start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure the circuitries are ready, and then slowly ramps up.

Three events can shut down the chip: EN going low, $V_{IN}$ UVLO, and thermal shutdown. During shutdown, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.


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# APPLICATION INFORMATION

## Setting the Output Voltage

The external resistor divider connected to the FB pin sets the output voltage. The feedback resistor (R1) must account for both stability and dynamic response, so it cannot be too large or too small. Choose R1 value to be about 40kΩ. R2 can be estimated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8} - 1} \quad (2)$$

Figure 4 shows the recommended T-type feedback network.

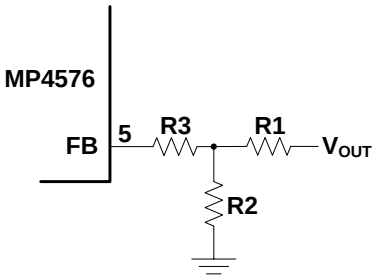


**Figure 4: Feedback Network**

R3 + R1 sets the loop bandwidth. A higher R3 + R1 indicates a lower bandwidth. To ensure loop stability, it is strongly recommended to limit the bandwidth below 1/10 of the switching frequency. The bandwidth should not exceed 100kHz.

The calculated resistance may need fine-tuning via bench testing. Table 1 lists the recommended feedback resistor divider values for common output voltages. Use check loop analysis before using the device in an application, and change the resistance of R3 for loop stability if required.

**Table 1: Resistor Values for Typical $V_{OUT}$**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | R3 (kΩ) |
|---|---|---|---|
| 3.3 | 41.2 | 13 | 20 |
| 5.0 | 41.2 | 7.68 | 20 |
| 8 | 41.2 | 4.53 | 20 |
| 12 | 41.2 | 2.98 | 20 |

## Selecting the Inductor

The inductor must supply constant current to the output load while being driven by the switching input voltage. For the highest efficiency, choose an inductor with a low DC resistance. A higher-value inductor results in less ripple current and a lower output voltage ripple. However, a higher-value inductor results in a physically larger inductor, higher series resistance, and lower saturation current.

A good rule to determine the ideal inductance is to make the inductor ripple current approximately 30% of the maximum load current. Ensure that the peak inductor current is below the device's peak current limit. The inductance can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where $\Delta I_L$ is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. Calculate the peak inductor current with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

## Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended because of their low ESR and small temperature coefficients. Other capacitors, such as Y5V and Z5U, should not be used since they lose too much capacitance with frequency, temperature, and bias voltage changes.

Place the input capacitors as close to the IN pin as possible. For most applications, a 22µF capacitor is sufficient. For higher output voltages, use a 47µF capacitor to improve system stability. To maintain a small solution size, choose a capacitor that has a voltage rating compliant with the input spec.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating that should not exceed the converter's maximum input ripple current.


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The input current ripple can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality ceramic capacitor (0.1μF), placed as close to the IC as possible. The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system design, choose an input capacitor that meets the specification.

The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

### Selecting the Output Capacitor

The output capacitor maintains the output DC voltage. Ceramic capacitors with low ESR are recommended due to their small size and low output voltage ripple. Electrolytic and polymer capacitors may also be used. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

Where $R_{ESR}$ is the equivalent series resistance of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When selecting an output capacitor, consider the allowable overshoot in $V_{OUT}$ if the load is suddenly removed. In this case, energy stored in the inductor is transferred to $C_{OUT}$, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, the output capacitance can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where $V_{OUTMAX} / V_{OUT}$ is the allowable maximum overshoot.

After calculating the capacitance required for both the ripple and overshoot specifications, choose the higher-value capacitor between the two values.

The characteristics of the output capacitor also affect the stability of the regulation system. The MP4576 can be optimized for a wide range of capacitance and ESR values.

### $V_{IN}$ Under-Voltage Lockout (UVLO) Setting

The MP4576 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 4.0V, while the falling threshold is about 3.5V. For applications that require a higher UVLO point, place an external resistor divider between the EN and IN pins to obtain a higher equivalent UVLO threshold. Add a 6V Zener diode between EN and GND if the EN pin is connected to the input through a resistor.

Figure 5 shows how to adjust the UVLO threshold when EN is rising.


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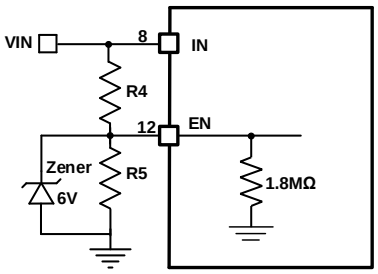


**Figure 5: Adjustable UVLO Using EN Divider when EN Rises**

Figure 6 shows how to adjust the UVLO threshold when EN is falling.

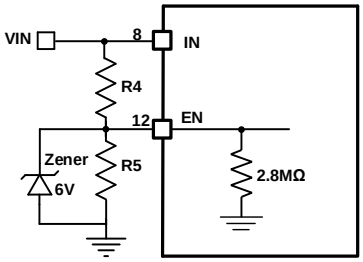


**Figure 6: Adjustable UVLO Using EN Divider when EN Falling**

The UVLO threshold can be calculated with Equation (13) and Equation (14) when EN is rising or falling, respectively:

$$INUV_{RISING} = (1+\frac{R4}{1.8M//R5}) \times V_{EN_RISING} \quad (13)$$

$$INUV_{FALLING} = (1+\frac{R4}{2.8M//R5}) \times V_{EN_FALLING} \quad (14)$$

Where $V_{EN_RISING}$ = 1.45V, $V_{EN_FALLING}$ = 1.12V.

When choosing R4, ensure that it can limit the current flowing into EN pin below 100μA.

### Selecting the BST Resistor and Capacitor

Place a resistor ($R_{BST}$) in series with the BST capacitor to reduce the SW rising rate and voltage spikes. This enhances EMI performance and reduces voltage stress at high input voltages. A higher resistance reduces SW spikes but compromises efficiency. To make a tradeoff between EMI and efficiency, it is recommended to keep $R_{BST}$ below 20Ω. The recommended BST capacitor value is between 0.1μF and 1μF.


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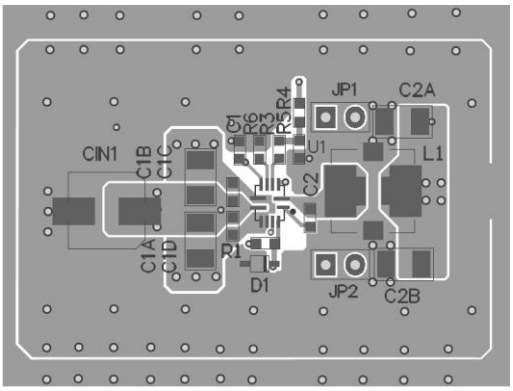
## PCB Layout Guidelines (11)

An optimized PCB layout is very important for proper operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 7 and follow the guidelines below:

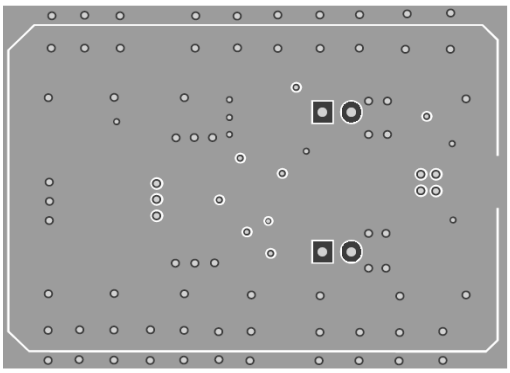
1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to the IN and GND pins as possible to minimize high-frequency noise.
4. Place the T-type feedback resistors as close as possible to the FB pin. Ensure that the trace connected to the FB pin is as short as possible.
5. Route SW and BST away from sensitive analog areas, such as FB.
6. Use multiple vias to connect the power planes to the internal layer.

**Note:**

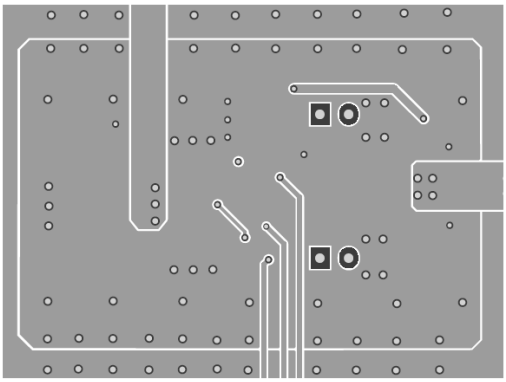
11) The recommended PCB layout is based on the circuit in Figure 8.



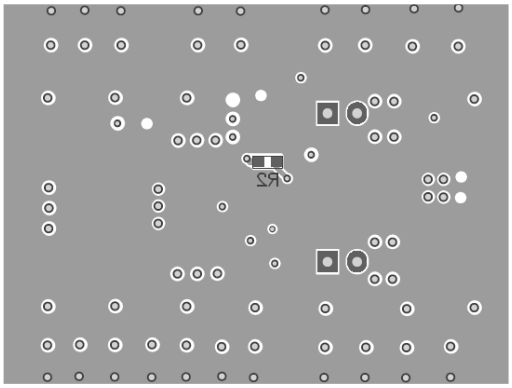

**Top Silk and Top Layer**



**Mid-Layer 1**



**Mid-Layer 2**



**Bottom Layer and Bottom Silk**

**Figure 7: Recommended PCB Layout**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# TYPICAL APPLICATION CIRCUITS

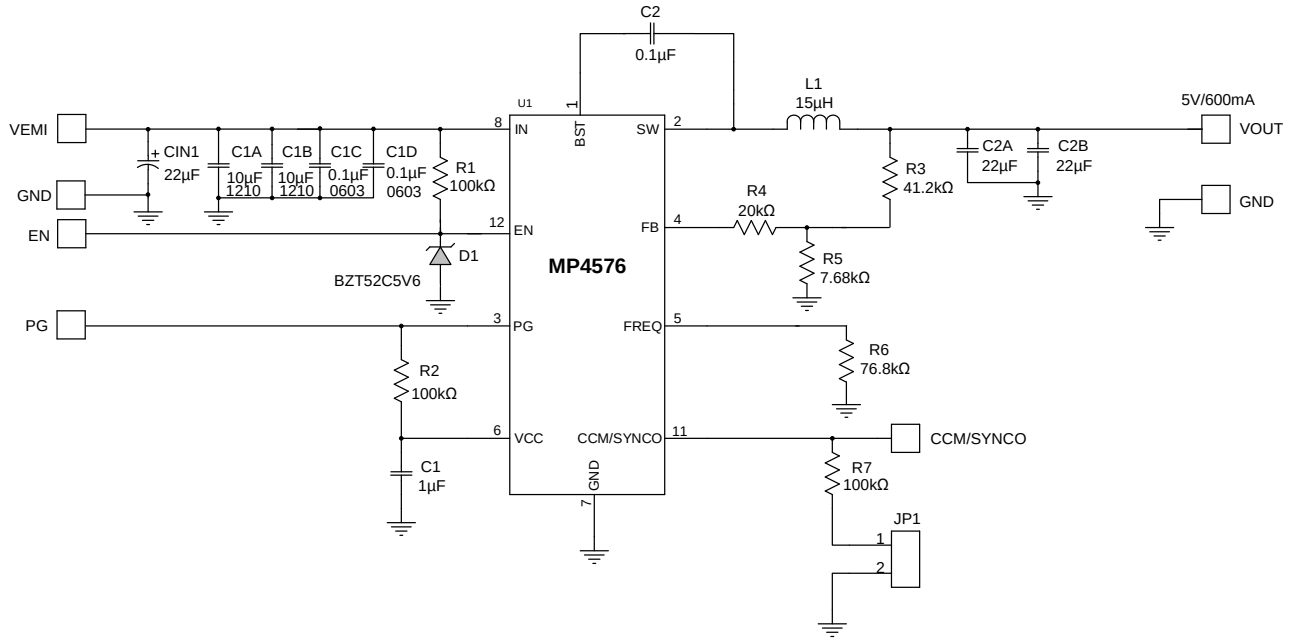


**Figure 8: Typical Application Circuit**

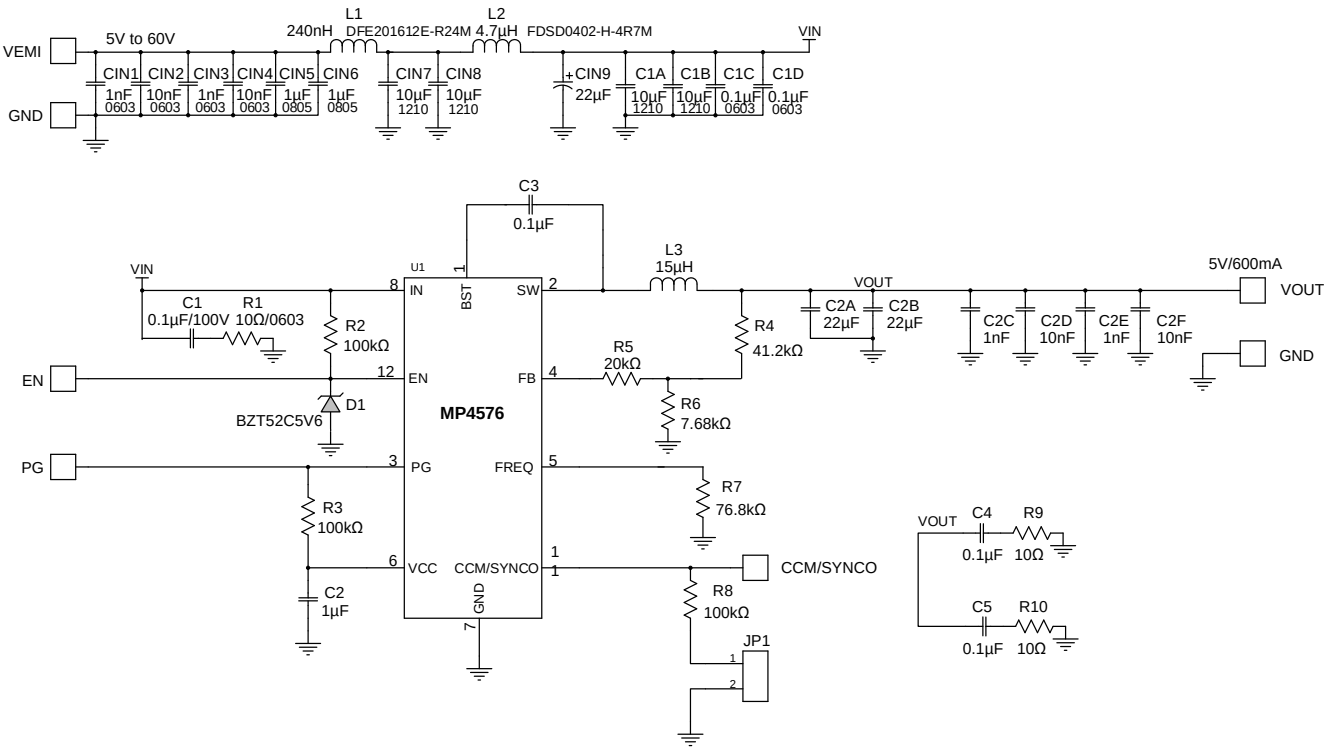


**Figure 9: Typical Application Circuit with EMI Filters**


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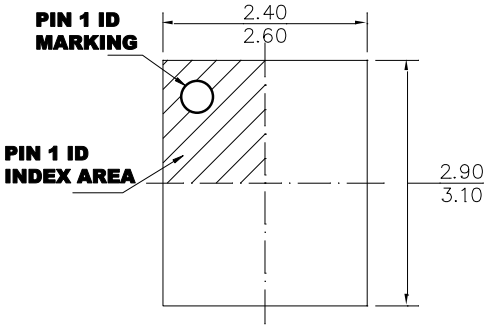
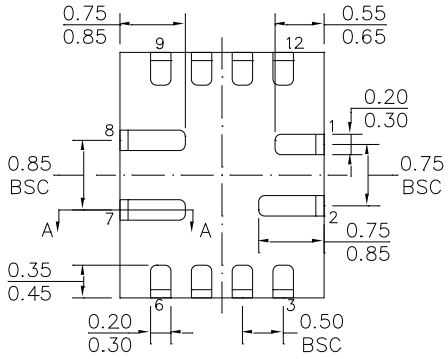
# PACKAGE INFORMATION

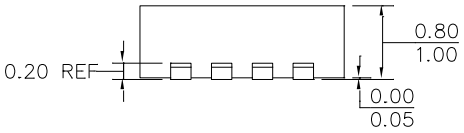
## QFN-12 (2.5mmx3mm)
### Wettable Flank



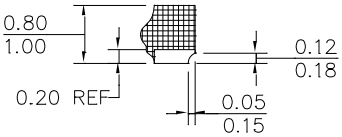

**TOP VIEW**



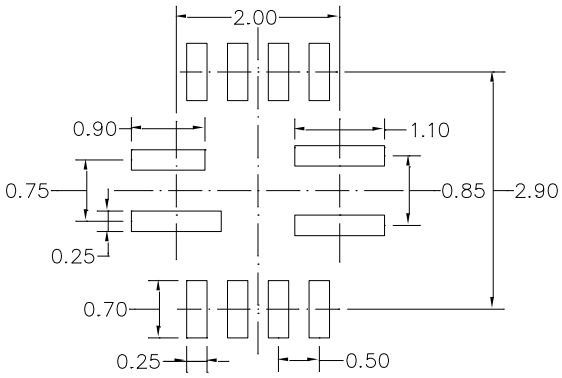

**BOTTOM VIEW**




**SIDE VIEW**




**SECTION A-A**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) THE LEAD SIDE IS WETTABLE.
2) LAND PATTERNS OF PINS 2, 7, AND 8 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.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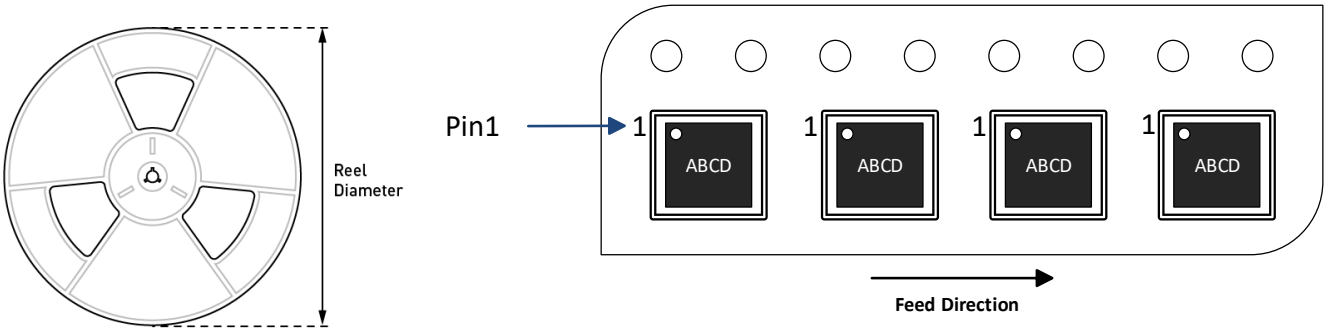
## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MP4576GQBE-Z | QFN-12 (2.5mmx3mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm |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## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 07/07/2021 | Initial Release | - |

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