# MP2338

## High-Efficiency, 28V, 3A, 450kHz, Synchronous Step-Down Converter In SOT583 Package

## DESCRIPTION

The MP2338 is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve 3A of continuous output current across a wide input range, with excellent load and line regulation. The MP2338 has synchronous mode operation for high efficiency across the wide output current load range.

Constant-on-time (COT) control provides very fast transient response and easy loop design, as well as tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP2338 requires a minimal number of readily available, standard external components. It is available in a space-saving SOT583 package.

## FEATURES

- Wide 4.5V to 28V Operating Input Range
- Wide 0.5V to 16V $V_{OUT}$
- ±1.5% Internal Reference Accuracy Over-Temperature
- 115mΩ/55mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 160μA Quiescent Current
- >90% Efficiency for 24V to 5V/3A Condition
- Power Save Mode at Light Load
- Fast Load Transient Response
- 450kHz Switching Frequency
- $t_{ON}$ Extension to Improve Dropout
- Configurable Soft-Start Time
- Power Good Indication
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown Protection
- Available in an SOT583 Package

MPL Optimized Performance with MPS Inductor MPL-AL Series

## APPLICATIONS

- Game Consoles
- Multi-Function Printers
- Power Meters
- Flat Panel Televisions and Monitors
- General-Purpose Power Supplies

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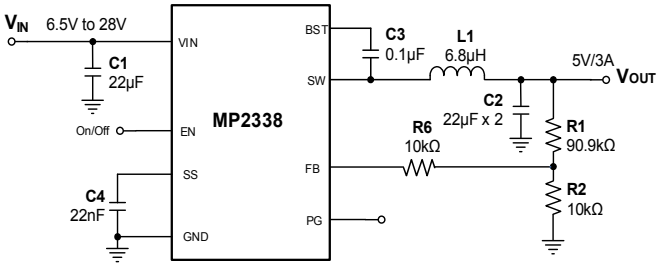
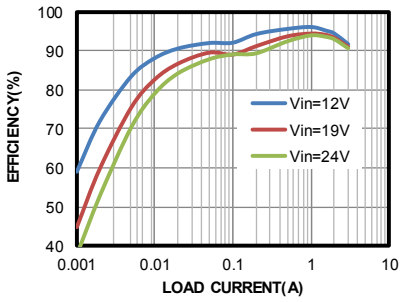
## TYPICAL APPLICATION




**Efficiency**

$V_{OUT}$ = 5V, L = 6.8μH, DCR = 16mΩ





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP2338GTL | SOT583 | *See Below* | 1 |

* For Tape & Reel, add suffix –Z (e.g. MP2338GTL–Z).

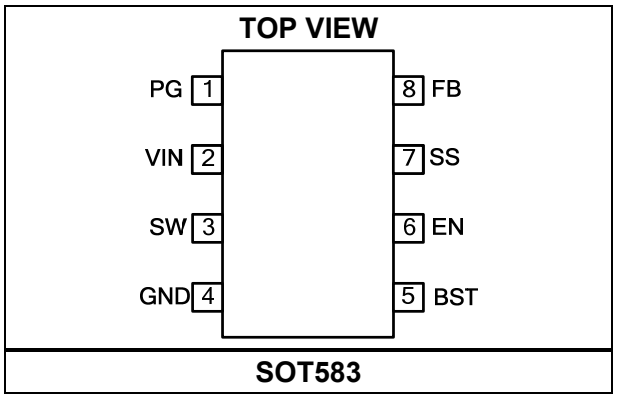
## TOP MARKING

BLPY

LLL

BLP: Product code of MP2338GTL
Y: Year code
LLL: Lot number

## PACKAGE REFERENCE





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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | PG | **Power good output**. This pin is an open-drain output. PG pulls low when the IC is disabled. PG can be pulled up to another DC source. Note that if PG is pulled up to an external voltage, PG does not de-assert (logic low) if the input power is off. It is recommended to pull PG up to $V_{OUT}$ so that PG can de-assert when the input power is off. |
| 2 | VIN | **Supply voltage**. The MP2338 operates from a 4.5V to 28V input rail. Place a ceramic capacitor on VIN to decouple the input rail. Connect VIN using a wide PCB trace. |
| 3 | SW | **Switch output**. Connect SW using a wide PCB trace. |
| 4 | GND | **System ground**. Reference ground of the regulated output voltage. GND requires additional considerations when designing the PCB layout. Connect GND with copper traces and vias. |
| 5 | BST | **Bootstrap.** Connect a capacitor between the SW and BST pins to form a floating supply across the high-side switch driver. Generally, use a 0.1μF bootstrap capacitor. |
| 6 | EN | **Enable pin**. EN is a digital input that turns the buck converter on or off. When the power supply of the control circuit is ready, drive EN high to turn the buck converter on. Drive EN low to turn the converter off. Connect EN to VIN through a resistive voltage divider for automatic start-up. The EN voltage should not exceed 6V. |
| 7 | SS | **Soft start**. Connect an external capacitor to SS to configure the soft-start time for the switch-mode converter. |
| 8 | FB | **Feedback**. Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. |


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## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ ..... -0.3V to +30V
$V_{SW}$ .....
-0.3V (-5V for <10ns) to +30V (+32V for <10ns)
$V_{BST}$ ..... $V_{SW}$ + 5.5V
All other pins ..... -0.3V to +6V
PG pin current ..... 5mA (2)
Continuous power dissipation ($T_A$ = 25°C) (3)
..... 2.27W (5)
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

### *ESD Ratings*

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

### *Recommended Operating Conditions* (4)

Supply voltage ($V_{IN}$) ..... 4.5V to 28V
Output voltage ($V_{OUT}$) .....
.....0.5V to 0.95 x $V_{IN}$ or 16V Max
Operating junction temp ($T_J$).....-40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| SOT583 | | |
| EVL2338-TL-00A (5) | 55 | 21 °C/W |
| JESD51-7 (6) | 130 | 60 °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) When the PG pin is pulled up to the power source, the current should be limited to be below the maximum value.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EVL2338-TL-00A, 2-layer, 63.5mmx63.5mm PCB.
6) The value of $\theta_{JA}$ given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C [7], typical values are tested at $T_J$ = 25°C, unless otherwise noted. The over-temperature limit is derived by characterization, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| VIN under-voltage lockout threshold | $VIN_{UVLO-R}$ | $V_{IN}$ rising, $V_{EN}$ = 2V | 3.66 | 3.96 | 4.25 | V |
| VIN under-voltage lockout hysteresis | $VIN_{UVLO-HYS}$ | | | 330 | | mV |
| Shutdown supply current | $I_{SD}$ | $V_{EN}$ = 0V | | 2 | 10 | μA |
| Quiescent supply current | $I_Q$ | $V_{EN}$ = 2V, $V_{FB}$ = 0.55V | | 160 | 250 | μA |
| **Enable Control** | | | | | | |
| EN rising threshold | $V_{EN-RISE}$ | | 1.1 | 1.2 | 1.3 | V |
| EN hysteresis | $V_{EN-HYS}$ | | | 120 | | mV |
| EN input current | $I_{EN}$ | $V_{EN}$ = 2V | | 2 | 10 | μA |
| **Power Switch** | | | | | | |
| High-side switch on resistance | $HS_{RDS(ON)}$ | $V_{BST-SW}$ = 5V | | 115 | | mΩ |
| Low-side switch on resistance | $LS_{RDS(ON)}$ | | | 55 | | mΩ |
| Switch leakage | $SW_{LKG}$ | $V_{EN}$ = 0V， $V_{IN}$ = 24V, SW short to VIN | | | 1 | μA |
| **Current Limit** | | | | | | |
| Low-side switching valley current limit | $I_{LIMIT-LS-OC}$ | | 2.9 | 3.75 | 4.6 | A |
| ZCD | $I_{ZCD}$ | $V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8μH | 0 | 50 | 200 | mA |
| **Frequency** | | | | | | |
| Oscillator frequency | $f_{SW}$ | $V_{IN}$ = 12V,$V_{OUT}$ = 5V, $I_{OUT}$ = 1.5A | 350 | 450 | 550 | kHz |
| Minimum on time [8] | $t_{ON-MIN}$ | | | 50 | | ns |
| Minimum off time [8] | $t_{OFF-MIN}$ | | | 160 | | ns |
| **Feedback Control** | | | | | | |
| Feedback voltage | $V_{REF}$ | $T_J$ = 25°C | 495 | 500 | 505 | mV |
| | | $T_J$ = -40°C to +125°C | 492.5 | 500 | 507.5 | mV |
| Feedback current | $I_{FB}$ | $V_{FB}$ = 0.52V | | 10 | 50 | nA |
| Soft-start current | $I_{SS}$ | | 5.5 | 7.5 | 9.5 | μA |


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## ELECTRICAL CHARACTERISTICS (*continued*)

**$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C [7], typical values are tested at $T_J$ = 25°C, unless otherwise noted. The over-temperature limit is derived by characterization, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **PG Indicator** | | | | | | |
| Power good lower trip rising threshold | $PG_{LOWER-R}$ | PG from low to high | 85 | 90 | 95 | % of $V_{REF}$ |
| Power good lower trip falling threshold | $PG_{LOWER-F}$ | PG from high to low | 79 | 84 | 89 | % of $V_{REF}$ |
| Power good upper trip rising threshold | $PG_{UPPER-F}$ | PG from high to low | 107 | 112 | 117 | % of $V_{REF}$ |
| Power good upper trip falling threshold | $PG_{UPPER-R}$ | PG from low to high | 101 | 106 | 111 | % of $V_{REF}$ |
| Power good rising delay | | | | 12 | | µs |
| Power good falling delay | | | | 20 | | µs |
| Power good sink current capability | $V_{PG}$ | Sink 4mA | | | 0.4 | V |
| Power good leakage current | $I_{PG-LKG}$ | $V_{IN}$ = 12V, $V_{EN}$ = 2V, $V_{FB}$ = 0.52V, $V_{PG}$ = 5V | | 2 | 10 | µA |
| **Protection** | | | | | | |
| FB under-voltage threshold | | | 40 | 50 | 60 | % of $V_{REF}$ |
| Hiccup protection duty cycle [8] | | | | 25 | | % |
| Thermal shutdown | | | | 150 | | °C |
| Thermal shutdown hysteresis | | | | 20 | | °C |

**Notes:**

7) Not tested in production. Derived by over-temperature correlation.
8) Derived by sample characterization. Not tested in production.


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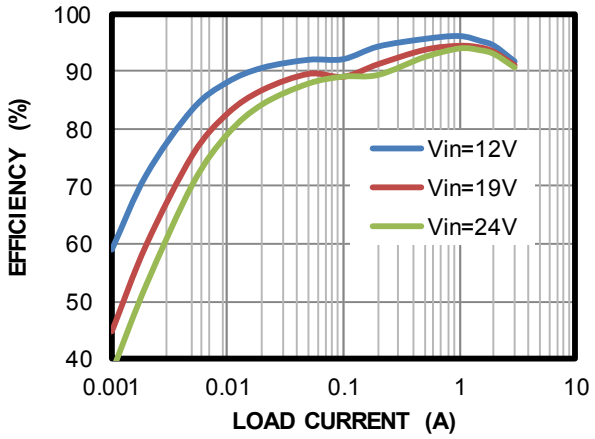
## TYPICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8µH, $T_A$ = 25°C, unless otherwise noted.**

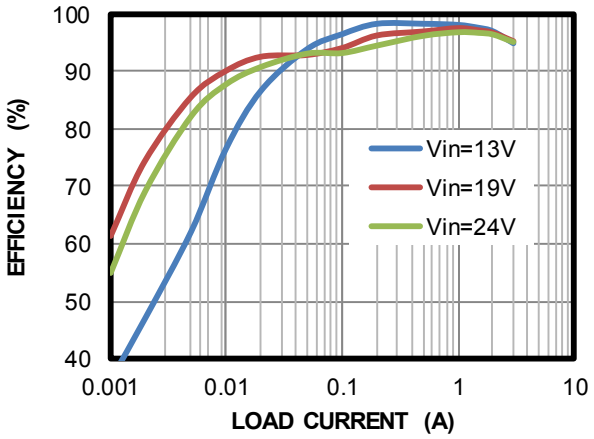
**Efficiency**

$V_{OUT}$ = 5V, L = 6.8µH, DCR = 16mΩ



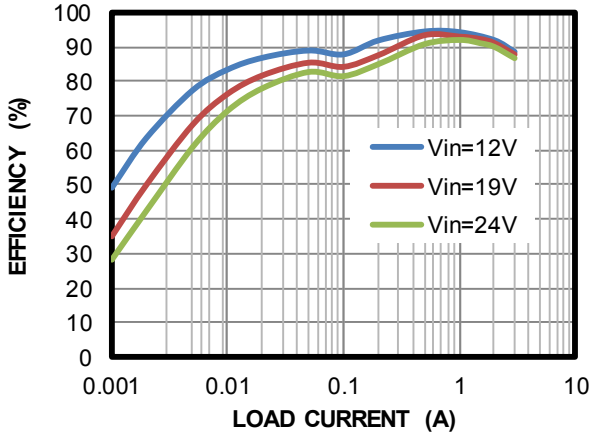

**Efficiency**

$V_{OUT}$ = 12V, L = 10µH, DCR = 24mΩ



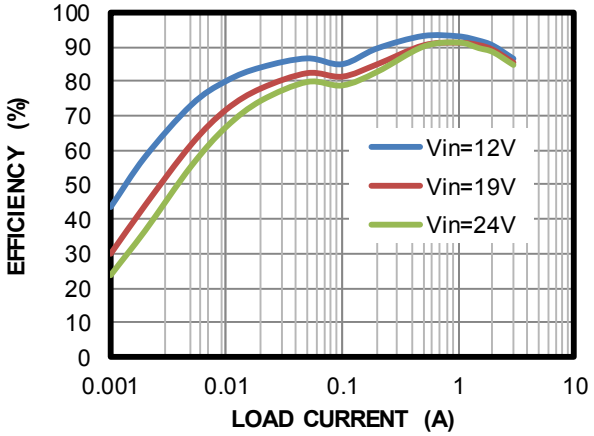

**Efficiency**

$V_{OUT}$ = 3.3V, L = 6.8µH, DCR = 16mΩ



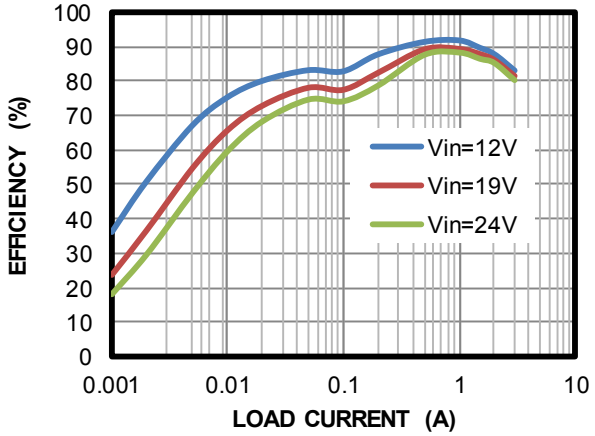

**Efficiency**

$V_{OUT}$ = 2.5V, L = 4.7µH, DCR = 12mΩ



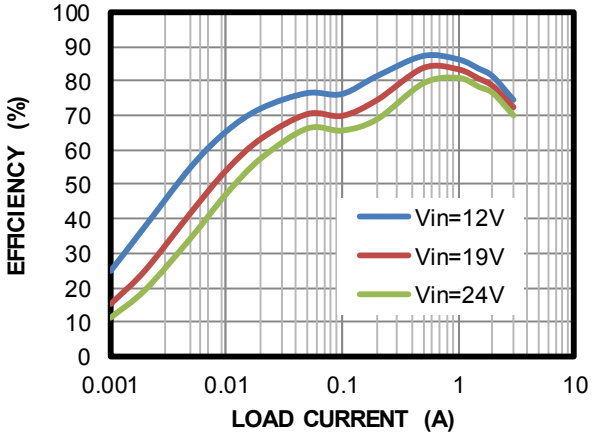

**Efficiency**

$V_{OUT}$ = 1.8V, L = 3.3µH, DCR = 11.7mΩ




**Efficiency**

$V_{OUT}$ = 1V, L = 2.2µH, DCR = 8.3mΩ





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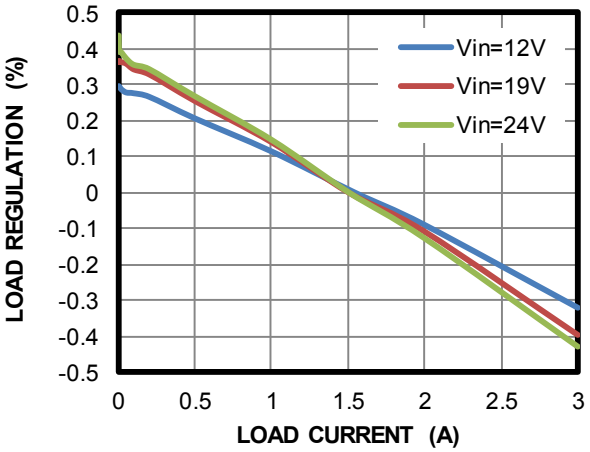
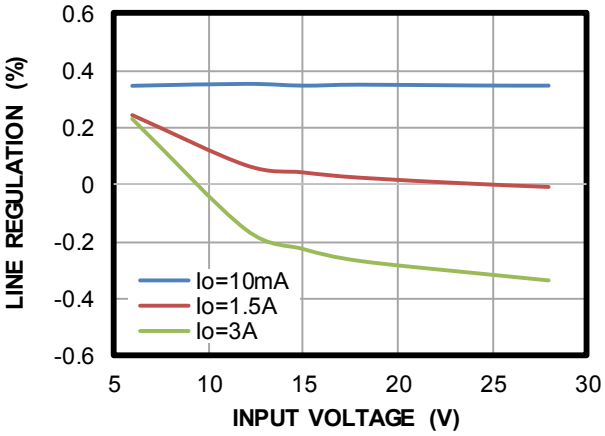
## TYPICAL CHARACTERISTICS (*continued*)

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8µH, $T_A$ = 25°C, unless otherwise noted.**

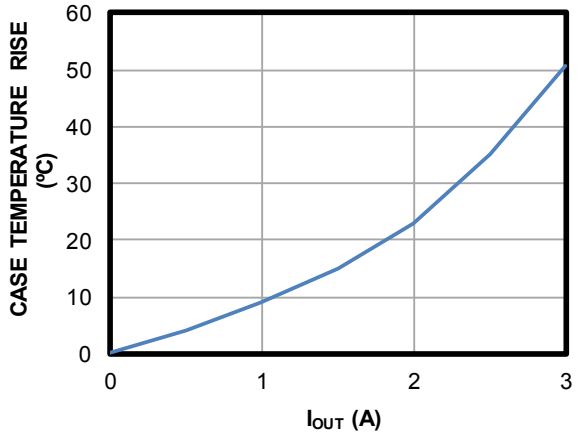
### Load Regulation



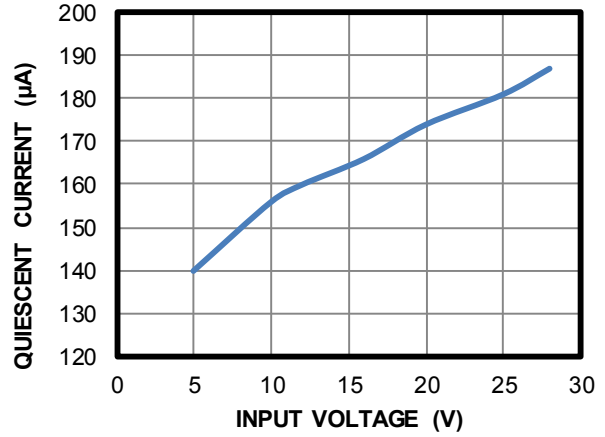

### Line Regulation



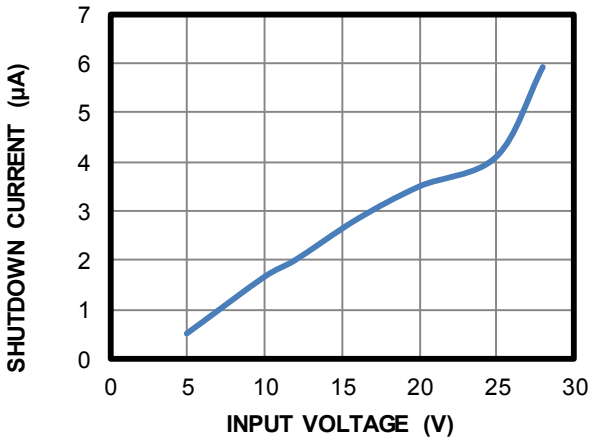

### Case Temperature Rise vs. $I_{OUT}$



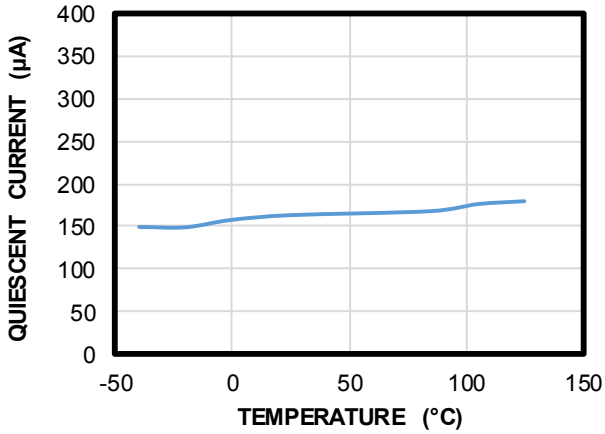

### Quiescent Current vs. Input Voltage




### Shutdown Current vs. Input Voltage




### Quiescent Supply Current vs. Temperature





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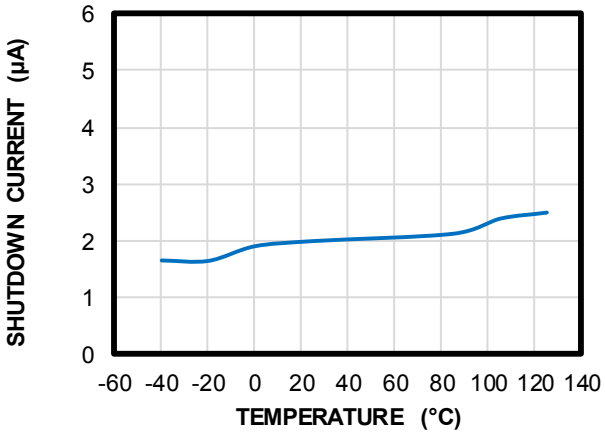
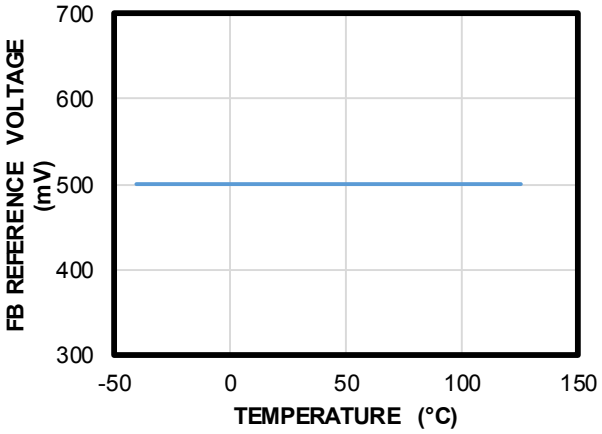
## TYPICAL CHARACTERISTICS (*continued*)

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8µH, $T_A$ = 25°C, unless otherwise noted.**

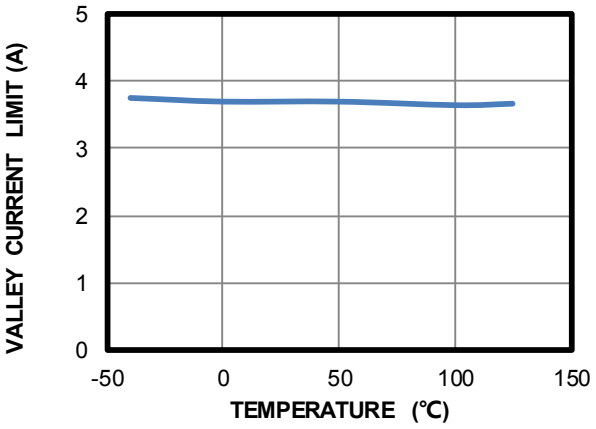
**Shutdown Supply Current vs. Temperature**



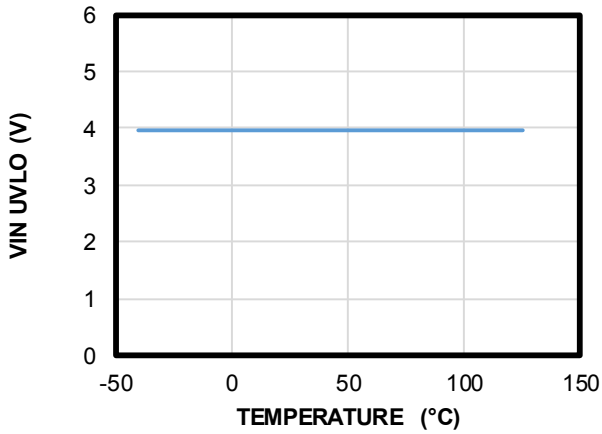

**FB Reference Voltage vs. Temperature**



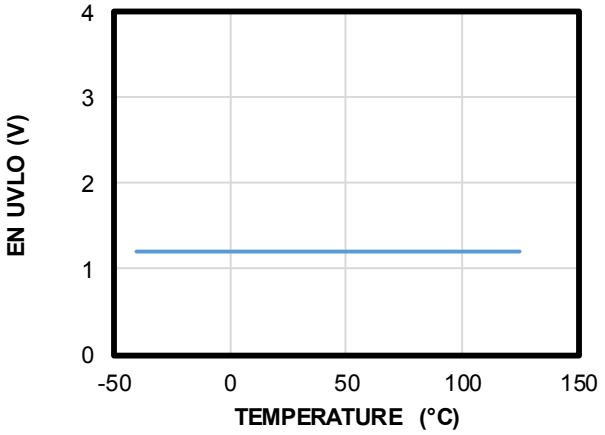

**Valley Current Limit vs. Temperature**



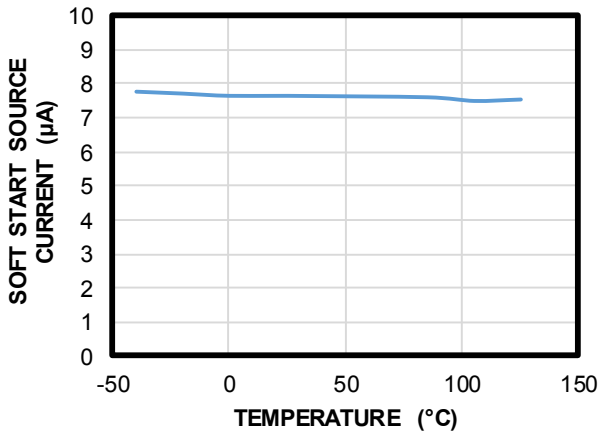

**VIN UVLO vs. Temperature**




**EN UVLO vs. Temperature**




**Soft Start Source Current vs. Temperature**





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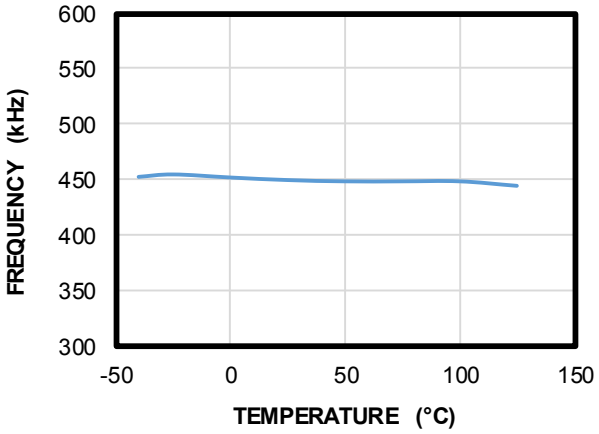
## TYPICAL CHARACTERISTICS (*continued*)

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8µH, $T_A$ = 25°C, unless otherwise noted.**

**Frequency vs. Temperature**





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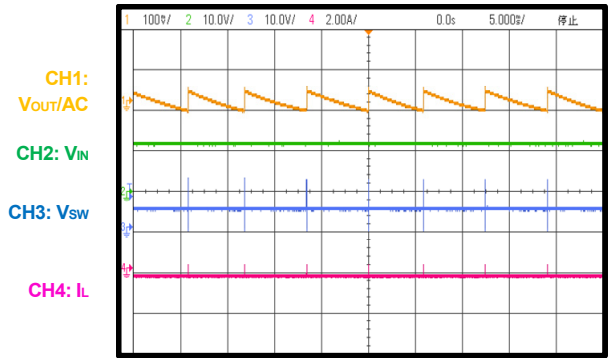
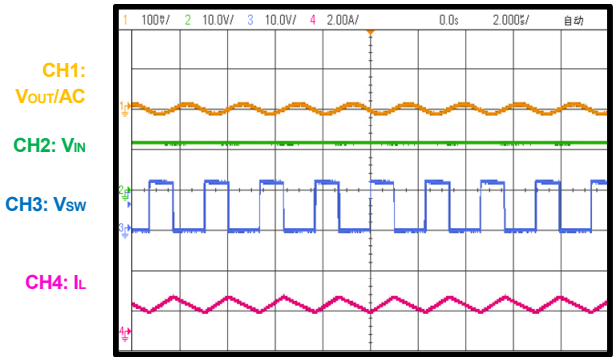
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8µH, $T_A$ = 25°C, unless otherwise noted.**

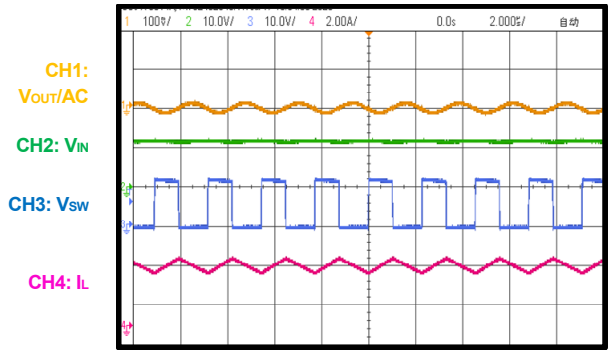
### Steady State
$I_{OUT}$ = 0A



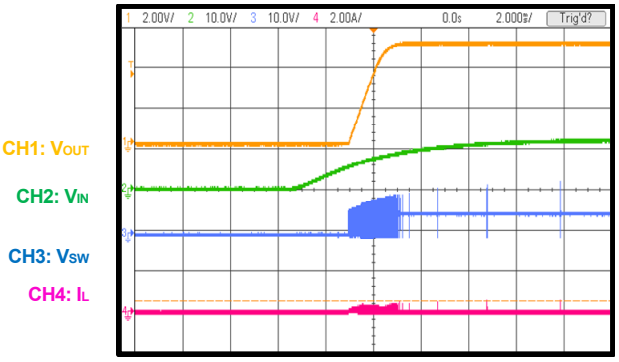

### Steady State
$I_{OUT}$ = 1.5A



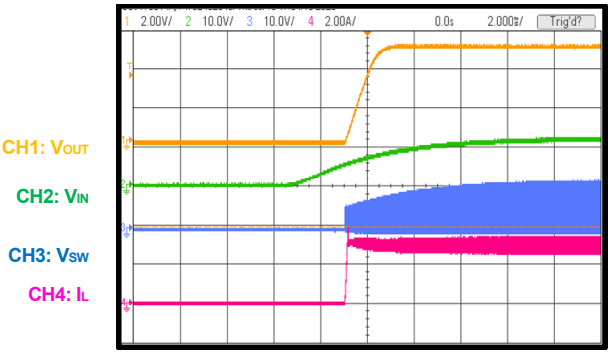

### Steady State
$I_{OUT}$ = 3A



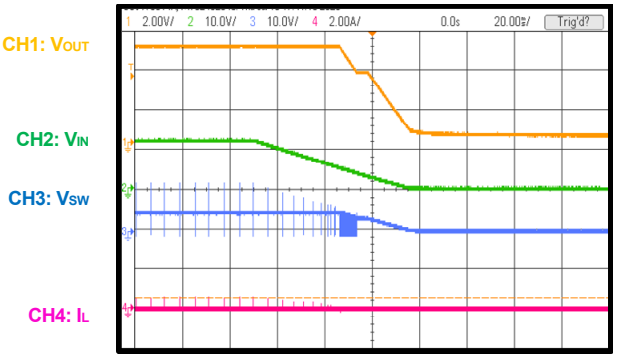

### Input Power Start-Up
$I_{OUT}$ = 0A




### Input Power Start-Up
$I_{OUT}$ = 3A




### Input Power Shutdown
$I_{OUT}$ = 0A





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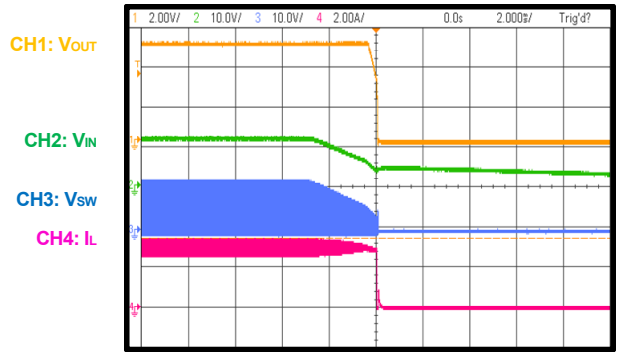
## TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8µH, $T_A$ = 25°C, unless otherwise noted.**

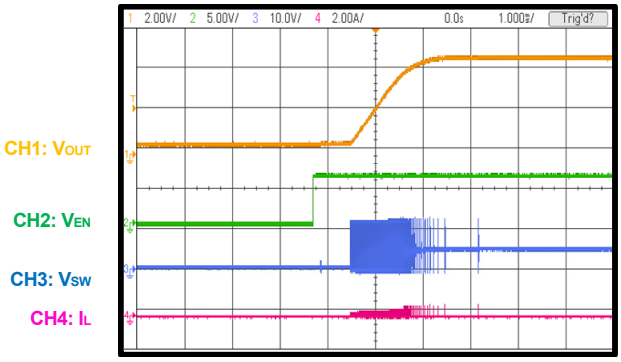
### Input Power Shutdown

$I_{OUT}$ = 3A



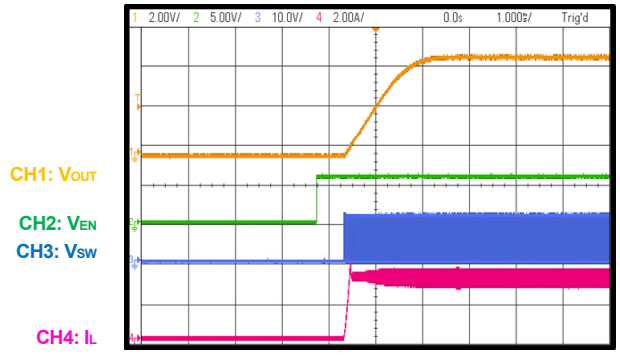

### Start-Up through EN

$I_{OUT}$ = 0A



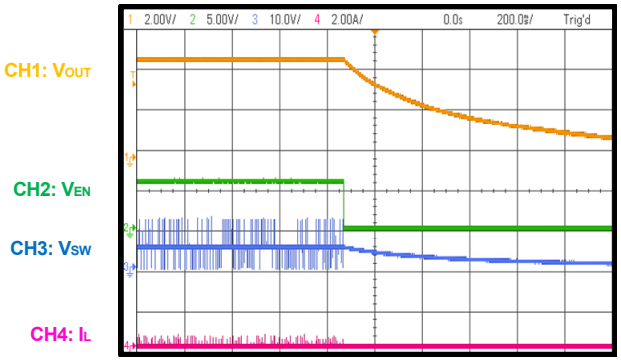

### Start-Up through EN

$I_{OUT}$ = 3A



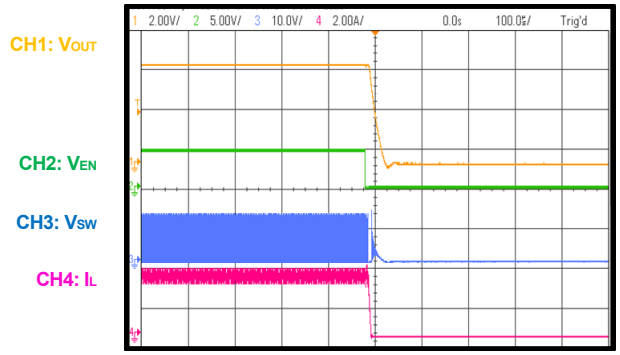

### Shutdown through EN

$I_{OUT}$ = 0A



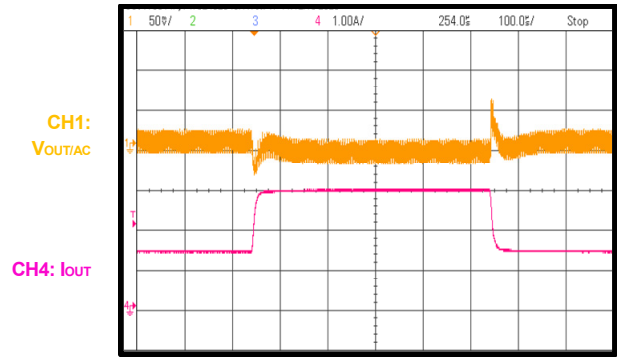

### Shutdown through EN

$I_{OUT}$ = 3A




### Load Transient

$I_{OUT}$ = 1.5A to 3A





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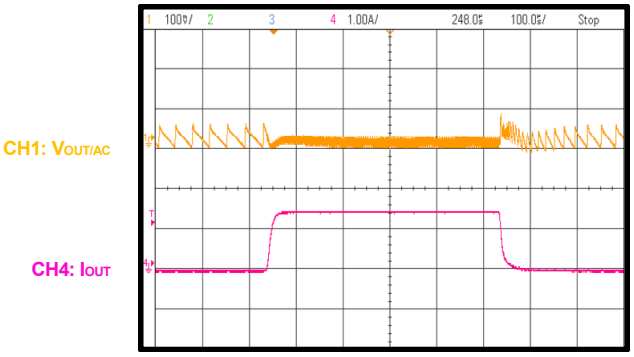
## TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8µH, $T_A$ = 25°C, unless otherwise noted.**

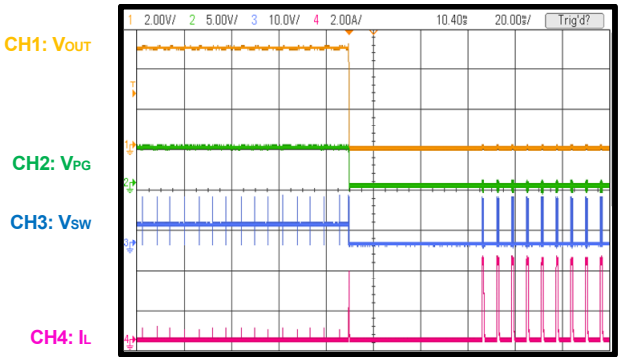
### Load Transient

$I_{OUT}$ = 0A to 1.5A



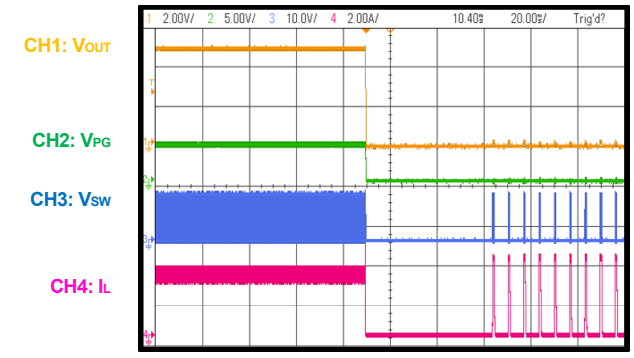

### SCP Entry

$I_{OUT}$ = 0A



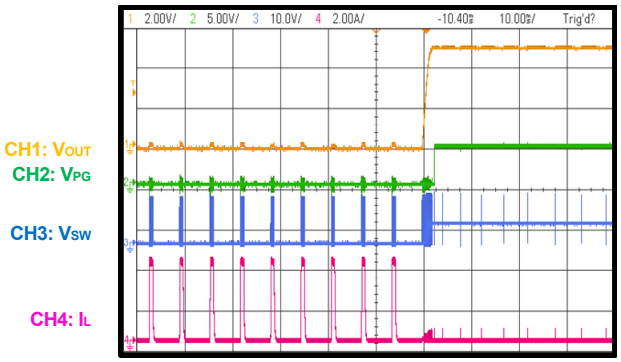

### SCP Entry

$I_{OUT}$ = 3A



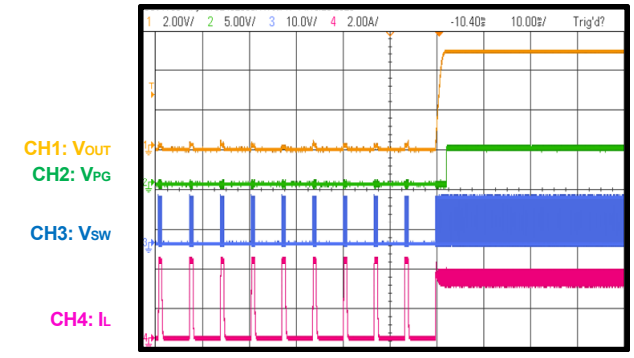

### SCP Recovery

$I_{OUT}$ = 0A




### SCP Recovery

$I_{OUT}$ = 3A





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# FUNCTIONAL BLOCK DIAGRAM

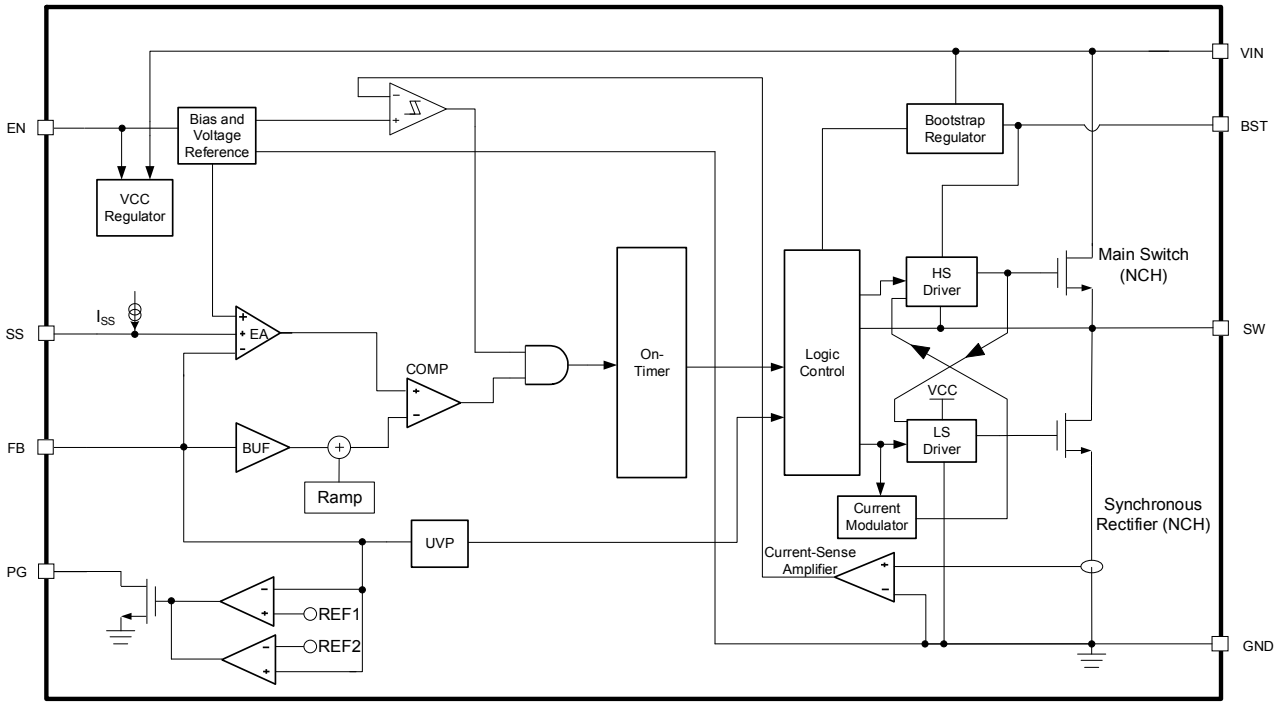


**Figure 1: Functional Block Diagram**


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## OPERATION

The MP2338 is a fully integrated, synchronous, rectified, step-down switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the FB voltage ($V_{FB}$) drops below the reference voltage ($V_{REF}$). The HS-FET turns on for a fixed interval determined by the one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to keep the switching frequency fairly constant across the input voltage range. After the on period finishes, the HS-FET turns off until the next period begins. By repeating this operation, the converter regulates the output voltage.

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above 0A. The low-side MOSFET (LS-FET) turns on when the HS-FET is off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET turn on at the same time. This is called shoot-through. To prevent shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on times, or vice versa.

The MP2338 works in pulse-frequency modulation (PFM) mode during light-load operation. In PFM, the device automatically reduces the switching frequency to maintain high efficiency, and the inductor current drops almost to 0A. When the inductor current reaches 0A, the low-side driver enters tri-state (Hi-Z). The output capacitors discharge slowly to GND through feedback resistors. When $V_{FB}$ drops below the reference voltage, the HS-FET turns on. This operation greatly improves device efficiency when the output current is low.

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does under heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. Then the switching frequency increases. The output current ($I_{OUT}$) reaches critical levels when the current modulator time is 0µs. $I_{OUT}$ can be estimated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{sw} \times V_{IN}} \quad (1)$$

The MP2338 reverts to pulse-width modulation (PWM) mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant across the output current range.

### Enable (EN) Control

The enable (EN) pin can enable or disable the entire chip. Pull EN high to turn the converter on. Pull EN low to turn the converter off.

For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. There is an internal 1MΩ resistor from EN to GND. To calculate the automatic start-up voltage, determine the values of the pull-up resistor ($R_{UP}$, from VIN to EN) and pull-down resistor ($R_{DOWN}$, from EN to GND) with Equation (2):

$$V_{IN_START} = 1.3 \times \frac{R_{UP} + R_{DOWN}//1000k\Omega}{R_{DOWN}//1000k\Omega} \quad (2)$$

For example, if $R_{UP}$ = 191kΩ and $R_{DOWN}$ = 49.9kΩ, set $V_{IN\text{-}START}$ to 6.5V.

To avoid damaging the internal circuit, the EN voltage must not exceed 6V.

### Under-Voltage Lockout (UVLO)

VIN under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO rising threshold on VIN is about 3.96V, and its falling threshold is about 3.63V.

### Soft Start (SS)

The MP2338 employs a soft start (SS) mechanism to ensure smooth output ramping during start-up.

When the part starts, an internal current source (typically 7.5µA) charges up the SS capacitor to generate a soft-start voltage ($V_{SS}$). When $V_{SS}$ is below $V_{REF}$, $V_{SS}$ overrides $V_{REF}$, and the error amplifier uses $V_{SS}$ as the reference.


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The output voltage smoothly ramps up. Once $V_{SS}$ rises above the $V_{REF}$, the error amplifier uses $V_{REF}$ as the reference. At this point, soft start finishes, and then the device enters steady state operation.

The SS capacitor value can estimated with Equation (3):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}} \quad (3)$$

Note that the soft-start time is the time it takes for the 22nF SS capacitor's output to rise from 0% to 100%. Generally, the soft-start time is about 1.5ms.

### Over-Current Protection (OCP)

The MP2338 has a valley current limit. While the LS-FET is on, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the device enters over-current protection (OCP) mode, and the HS-FET does not turn on again until the valley current limit disappears. Meanwhile, the output voltage drops until $V_{FB}$ falls below the FB under-voltage (UV) threshold. Once the UV condition is triggered, the MP2338 enters hiccup mode (after the SS period) to periodically restart the part.

During OCP, the device tries to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft-start capacitor, and then automatically tries to soft start again. If the over-current condition remains after soft start ends, the device repeats this operation cycle until the over-current conditions disappear. Then the output rises back to the regulation level.

### Power Good (PG)

The power good (PG) pin indicates whether the output voltage is in the normal range compared to the internal reference voltage. It is an open-drain output that requires an external pull-up supply. During start-up, the PG output is pulled low.

When the output voltage is between 90% and 112% of the internal reference voltage and soft start is finished, the power good signal is pulled high. If the output voltage is below 84% after soft start finishes, the PG signal stays low.

When the output voltage exceeds 112% of the internal reference, PG switches low. The PG signal pulls high once the output voltage drops below 106% of the internal reference voltage.

The PG output is pulled low if the following protections are triggered: EN under-voltage lockout (UVLO), over-current protection (OCP), or over-temperature protection (OTP).

If PG is pulled up to an external voltage, PG does not de-assert (logic low) if $V_{IN}$ drops below 0.8V. If PG is pulled up to $V_{OUT}$, the PG signal de-asserts (logic low) if $V_{IN}$ drops below 0.8V.

### On Time ($t_{ON}$) Extension

To improve dropout, the MP2338 is designed to extend its on time ($t_{ON}$) when the duty cycle exceeds 92%. When the HS-FET on time is extended, the frequency drops. The typical minimum frequency is 250kHz. The frequency cannot drop below 250kHz.

### Pre-Biased Start-Up

The MP2338 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged. The voltage on the soft-start capacitor is also charged. If the BST voltage exceeds its rising threshold voltage, and $V_{SS}$ exceeds the sensed output feedback voltage at the FB pin, the part starts switching normally.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection, with a rising threshold of 2.62V and a hysteresis of 130mV. $V_{IN}$ regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1, and C2 (see Figure 2). If ($V_{IN}$ - $V_{SW}$) exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C3.

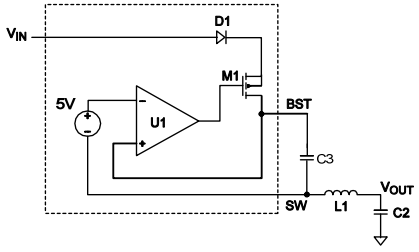


**Figure 2: Internal Bootstrap Charger**


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### Start-Up and Shutdown

If both $V_{IN}$ and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal converter is enabled. The converter provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, $V_{IN}$ going low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. Then the internal supply rail is pulled down.

### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 150°C, the whole chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.


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# APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the output voltage. Choose a value for R2. R2 should be chosen reasonably, as a smaller-value resistor results in considerable quiescent current loss, while a larger-value resistor makes FB sensitive to noise. Typically, set the current through R2 to be between 5μA and 30μA for an optimal balance between system stability and no-load loss. Then R1 can be calculated with Equation (4):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (4)$$

Figure 3 shows the feedback circuit. $R_T$ is an optional resistor for feedback compensation.

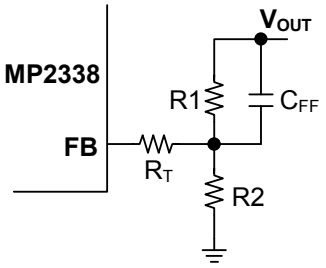


**Figure 3: Feedback Network**

Table 1 lists the recommended feedback resistor values for common output voltages.

**Table 1: Parameter Selection for Common Output Voltages**

| VOUT (V) | R1 (kΩ) | R2 (kΩ) | RT (kΩ) | CFF (pF) | L (μH) |
|---|---|---|---|---|---|
| 1 | 51 | 51 | 10 | 82 | 2.2 |
| 1.8 | 51 | 16.9 | 10 | 470 | 3.3 |
| 2.5 | 51 | 12.7 | 10 | 470 | 4.7 |
| 3.3 | 51 | 9.09 | 10 | 470 | 6.8 |
| 5 | 90.9 | 10 | 10 | 300 | 6.8 |
| 12 | 255 | 11 | 10 | 82 | 10 |

### Selecting the Inductor

The inductor must supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, a larger-value inductor has a larger physical footprint, higher series resistance, and lower saturation current. The inductance value can be calculated with Equation (5):

$$L = \frac{V_{OUT}}{f_{sw} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Where $\Delta I_L$ is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be estimated with Equation (6):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{sw} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

**Table 2: Power Inductor Selection**

| Part Number | Inductor Value | Manufacturer |
|---|---|---|
| MPL-AL | 2.2μH to 10μH | MPS |
| MPL-AL-6050-2R2 | 2.2μH | MPS |
| MPL-AL-6050-3R3 | 3.3μH | MPS |
| MPL-AL-6060-4R7 | 4.7μH | MPS |
| MPL-AL6060-6R8 | 6.8μH | MPS |
| MPL-AL6060-100 | 10μH | MPS |

Visit MonolithicPower.com under Products > Inductors for more information.

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and they should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter.


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The input ripple current can be calculated with Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (8):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (8)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be calculated with Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{sw} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (10):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{sw} \times C_{IN}} \quad (10)$$

### Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (11)$$

With ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

The output voltage ripple caused by ESR is very small. With POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

Besides considering the output ripple, choosing a larger-value output capacitor improves load transient response, but the maximum output capacitor limitation should also be considered in design applications. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value ($C_{O_MAX}$) can be estimated with Equation (14):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (14)$$

Where $I_{LIM_AVG}$ is the average start-up current during soft start, and $t_{SS}$ is the soft-start time.

### Design Example

Table 3 shows a design example following the application guidelines for the specifications below.

**Table 3: Design Example**

| | |
|---|---|
| **$V_{IN}$** | 6.5V to 28V |
| **$V_{OUT}$** | 5V |
| **$I_{OUT}$** | 3A |

For the detailed application schematic, see Figure 9 on page 22. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 11. For more device applications, refer to the related evaluation board datasheet.


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## PCB Layout Guidelines

Proper layout of the switching power supplies is very important and critical for proper function. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the high current paths (GND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible (it is recommended to be within 1mm).
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short, and route it away from the feedback network.

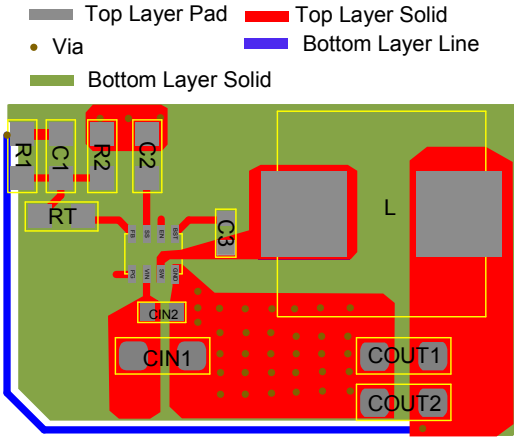


**Figure 4: Recommended PCB Layout**


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## TYPICAL APPLICATION CIRCUITS

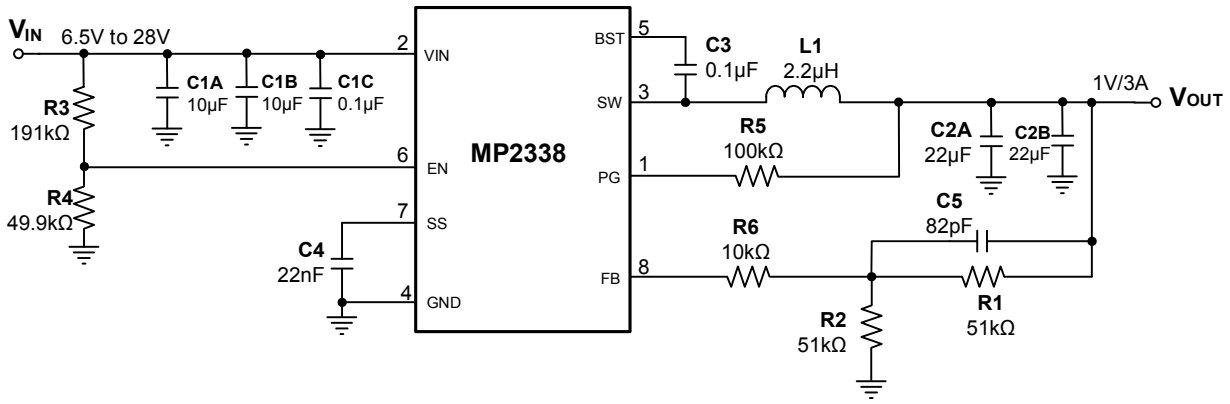


**Figure 5: $V_{IN}$ = 6.5V to 28V, $V_{OUT}$ = 1V, $I_{OUT}$ = 3A**

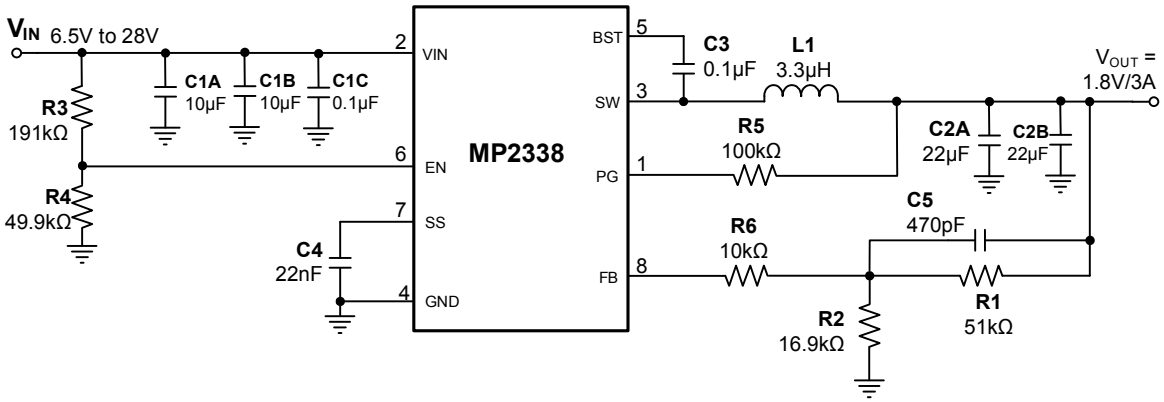


**Figure 6: $V_{IN}$ = 6.5V to 28V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

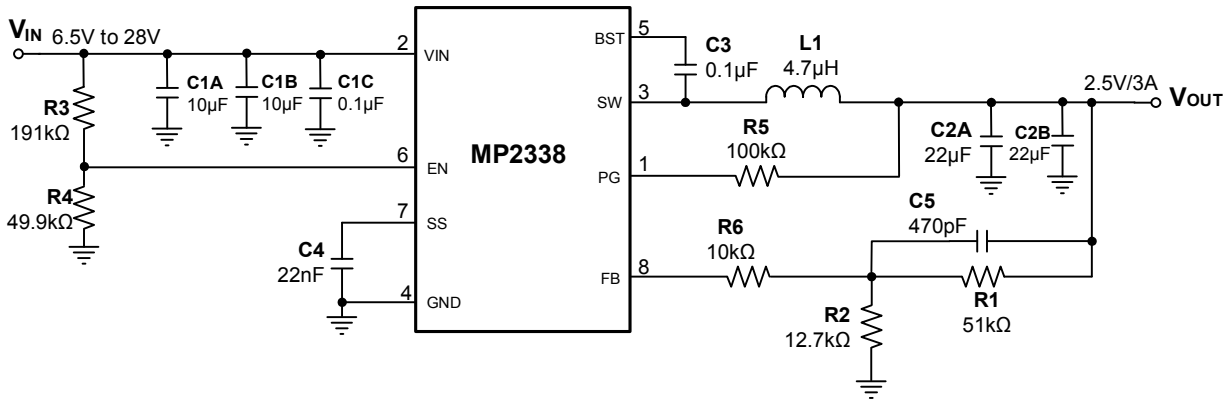


**Figure 7: $V_{IN}$ = 6.5V to 28V, $V_{OUT}$ = 2.5V, $I_{OUT}$ = 3A**


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## TYPICAL APPLICATION CIRCUITS *(continued)*

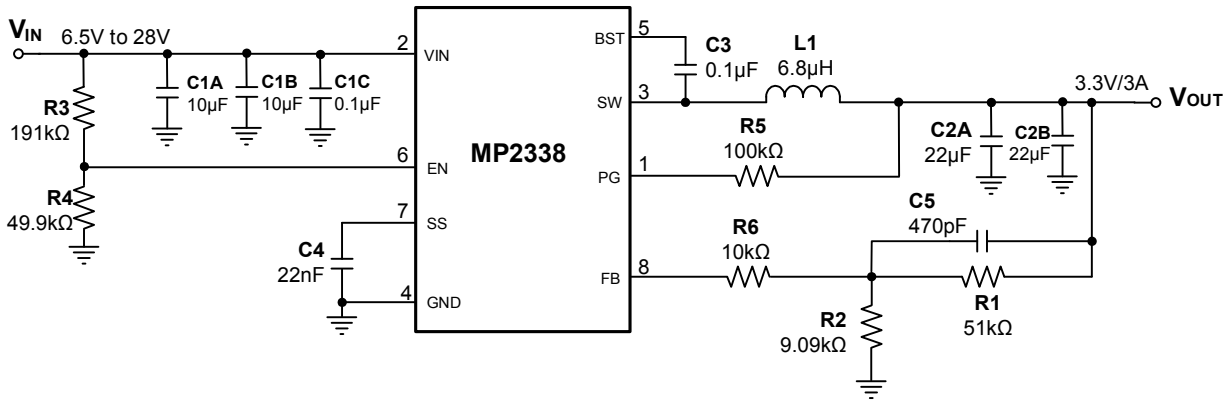


**Figure 8: $V_{IN}$ = 6.5V to 28V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 3A**

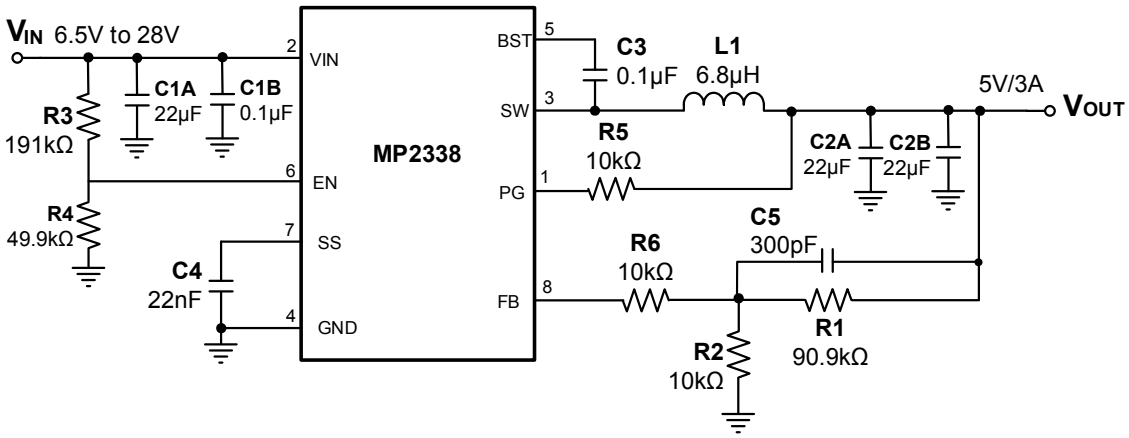


**Figure 9: $V_{IN}$ = 6.5V to 28V, $V_{OUT}$ = 5V, $I_{OUT}$ = 3A**

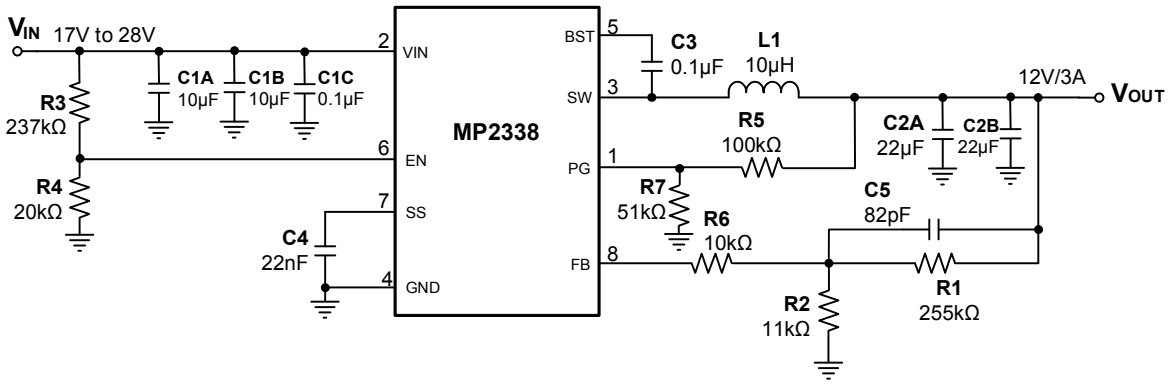


**Figure 10: $V_{IN}$ = 6.5V to 28V, $V_{OUT}$ = 12V, $I_{OUT}$ = 3A**

**Note:**

9) C5 improves transient performance. C5 is not required if there is not a high request for the load transient.


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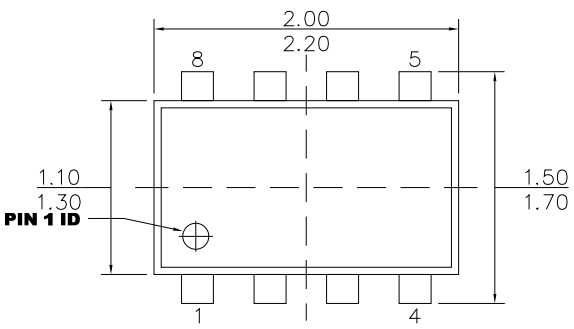
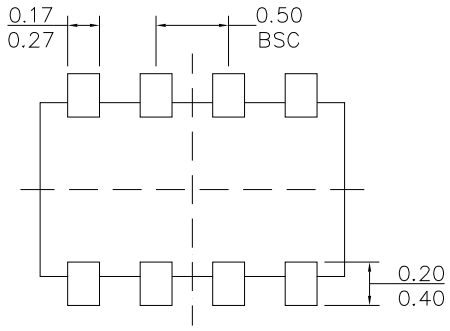
## PACKAGE INFORMATION

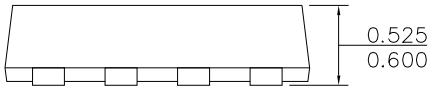
### SOT583



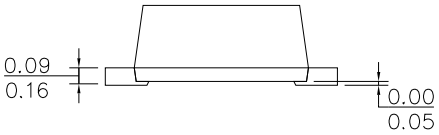

**TOP VIEW**



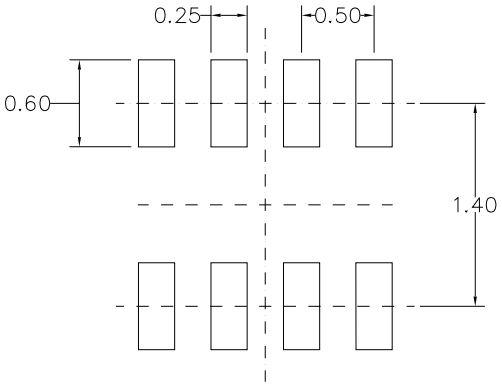

**BOTTOM VIEW**




**FRONT VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.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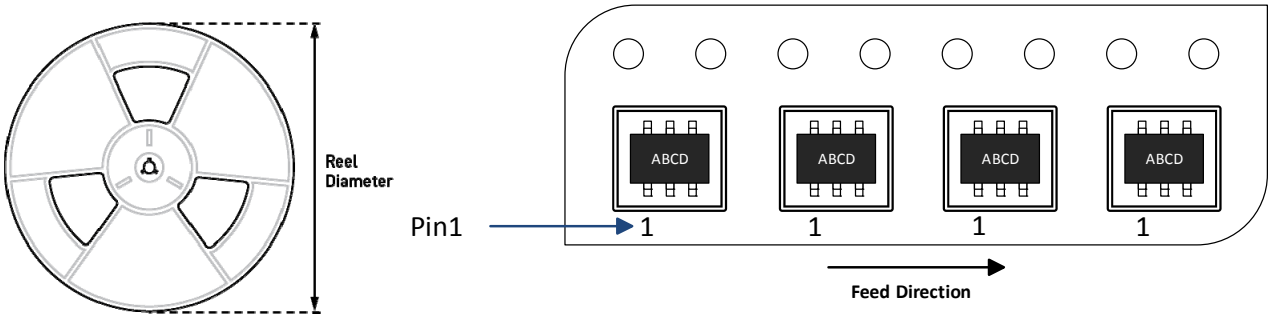
## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tray | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MP2338GTL–Z | SOT583 | 5000 | N/A | N/A | 7in | 8mm | 4mm |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## Revision History

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 12/11/2020 | Initial Release | - |

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