MPM3806

5.5V, 1A, Synchronous Step-Down Power Module, AEC-Q100 Qualified

DESCRIPTION

The MPM3806 is an easy-to-use, fully integrated, synchronous step-down power module with a built-in inductor and power MOSFETs. It can achieve up to 1A of continuous output current (I_{OUT}), with excellent load and line regulation.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown. An open-drain power good (PG) signal indicates that the output voltage (V_{OUT}) exceeds 90% of its nominal voltage.

The MPM3806 is ideal for a wide range of applications, including high-performance digital signal processors (DSPs), advanced driver assistance system (ADAS) sensors, portable and mobile devices, and other low-power systems with constrained area.

The MPM3806 requires a minimal number of readily available, standard external components, and is available in a small QFN-15 (3mmx4mmx1.6mm) package.

FEATURES

- Designed for Automotive Applications:
  - Wide 2.5V to 5.5V Operating V_{IN} Range
  - Up to 1A Output Current (I_{OUT})
  - 1% Feedback (FB) Accuracy
  - -40°C to +150°C T_J Range
  - Available in AEC-Q100 Grade 1
- Increased Battery Life:
  - 21μA Sleep Mode I_Q
  - Advance Asynchronous Modulation (AAM) Mode for Increased Efficiency under Light-Load Conditions
- High Performance for Improved Thermals:
  - 75mΩ and 45mΩ Integrated Internal Power MOSFETs
- Optimized for EMC and EMI Reduction:
  - 2.4MHz Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- Optimized for Board Size and BOM:
  - Integrated Internal Power MOSFETs
  - Integrated Compensation Network
  - Fixed-Output Options (1): 0.8V, 1V, 1.1V, 1.2V, 1.25V, 1.5V, 1.8V, 2.5V, 2.8V, and 3.3V
  - Available in a QFN-15 (3mmx4mmx1.6mm) Package
- Additional Features:
  - Enable (EN) for Power Sequencing
  - Power Good (PG)
  - 100% Duty Cycle
  - External Soft Start (SS) Control
  - Output Discharge
  - OVP and SCP with Hiccup Mode
  - Available in a Wettable Flank Package

Note:

1) See the Ordering Information section on page 3 for the availability of each fixed-output version. Contact an MPS FAE for details on additional output voltage (V_{OUT}) options.

APPLICATIONS

- Camera Modules
- ADAS Sensors
- Automotive Infotainment Systems
- Automotive V2X

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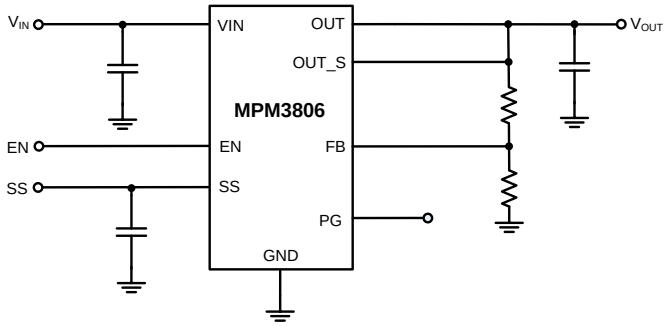
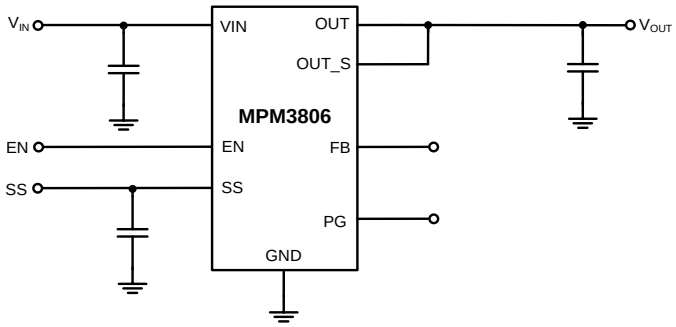
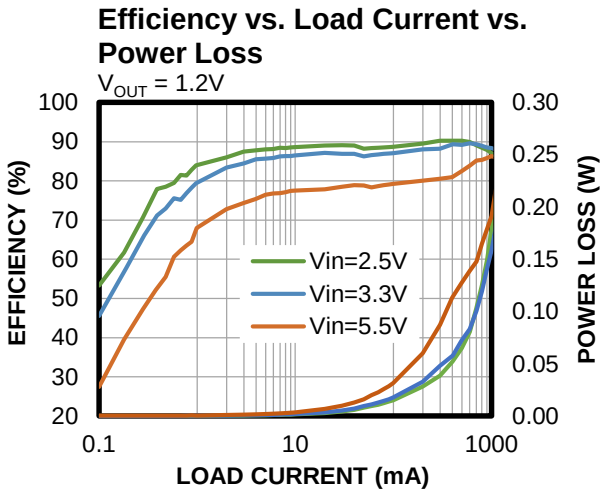
TYPICAL APPLICATION



Typical Application (Adjustable Output)



Typical Application (Fixed Output)



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ORDERING INFORMATION

Part Number* (2)	Output Voltage	Package	Top Marking	MSL Rating**
MPM3806GLE-AEC1***	Adjustable	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1
MPM3806GLE-12-AEC1***	Fixed 1.2V	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1
MPM3806GLE-18-AEC1***	Fixed 1.8V	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPM3806CGLE-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

Note:

2) Contact an MPS FAE for details on additional V_{OUT} options.

TOP MARKING

MPYW
3806
LLL
ME

MP: MPS prefix
Y: Year code
W: Week code
3806: First four digits of the part number
LLL: Lot number
M: Module
E: Wettable flank frame

MPYW
3806
LLL
ME12

MP: MPS prefix
Y: Year code
W: Week code
3806: First four digits of the part number
LLL: Lot number
M: Module
E: Wettable flank frame
12: 1.2V fixed-output version of the MPM3806

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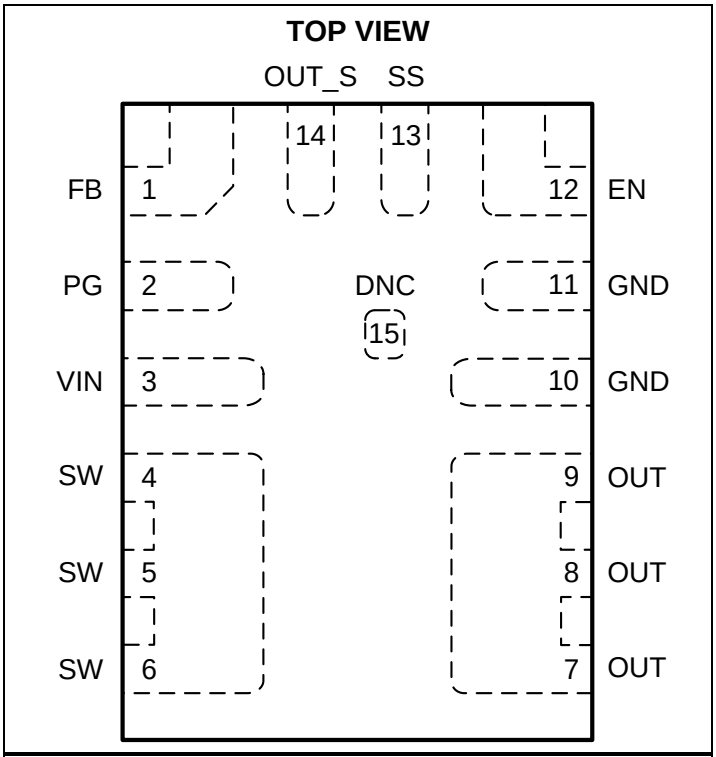
MPYW
3806
LLL
ME18

MP: MPS prefix
Y: Year code
W: Week code
3806: First four digits of the part number
LLL: Lot number
M: Module
E: Wettable flank frame
18: 1.8V fixed-output version of the MPM3806

PACKAGE REFERENCE



QFN-15 (3mmx4mmx1.6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	FB	**Feedback.** To set the output voltage (V_{OUT}) for the adjustable-output version of the MPM3806, connect the feedback (FB) pin to an external resistor divider between the output and GND. To set the regulation voltage, the FB voltage (V_{FB}) is compared to the internal reference voltage (V_{REF}) (0.6V). Float the FB pin for the fixed-output version of the MPM3806..
2	PG	**Power good indicator.** The power good (PG) pin is an open-drain output. Connect PG to a voltage source using an external resistor. If V_{FB} exceeds 90% of V_{REF}, PG is pulled high. If V_{FB} drops below 85% of V_{REF}, PG is pulled to GND. Float PG if not used.
3	VIN	**Input voltage supply.** The MPM3806 operates from a 2.5V to 5.5V input voltage (V_{IN}) range. A decoupling capacitor is required to prevent large voltage spikes at the input.
4, 5, 6	SW	**Switch output.** The SW pin is the internal, P-channel high-side MOSFET (HS-FET) drain. SW is connected internally to the power inductor.
7, 8, 9	OUT	**Power output.** Connect the OUT pin to the load. An output capacitor (C_{OUT}) is required to reduce the voltage ripple.
10, 11	GND	**IC ground.** Connect the GND pin to the negative terminals of the input and output capacitors using large copper areas. Use several vias to connect GND to the ground plane.
12	EN	**Enable.** Pull the EN voltage (V_{EN}) above 0.9V to turn the device on; pull V_{EN} below 0.65V turn it off. There is an internal 2MΩ resistor connected between EN and GND.
13	SS	**Soft start.** Connect a ≥1nF soft-start capacitor (C_{SS}) between the SS and GND pins to set the soft-start time (t_{SS}) and reduce the start-up inrush current.
14	OUT_S	**Output sense.** The OUT_S pin is the V_{OUT} sense, as well as the discharge path to the 150Ω resistive load.
15	DNC	**Do not connect.** The DNC pad is connected internally to SW. Do not route or place vias under this area.

ABSOLUTE MAXIMUM RATINGS (3)

All pins……...-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (4) (8)
QFN-15 (3mmx4mmx1.6mm)……2.4W
Operating junction temperature .....150°C
Lead temperature…….....260°C
Storage temperature……...-65°C to +150°C

ESD Ratings

Human body model (HBM).....Class 2 (5)
Charged device model (CDM).....Class 2b (6)

Recommended Operating Conditions

Input voltage (V_{IN})……2.5V to 5.5V
Output voltage (V_{OUT})……0.6V to V_{IN} - 0.5V
Load current range……0A to 1A
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-15 (3mmx4mmx1.6mm)
JESD51-7…..…....…….65……14…°C/W (7)
EVM3806-LE-00A.....53.....10...°C/W (8)

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AEC-Q100-002
6) Per AEC-Q100-011
7) Measured on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. θ_{JC} is the thermal resistance from the junction to case bottom.
8) Measured on EVM3806-LE-00A (6.3cmx6.3cm), 2oz copper, 4-layer PCB. θ_{JC} is the thermal resistance from the junction to case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$			2.3	2.45	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$			2.1		V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			0.2		V
Input quiescent current	I_Q	V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V, T_J = 25°C		21	30	µA
		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V, T_J = -40°C to +125°C (9)			40	µA
		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V, T_J = -40°C to +150°C			80	µA
Input shutdown current	I_{SD}	V_{EN} = 0V, T_J = 25°C		0.01	1	µA
		V_{EN} = 0V, T_J = -40°C to +125°C (9)			3	µA
		V_{EN} = 0V, T_J = -40°C to +150°C			20	µA
V_{IN} over-voltage protection (OVP) rising threshold	$V_{IN\_OVP\_RISING}$	After output OVP is enabled		6.15		V
V_{IN} OVP falling threshold	$V_{IN\_OVP\_FALLING}$			5.95		V
V_{IN} OVP hysteresis	V_{INOVP_HYS}			0.2		V
Switching Frequency (f_{SW}), MOSFETs, and Inductors						
Switching frequency	f_{SW}		2000	2400	2640	kHz
Minimum on time (7)	t_{ON_MIN}	V_{IN} = 5V		50		ns
Minimum off time (7)	t_{OFF_MIN}	V_{IN} = 5V		80		ns
Maximum duty cycle	D_{MAX}			100		%
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = 25°C		0	1	µA
		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = -40°C to +125°C (9)			30	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{IN} = 5V		75	110	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{IN} = 5V		45	70	mΩ
Integrated inductor (9)	L_1		376	470	564	nH
Integrated inductor DC resistance	R_L			25	65	mΩ
Integrated inductor saturation current (9)	I_{L_SAT}		4.8	5.4		A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output and Regulation						
Feedback (FB) voltage (adjustable output)	V_{FB}	T_J = 25°C	0.594	0.6	0.606	V
		T_J = -40°C to +150°C	0.591	0.6	0.609	V
Output regulation voltage (fixed output)	V_{OUT_REG}	1.2V fixed output	1.176	1.2	1.224	V
		1.8V fixed output	1.764	1.8	1.836	
FB input current	I_{FB}	Adjustable output		50	100	nA
		1.2V fixed output		3	8	µA
		1.8V fixed output		5	10	
V_{OUT} discharge resistance	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		150		Ω
Enable (EN)						
EN rising threshold	V_{EN_RISING}			0.9	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.4	0.65		V
EN threshold hysteresis	V_{EN_HYS}			0.25		V
EN turn-on delay		Pull EN high to enable SW		100		µs
EN turn-off delay		Pull EN low to stop switching		30		µs
EN pull-down resistance				2		MΩ
EN input current	I_{EN}	V_{EN} = 2V		1.2		µA
		V_{EN} = 0V		0		µA
Soft Start (SS)						
Soft-start current	I_{SS}		1.5	3	4.5	µA
Power Good (PG)						
PG rising threshold	V_{PG_RISING}	FB rising edge	87%	90%	93%	V_{FB}
PG falling threshold	$V_{PG\_FALLING}$	FB falling edge	82%	85%	88%	V_{FB}
PG logic high voltage	V_{PG_HIGH}	V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
PG logic low voltage	V_{PG_LOW}	Sink 1mA			0.4	V
PG rising deglitch time	t_{PG_RISING}			80		µs
PG falling deglitch time	$t_{PG\_FALLING}$			80		µs
PG leakage current (high)		5V logic high			100	nA
PG self-bias		V_{IN} = 0V, V_{EN} = 0V, PG is pulled up to between 3V and 5.5V via a 100kΩ resistor			0.7	V
Protections						
Peak current limit (I_{LIMIT})	I_{LIMIT_PEAK}		1.6	2.5	3.4	A
Valley I_{LIMIT}	I_{LIMIT_VALLEY}		0.4	1.0	1.6	A
Reverse I_{LIMIT}	$I_{LIMIT\_REVERSE}$	Current flows from SW to GND		1.2		A
Zero-current detection (ZCD) threshold				50		mA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal shutdown (9)	T_{SD}			170		°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			20		°C
Output OVP threshold	V_{OVP}		110	115	120	% of V_{FB}
Output OVP hysteresis	V_{OVP_HYS}			10		% of V_{FB}
OVP delay				2		µs

Note:

9) Guaranteed by design and characterization. Not tested in production.

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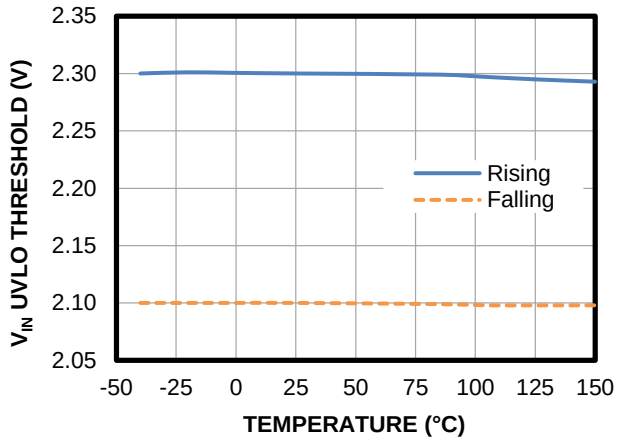
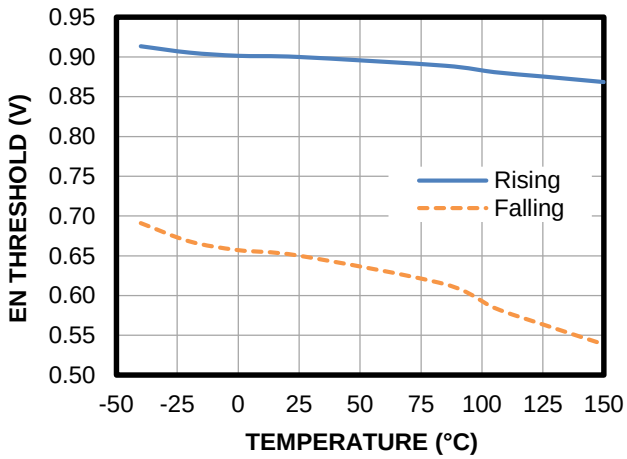
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

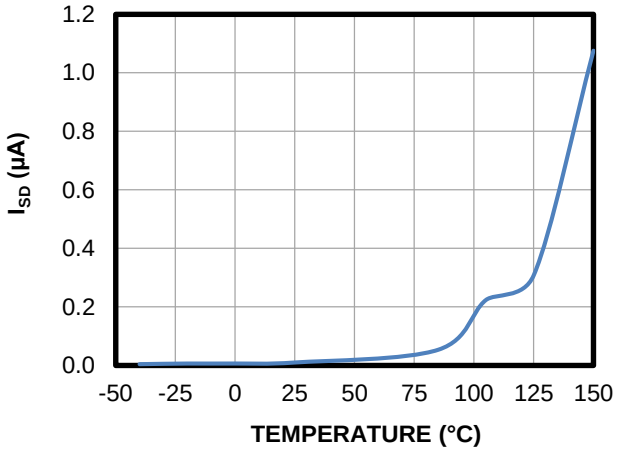
V_{IN} UVLO Threshold vs. Temperature



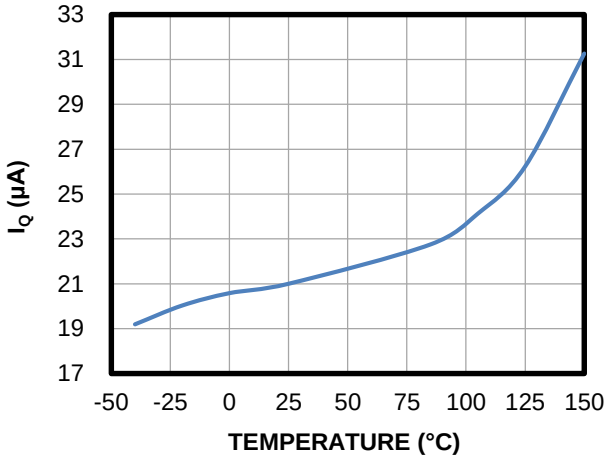
EN Threshold vs. Temperature



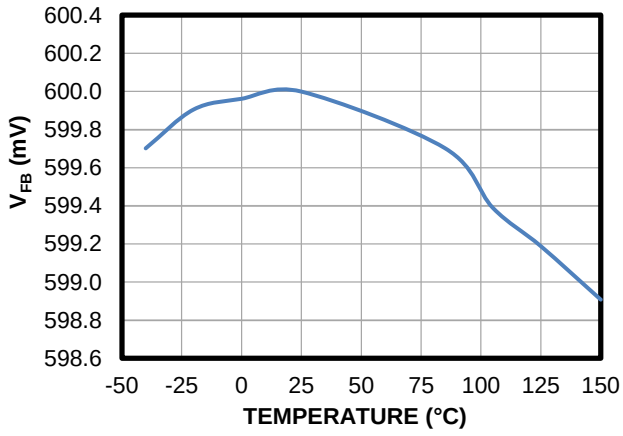
Shutdown Current vs. Temperature



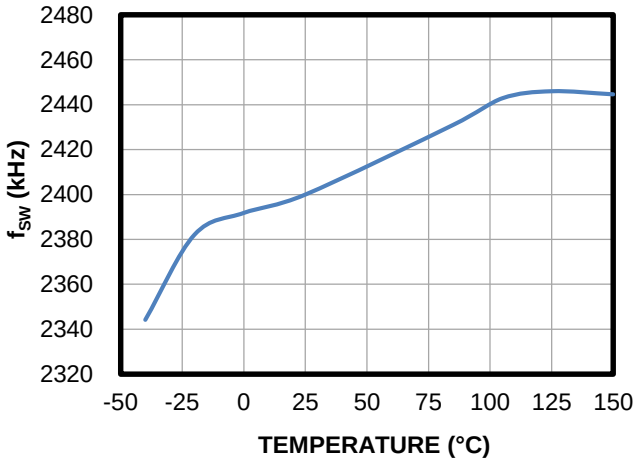
Quiescent Current vs. Temperature



Feedback Voltage vs. Temperature



Switching Frequency vs. Temperature



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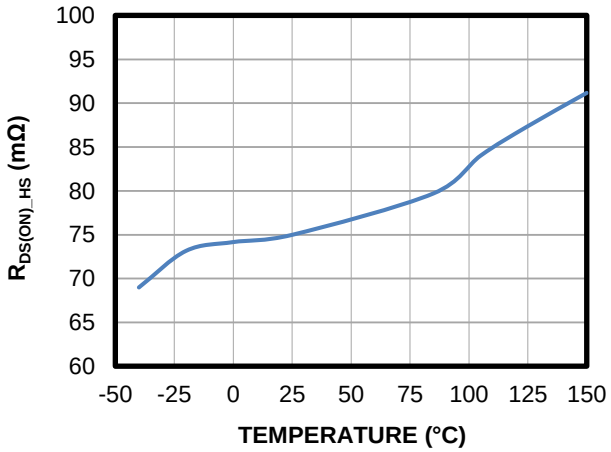
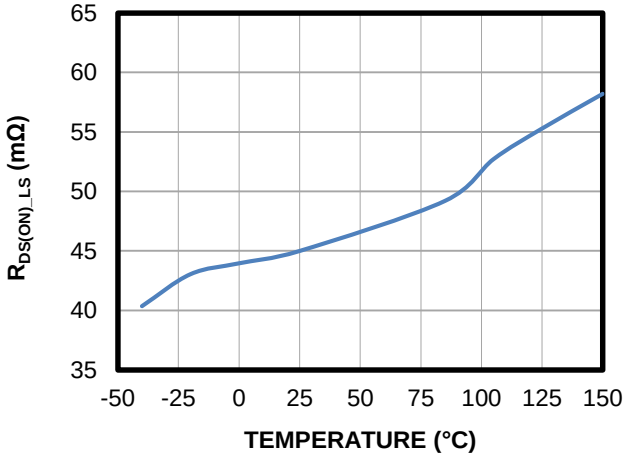
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

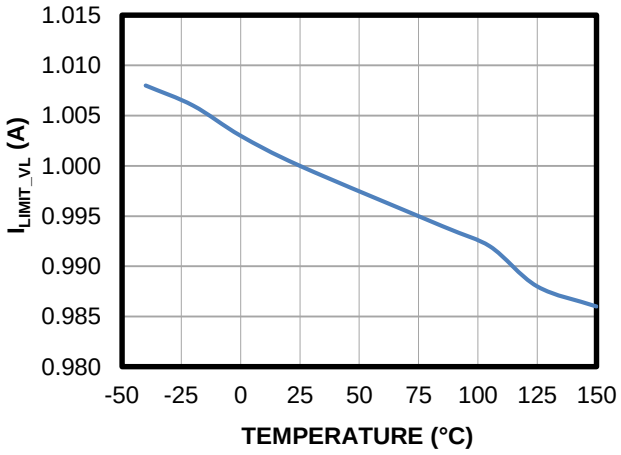
HS-FET On Resistance vs. Temperature



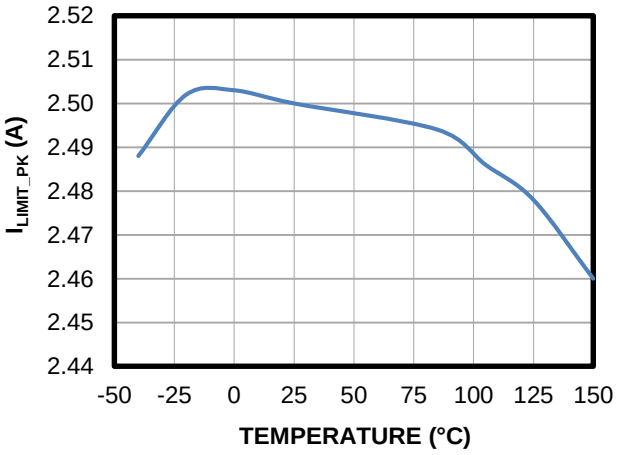
LS-FET On Resistance vs. Temperature



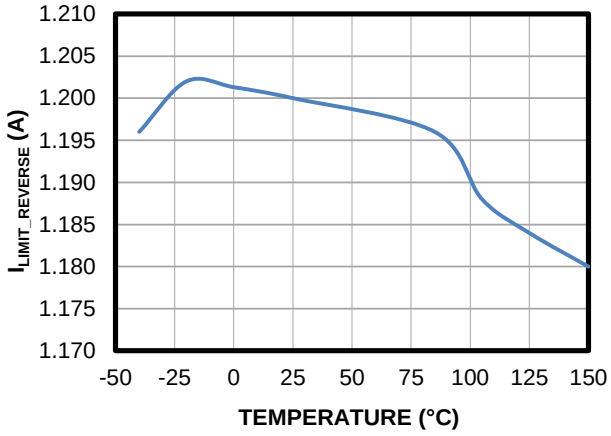
Valley Current Limit vs. Temperature



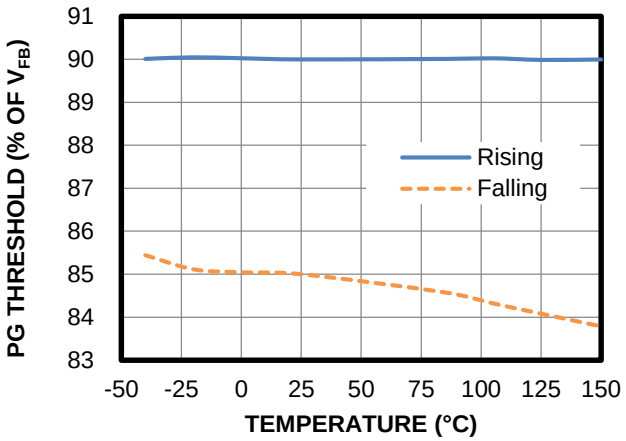
Peak Current Limit vs. Temperature



Reverse Current Limit vs. Temperature



PG Threshold vs. Temperature



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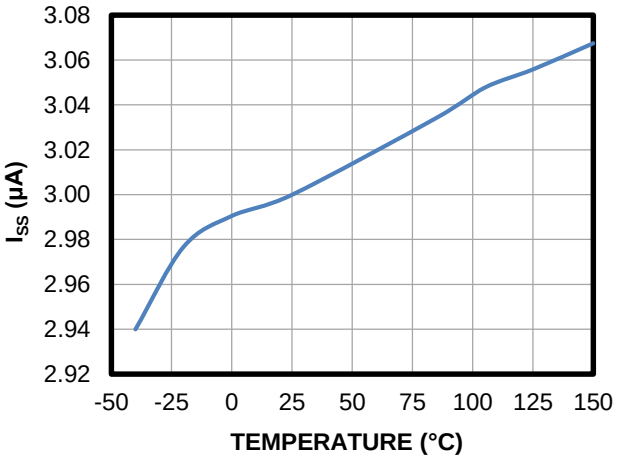
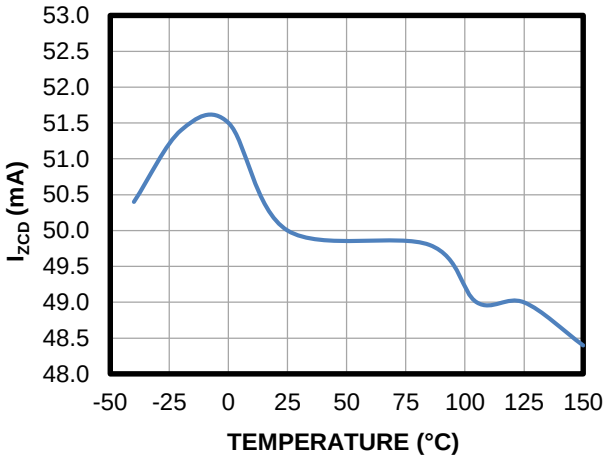
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

Soft-Start Current vs. Temperature



Zero-Current Detection vs. Temperature



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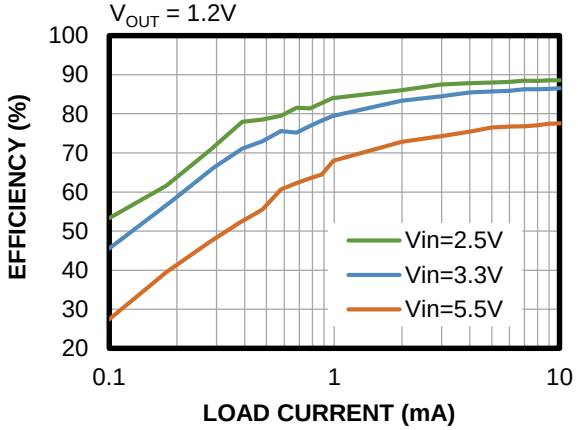
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

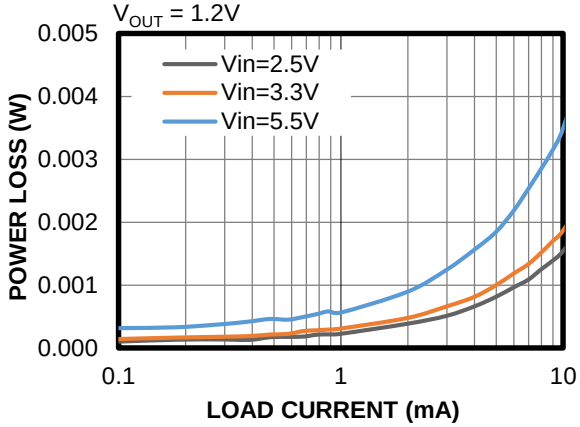
Efficiency vs. Load Current

V_{OUT} = 1.2V



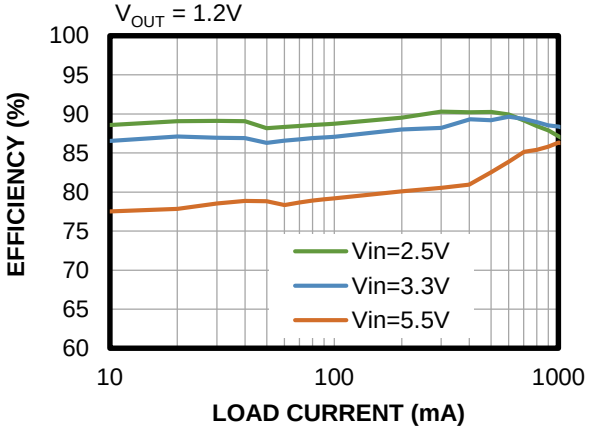
Power Loss vs. Load Current

V_{OUT} = 1.2V



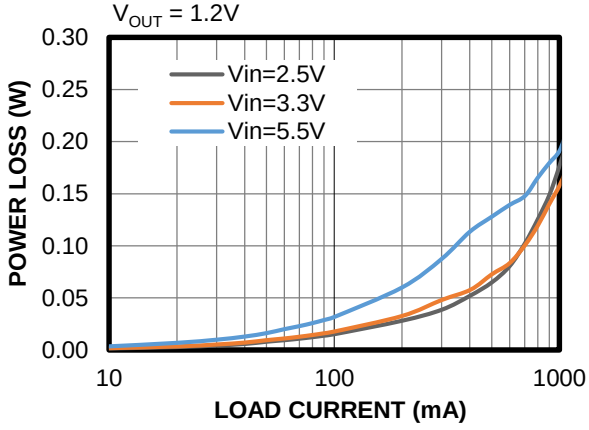
Efficiency vs. Load Current

V_{OUT} = 1.2V



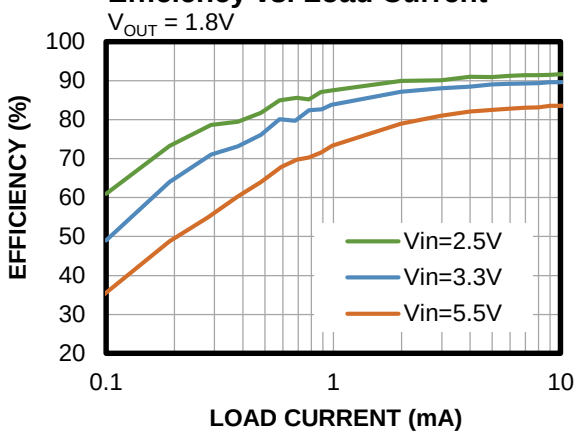
Power Loss vs. Load Current

V_{OUT} = 1.2V



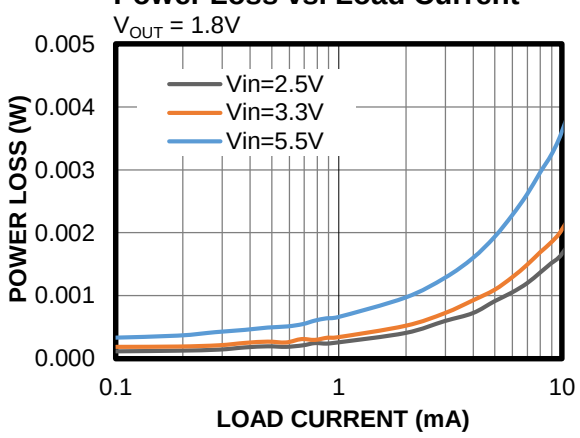
Efficiency vs. Load Current

V_{OUT} = 1.8V



Power Loss vs. Load Current

V_{OUT} = 1.8V



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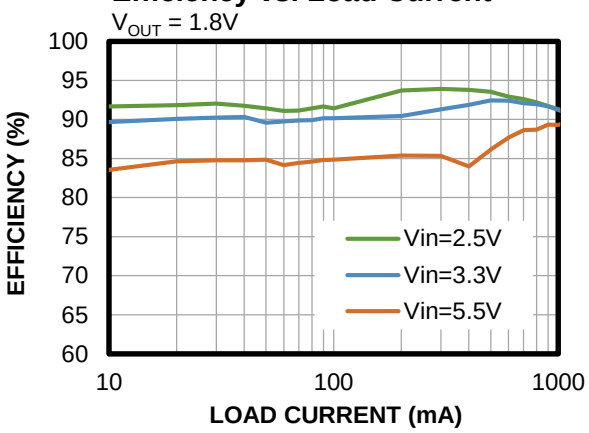
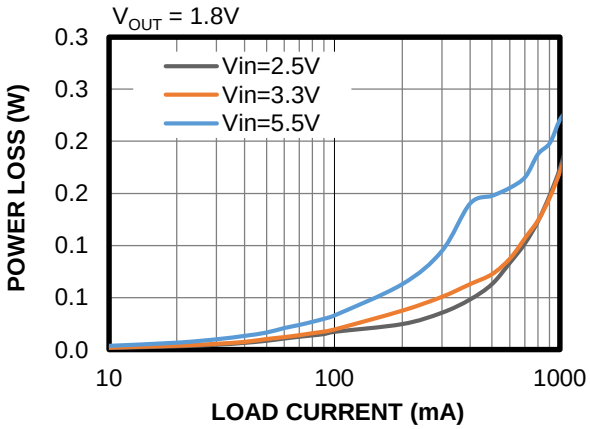
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

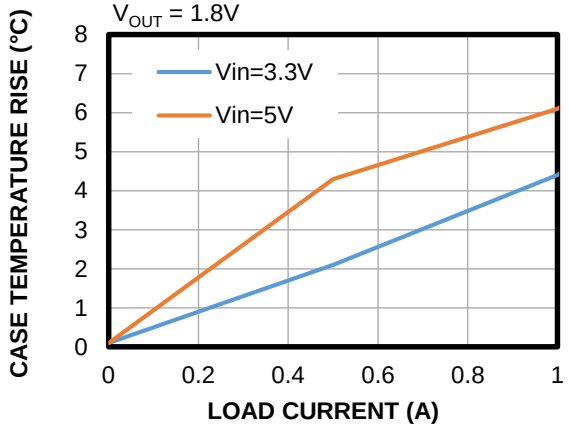
Efficiency vs. Load Current



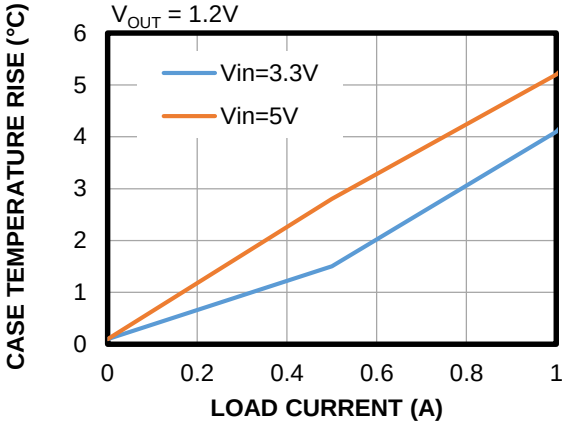
Power Loss vs. Load Current



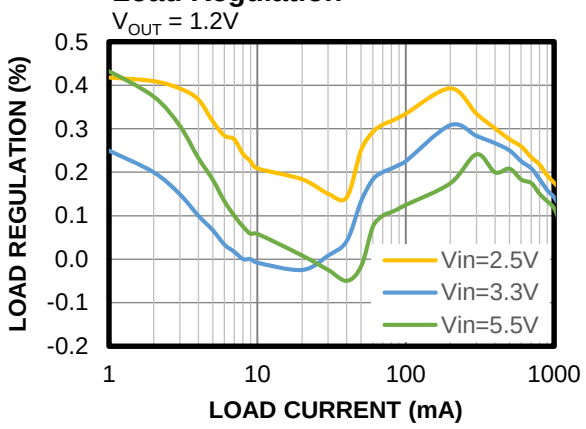
Case Temperature Rise



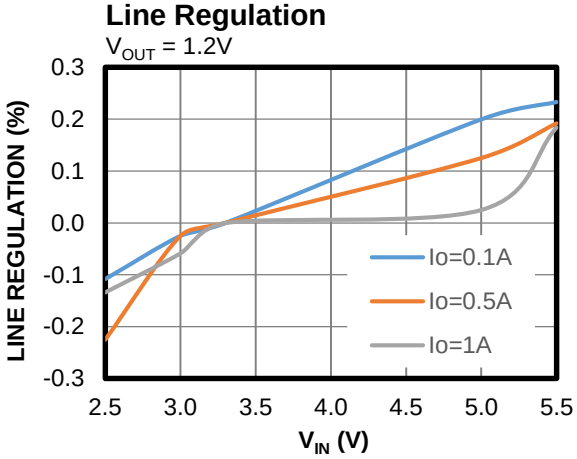
Case Temperature Rise



Load Regulation



Line Regulation



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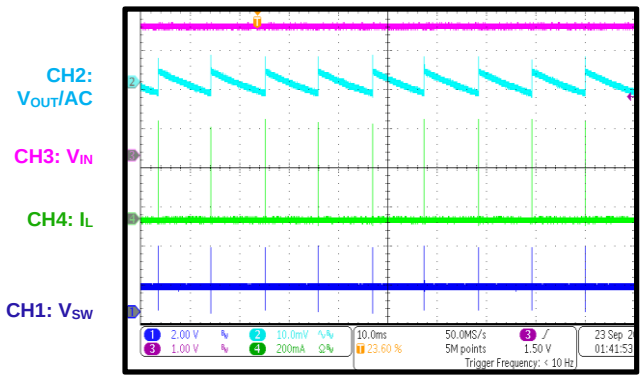
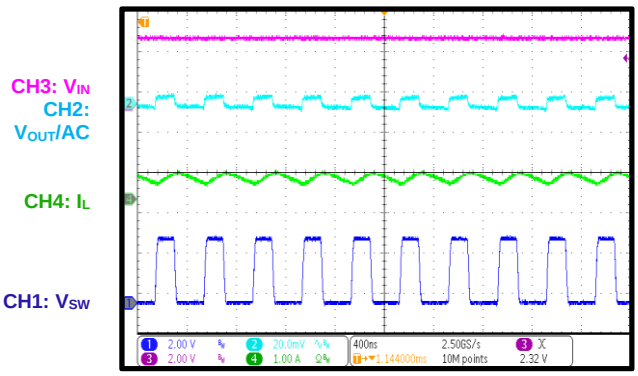
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

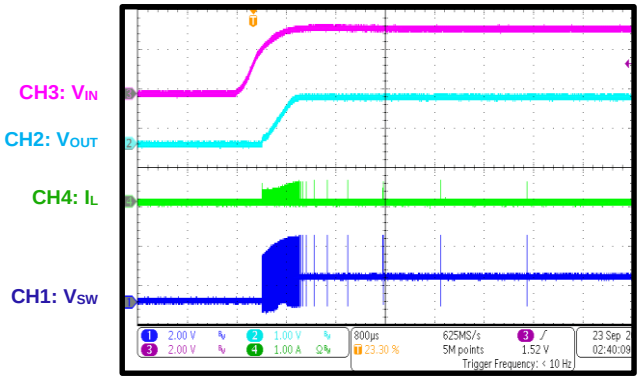
Steady State
I_{OUT} = 0A



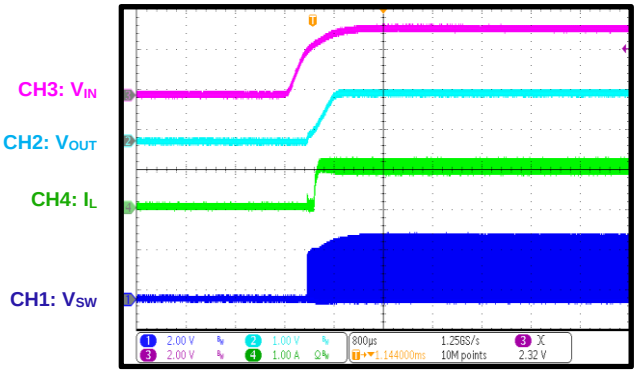
Steady State
I_{OUT} = 1A



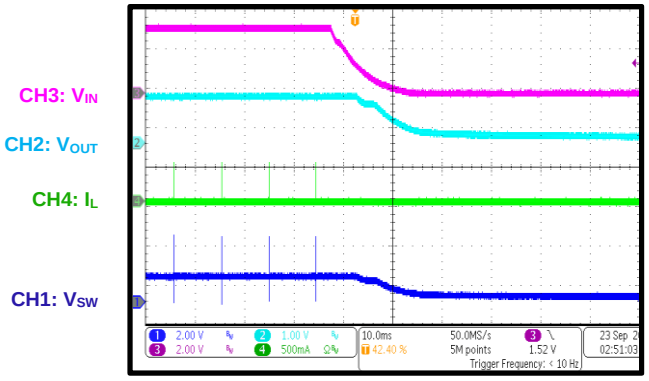
Start-Up through VIN
I_{OUT} = 0A



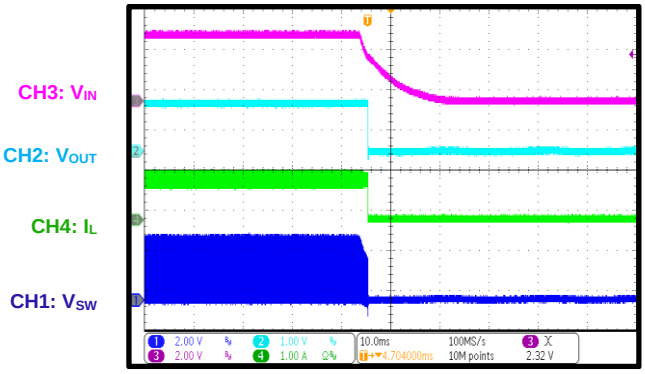
Start-Up through VIN
I_{OUT} = 1A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 1A



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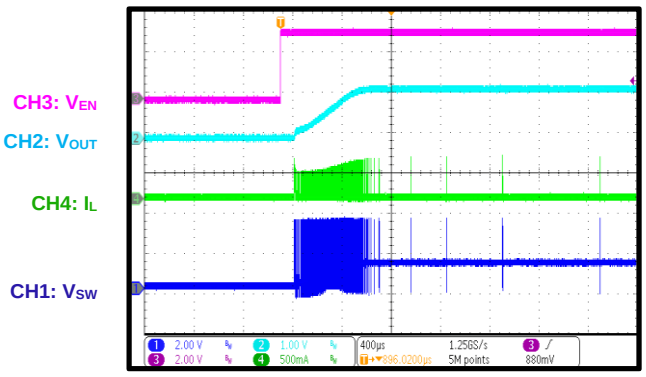
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

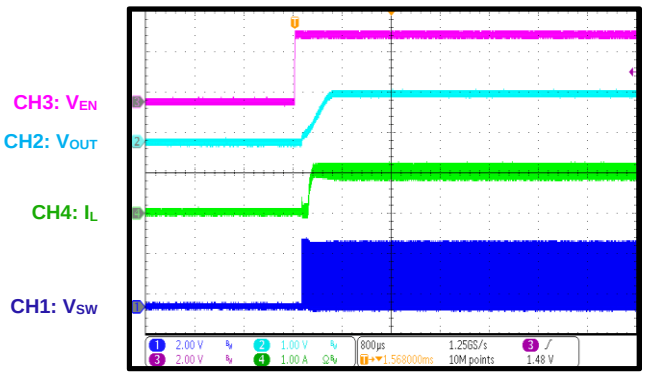
Start-Up through EN

I_{OUT} = 0A



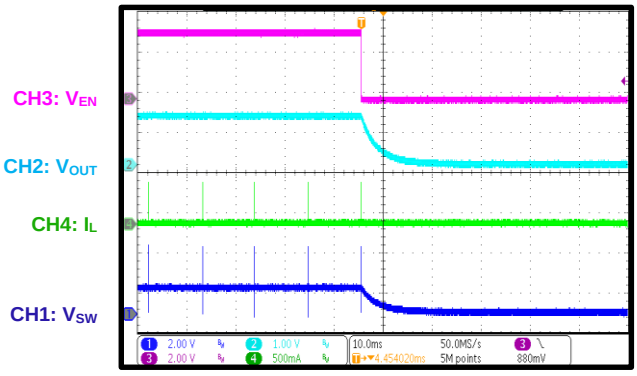
Start-Up through EN

I_{OUT} = 1A



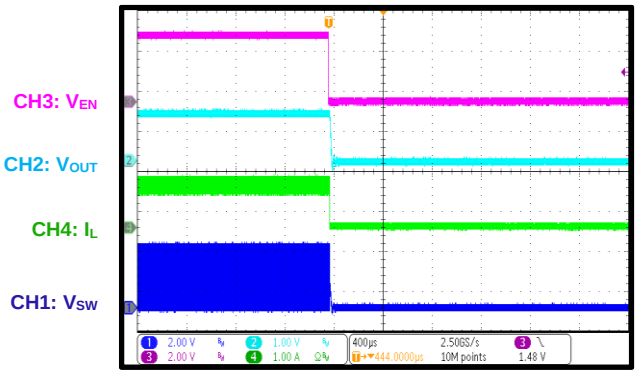
Shutdown through EN

I_{OUT} = 0A



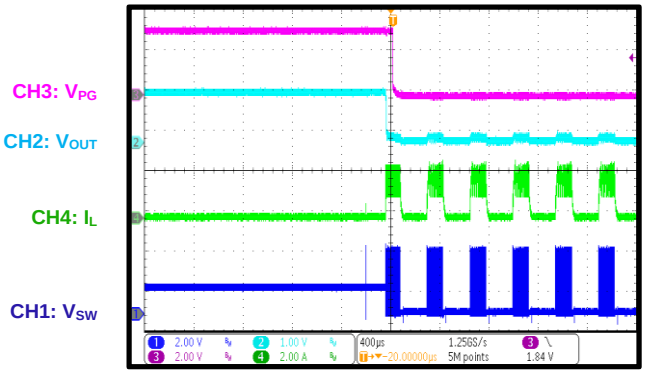
Shutdown through EN

I_{OUT} = 1A



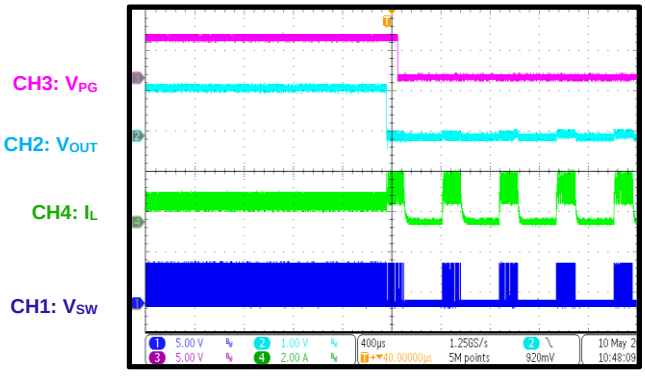
SCP Entry

I_{OUT} = 0A



SCP Entry

I_{OUT} = 1A



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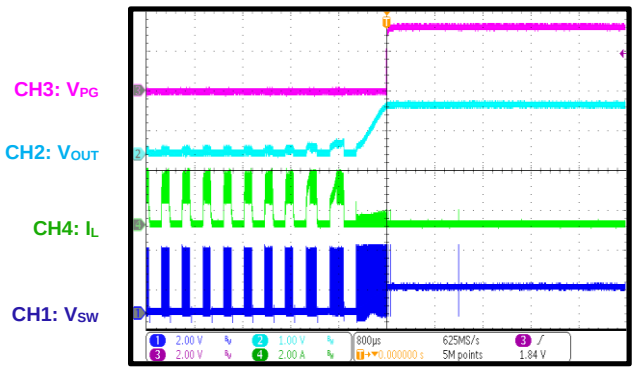
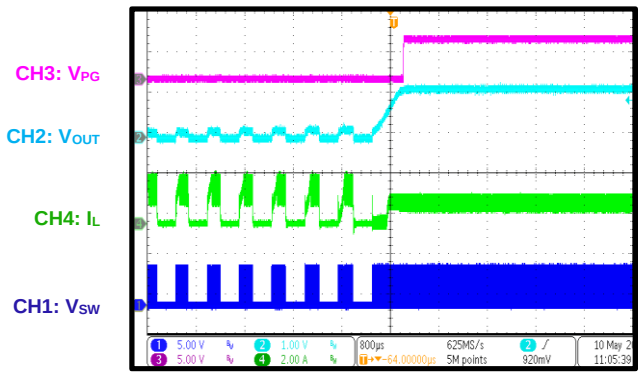
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

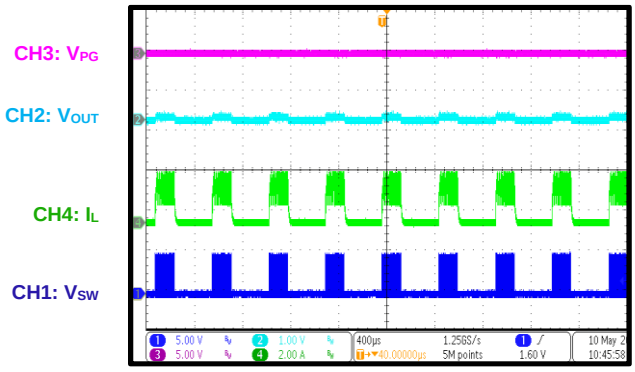
SCP Recovery
I_{OUT} = 0A



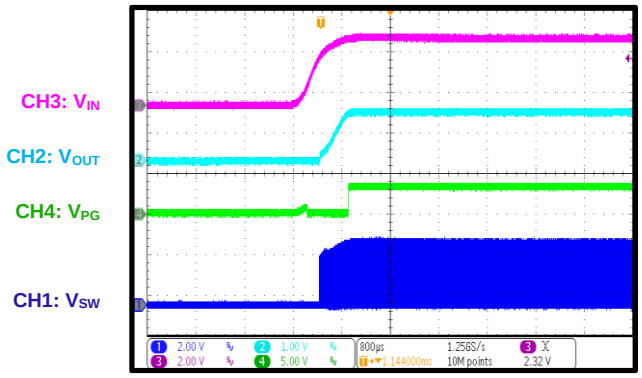
SCP Recovery
I_{OUT} = 1A



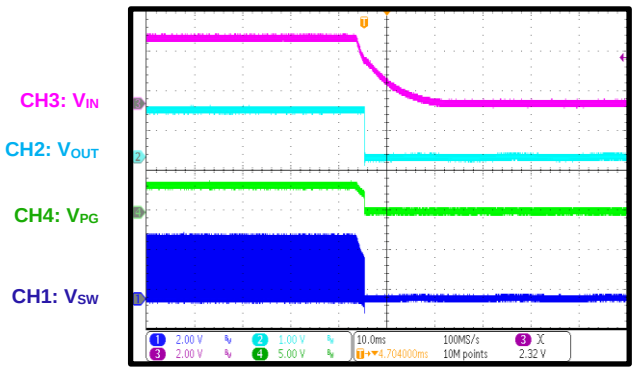
Short-Circuit Protection



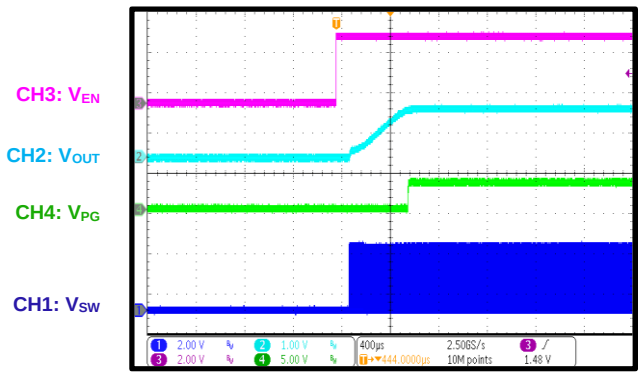
PG Start-Up through VIN
I_{OUT} = 1A



PG Shutdown through VIN
I_{OUT} = 1A



PG Start-Up through EN
I_{OUT} = 1A



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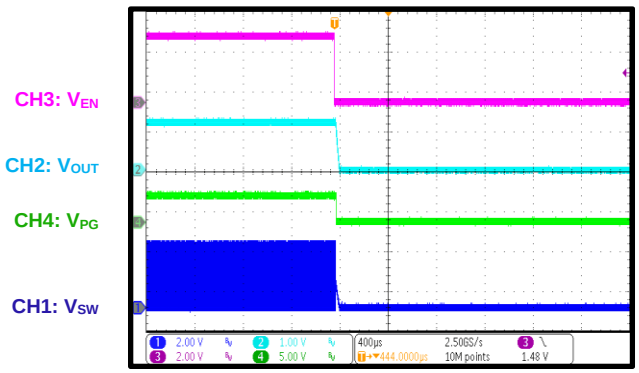
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

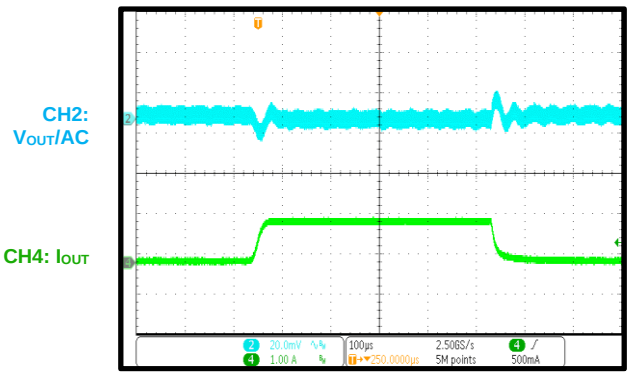
PG Shutdown through EN

I_{OUT} = 1A



Load Transient

I_{OUT} = 0A to 1A, 1A/µs



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FUNCTIONAL BLOCK DIAGRAM

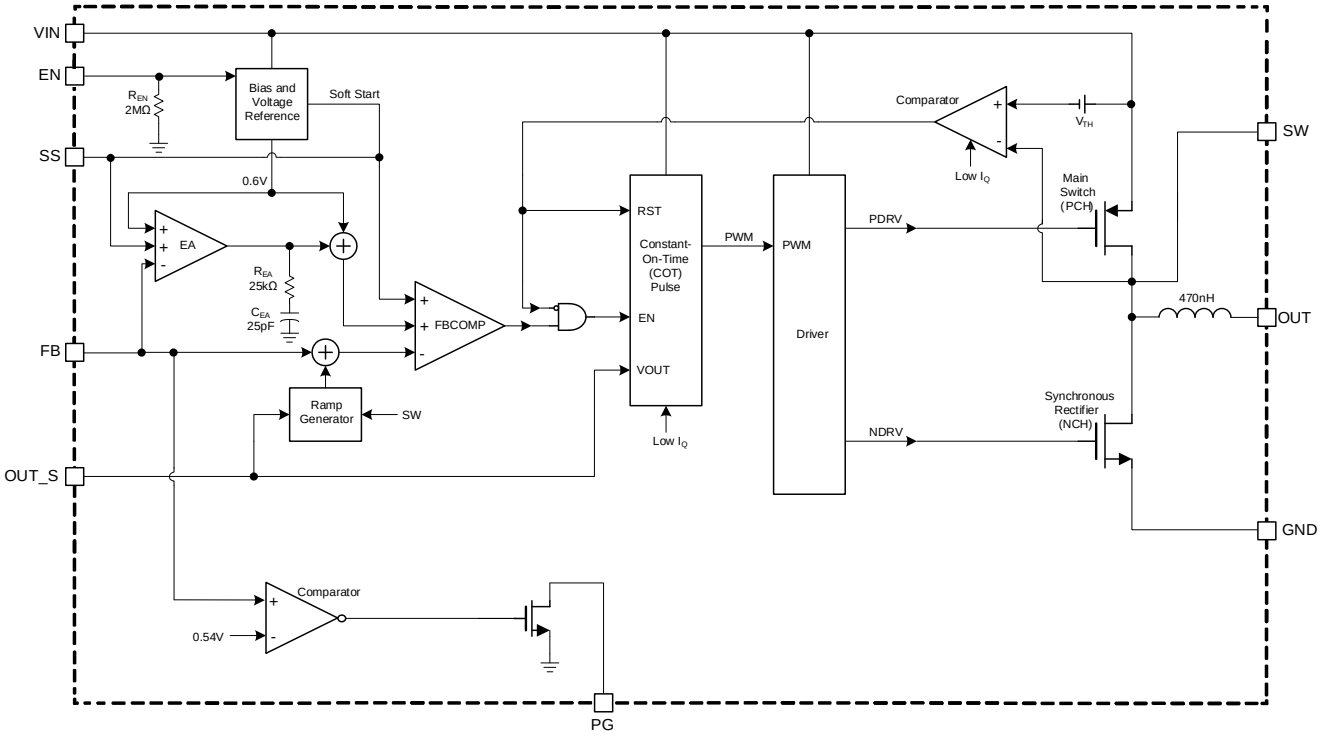

Figure 1: Functional Block Diagram (Adjustable Output)

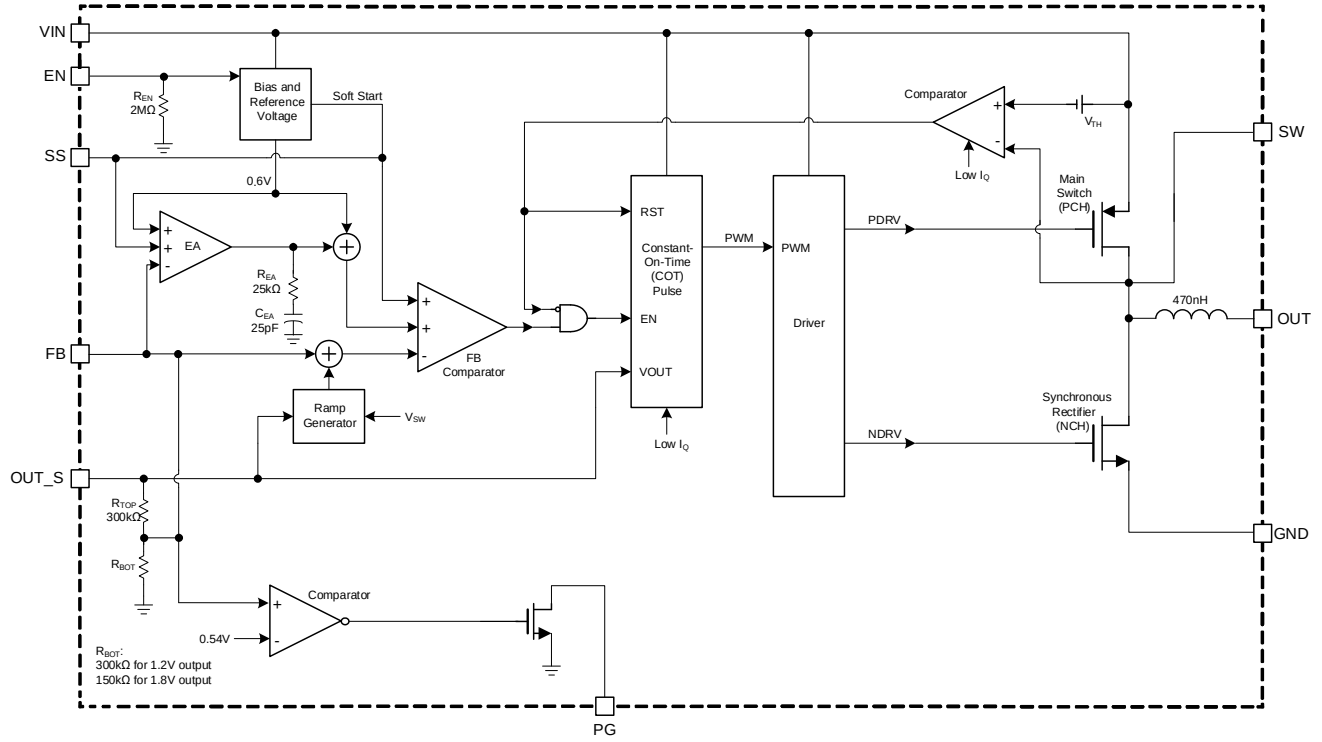

Figure 2: Functional Block Diagram (Fixed Output)

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OPERATION

The MPM3806 employs input voltage (V_{IN}) feed-forward and constant-on-time (COT) control to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. It can achieve up to 1A of output current (I_{OUT}) across a 2.5V to 5.5V V_{IN} range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V. A 100% maximum duty cycle can be achieved in low-dropout (LDO) mode.

Constant-On-Time (COT) Control

COT control provides a simple control loop and fast transient response. The switching cycles have a fixed minimum off time (t_{OFF_MIN}) to prevent inductor current (I_L) runaway during load transient. If the low-side MOSFET (LS-FET) turns on, it remains on for at least t_{MIN_OFF} (typically 80ns). The high-side MOSFET (HS-FET) turns on once the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient V_{OUT}. V_{IN} feed-forward allows the device to maintain a nearly constant f_{SW} across the V_{IN} and load ranges. The f_{SW} on time (t_{ON}) can be calculated using Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400ns \quad (1)$$

Sleep Mode

The MPM3806 employs sleep mode for high efficiency under light-load conditions. In sleep mode, most of the circuit block input currents (I_{IN}) decrease, specifically the error amplifier (EA) and pulse-width modulation (PWM) comparator.

As the load decreases, the converter's f_{SW} decreases. If the load continues to decrease and the off time (t_{OFF}) exceeds 3.5µs, then the MPM3806 enters sleep mode. To further improve light-load efficiency, the converter consumes a very low quiescent current (I_Q) while in sleep mode.

Once an HS-FET pulse occurs, the MPM3806 exits sleep mode.

Advanced Asynchronous Modulation (AAM) Mode under Light-Load Conditions

The MPM3806 features advanced asynchronous modulation (AAM) mode and a zero-current detection (ZCD) circuit for light-load operation.

The AAM current (I_{AAM}) is set internally. The SW pin's t_{ON} is determined by the on-timer generator and AAM comparator. Under light-load conditions, SW's t_{ON} exceeds the AAM comparator's t_{ON}. Figure 3 shows the simplified AAM control logic.

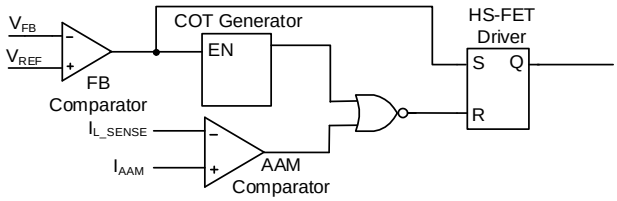

Figure 3: Simplified AAM Control Logic

If the AAM comparator's t_{ON} exceeds the on-timer's pulse, then the AAM comparator controls SW's t_{ON} (see Figure 4).

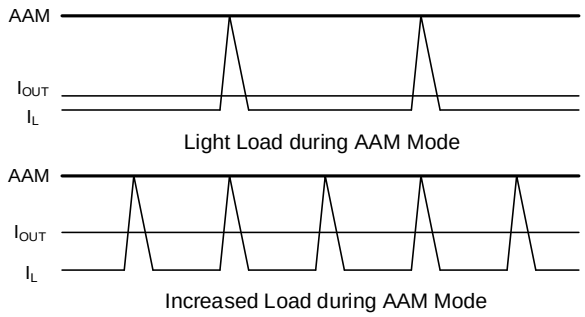

Figure 4: AAM Comparator Controls SW's t_{ON}

If the AAM comparator's t_{ON} is below the on-timer when using a lower-value inductor, the HS-FET depends on the on-timer. Therefore, the on-timer controls SW's t_{ON} (see Figure 5).

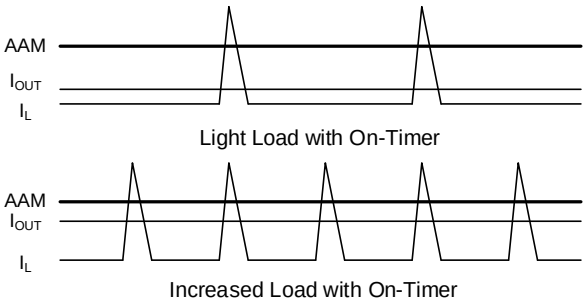

Figure 5: On-Timer Controls SW's t_{ON}

Aside from the on-timer method, the AAM circuit has another AAM blanking time (150ns) for sleep mode. This means that if the on-timer drops

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below 150ns, then the HS-FET turns off after an on-timer pulse is generated without AAM control.

In this scenario, I_L may not reach the AAM threshold (see Figure 6).

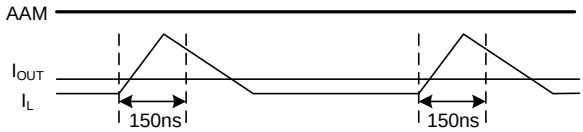

Figure 6: AAM Blanking Time during Sleep Mode

In sleep mode, the on-timer's pulse is about 40% above its pulse during discontinuous conduction mode (DCM) and continuous conduction mode (CCM). Figure 7 shows how the AAM threshold decreases as t_{ON} increases gradually. In CCM, I_{OUT} should exceed half of the AAM threshold.

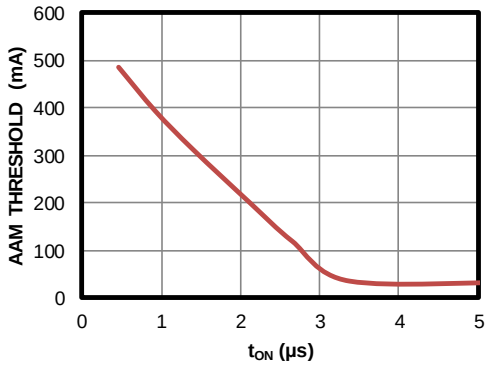

Figure 7: AAM Threshold Decreases as t_{ON} Increases

The MPM3806 employs ZCD to determine whether I_L begins to reverse. If I_L reaches the ZCD threshold (typically 50mA), then the LS-FET turns off.

Even if V_{OUT} is close to V_{IN}, AAM mode and ZCD allow the device to operate continually in DCM under light-load conditions.

Enable (EN) Control

The enable (EN) pin is a digital control pin that turns the MPM3806 on and off. Pull the EN voltage (V_{EN}) above 0.9V to turn the converter on; pull V_{EN} below 0.65V or float EN to turn it off. Pulling EN to GND also disables the device. There is an internal 2MΩ resistor connected between EN and GND.

Output Discharge

If the MPM3806 shuts down, the device initiates output discharge mode. The internal discharge MOSFET provides a resistive discharge path for the output capacitor (C_{OUT}) between the OUT_S pin and GND. To block the output discharge path, add an external capacitor between V_{OUT} and the OUT_S pin (see the Output Discharge Blocking section on page 23).

Soft Start (SS)

The MPM3806 features external soft start (SS). To avoid overshoot during start-up, the SS pin ramps up V_{OUT} at a controlled slew rate. The soft-start charge current (I_{SS}) is typically 3µA. The soft-start time (t_{SS}) is determined by the external soft-start capacitor (C_{SS}). t_{SS} can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 0.6V}{I_{SS}(\mu A)} \quad (2)$$

Where I_{SS} is the internal soft-start charge current (3µA).

It is recommended that be $C_{SS} \geq 1nF$.

The MPM3806 has a pre-biased start-up function. Once V_{EN} exceeds 0.9V, the converter starts up, regardless of any pre-biased voltage on the output. Pre-biased start-up works even while the output discharge path is blocked.

Peak Current Limit and Valley Current Limit

Both the HS-FET and LS-FET feature current-limit protection. If I_L reaches the HS-FET's peak current limit (I_{LIMIT_PEAK}) threshold (typically 2.5A), the HS-FET turns off and the LS-FET turns on to discharge the energy. The HS-FET does not turn on again until I_L drops below the valley current limit (I_{LIMIT_VALLEY}) threshold (typically 1A). This prevents current runaway during overload and short-circuit conditions. I_{LIMIT_VALLEY} is blocked unless HS-FET turns off due to the triggered I_{LIMIT_PEAK}.

Short-Circuit Protection (SCP) and Recovery

If a short-circuit condition occurs, the MPM3806 reaches its current limit (I_{LIMIT}) immediately. V_{OUT} drops until V_{FB} drops below 50% of V_{REF}, which is considered an output dead short. Short-circuit protection (SCP) with hiccup mode is triggered to periodically restart the part. In hiccup mode, the output power stage is disabled, and the soft-start voltage (V_{SS}) is discharged. Once V_{SS} is discharged completely, the device initiates a new SS. This process repeats until the fault condition is removed.

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Over-Voltage Protection (OVP)

The MPM3806 monitors V_{FB} to detect over-voltage (OV) conditions. If V_{FB} exceeds 115% of V_{REF}, then the converter enters its dynamic regulation period. During this period, the LS-FET remains on until its current reaches -1.2A. This process discharges V_{OUT} to keep it within its normal range. If the OV condition still remains after this process, there is a 1.5µs delay before the LS-FET turns on again. Once V_{FB} drops below 105% of V_{REF}, the converter exits the regulation period. If the dynamic regulation period cannot prevent V_{OUT} from increasing, and a 6.1V V_{IN} is detected, then over-voltage protection (OVP) is triggered. The device stops switching until V_{IN} drops below 6V. Once V_{IN} drops below 6V, the MPM3806 resumes normal operation.

Power Good (PG) Indicator

The MPM3806 has a power good (PG) output that indicates whether the converter is operating normally after start-up. PG is the open drain of an internal MOSFET. It is recommended that this MOSFET's maximum on resistance be below 400Ω. PG can be connected to V_{IN} or an external voltage source via an external resistor (10kΩ to 100kΩ). Once V_{IN} is applied, the MOSFET turns on and PG is pulled to GND before SS is ready. Once V_{FB} reaches 90% of V_{REF}, PG is pulled high by the external voltage source. If V_{FB} drops to 85% of V_{REF}, then the PG voltage (V_{PG}) is pulled to GND to indicate an output failure.

If V_{IN} and V_{EN} are not available, and PG is pulled up via an external power supply, then PG self-biases and asserts. If a 100kΩ pull-up resistor is being used, then V_{PG} should be below 0.7V.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the MPM3806's adjustable V_{OUT}. Select a FB resistor (R4) to reduce the V_{OUT} leakage current (typically between 10kΩ and 100kΩ). R5 can then be calculated using Equation (3):

$$R5 = \frac{R4}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

Figure 8 shows the FB network.

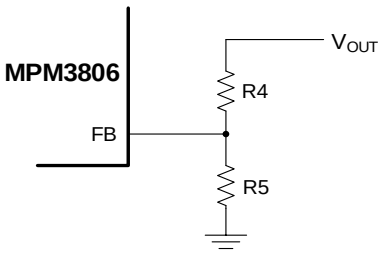

Figure 8: Feedback Network

Table 1 shows the recommended resistances for common output voltages.

Table 1: Resistances for Common Output Voltages

V_{OUT} (V)	R4 (kΩ)	R5 (kΩ)
1	30.9 (1%)	47 (1%)
1.2	100 (1%)	100 (1%)
1.8	36 (1%)	18 (1%)
2.5	51 (1%)	16 (1%)
3.3	68 (1%)	15 (1%)

For the fixed-output version of the MPM3806, it is not necessary to connect the external resistor divider. Do not float the FB pin.

Frequency Scaling at Low Input Voltages

Under heavy-load conditions, the HS-FET voltage decreases as t_{ON} increases, and the duty cycle is extended. If t_{OFF_MIN} is reached at a low V_{IN} under heavy-load conditions, then f_{SW} scales down. To maintain a constant f_{SW} at heavy loads, a larger V_{OUT} is required for a larger V_{IN}. For a 1.8V V_{OUT} at a 1A load, V_{IN} should be above 2.9V to keep f_{SW} above 2MHz. If f_{SW} begins to scale down, V_{IN} can be estimated with Equation (4):

$$V_{IN} = \frac{V_{OUT} + R_{DS(ON)\_HS} \times I_{OUT}}{1 - \frac{t_{OFF\_MIN}}{400 \times 10^{-9}}} \quad (4)$$

Where the maximum t_{OFF_MIN} is 125ns. (10)

Note:

10) Guaranteed by design and bench characterization. Not tested in production.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, it is recommended to use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. Higher output voltages may require a 22µF capacitor to increase system stability.

The input capacitor (C_{IN}) requires an adequate ripple current rating to absorb the switching I_{IN}.

The input capacitor's RMS current rating (I_{CIN}) can be estimated using Equation (5):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated using Equation (6):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current that exceeds half of the maximum load current.

C_{IN} can be an electrolytic, tantalum, or ceramic capacitor. When using electrolytic or tantalum capacitors, place a small, high-quality, 0.1µF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that the capacitor has enough capacitance to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) can be estimated using Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

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Selecting the Output Capacitor

The output capacitor (C_{OUT}) stabilizes the DC V_{OUT}. It is recommended to use ceramic capacitors for C_{OUT}, particularly low-ESR capacitors as they effectively limit the output voltage ripple (ΔV_{OUT}). ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (8)$$

Where L_1 is the inductance, and R_{ESR} is the output capacitor's ESR.

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of C_{OUT} can also affect the regulation system's stability.

Output Discharge Blocking

If the device is disabled, an internal resistive discharge path between the OUT_S pin and GND is enabled to discharge C_{OUT}. The discharge path can be blocked by adding an external capacitor between V_{OUT} and the OUT_S pin (see Figure 9).

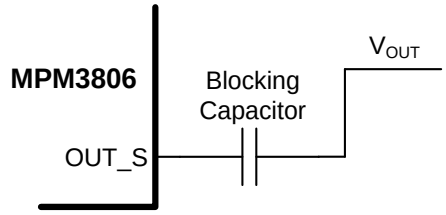

Figure 9: Circuit with V_{OUT} Discharge Blocking

Discharge blocking is only supported by the adjustable-output version. For the fixed-output versions, connect the OUT_S pin directly to the output to regulate V_{OUT}.

To avoid influencing the loop and load transient, choose the blocking capacitor to be between 10nF and 100nF. A larger-value blocking capacitor does not have an impact on loop performance, but is physically larger and is typically unnecessary for the best results.

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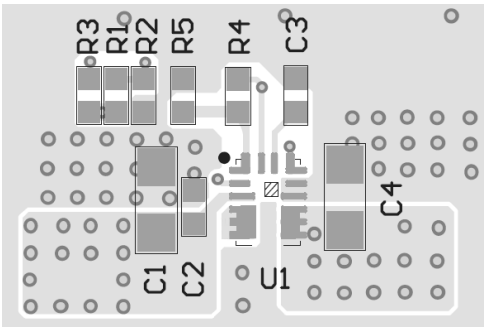
PCB Layout Guidelines (11)

Efficient PCB layout is critical for stable operation. The MPM3806's integrated inductor simplifies the schematic and layout design, but some considerations should still be taken to ensure proper operation. A 4-layer layout is recommended to reduce EMC and improve thermal performance. For the best results, refer to Figure 10 and follow the guidelines below:

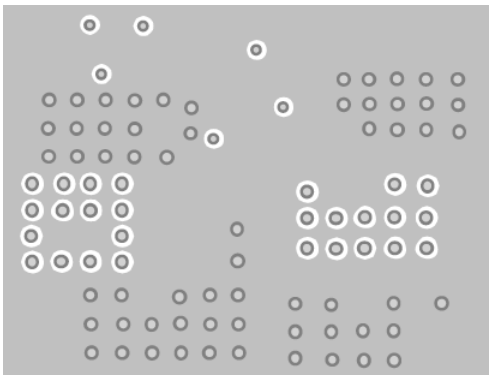
1. Place the high-current paths (GND and VIN) very close to the IC using short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to VIN as possible.
4. Place several vias close to the capacitor's GND terminal and the GND pin on the IC to reduce high-frequency noise.
5. Place the FB resistors as close to the FB pin as possible to make the FB trace as short as possible.
6. Use multiple vias to connect the power planes to the internal layer.

Note:

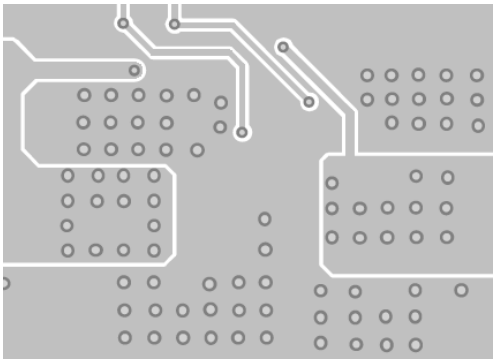
11) The recommended PCB layout is based on Figure 11 on page 25.



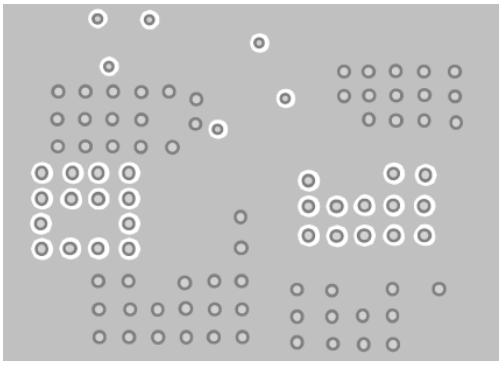
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 10: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

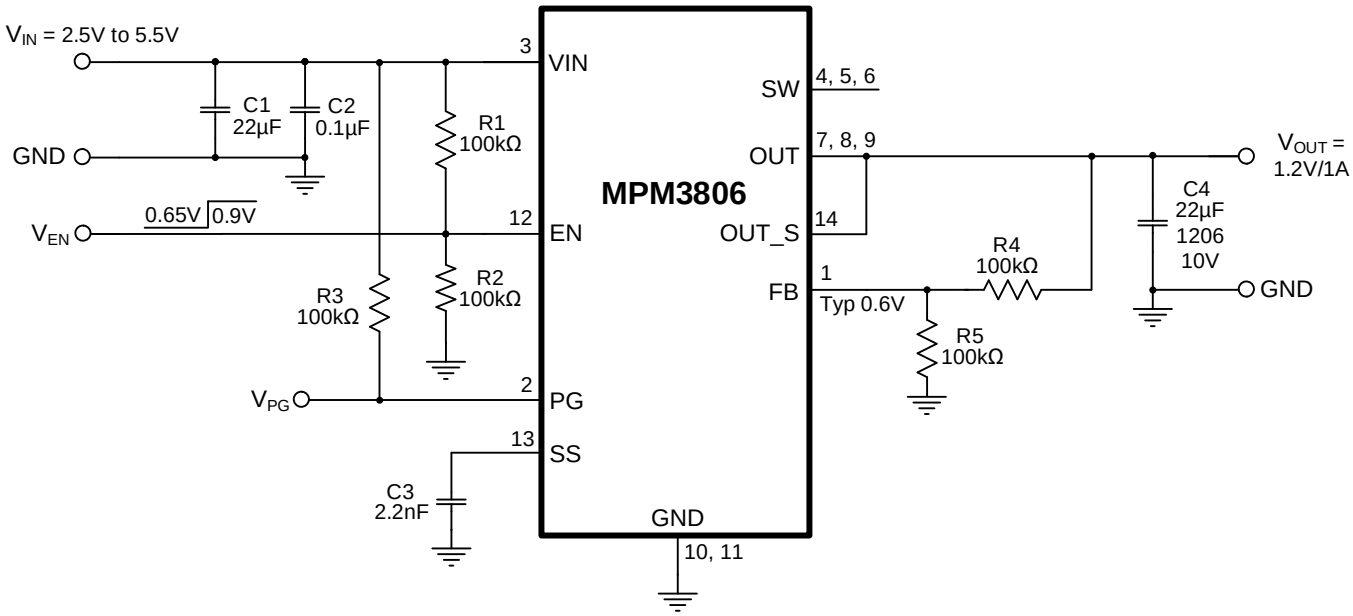

Figure 11: Typical Application (Adjustable Output, V_{OUT} = 1.2V)

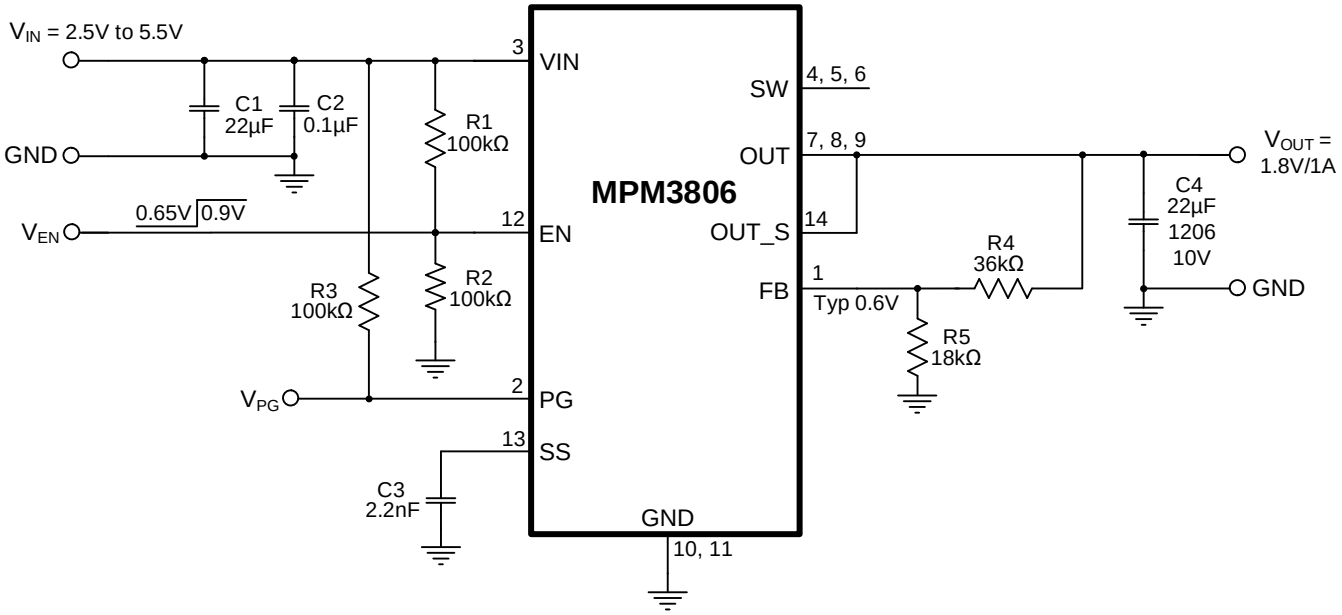

Figure 12: Typical Application (Adjustable Output, V_{OUT} = 1.8V)

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TYPICAL APPLICATION CIRCUITS *(continued)*

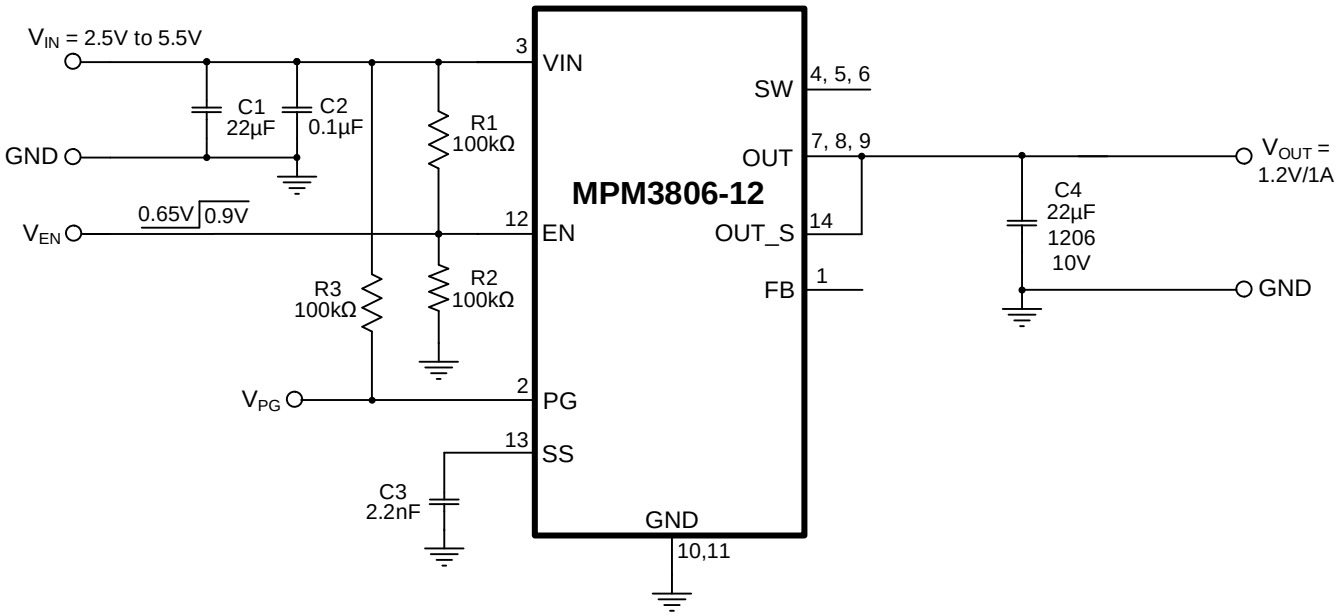

Figure 13: Typical Application (Fixed Output, V_{OUT} = 1.2V)

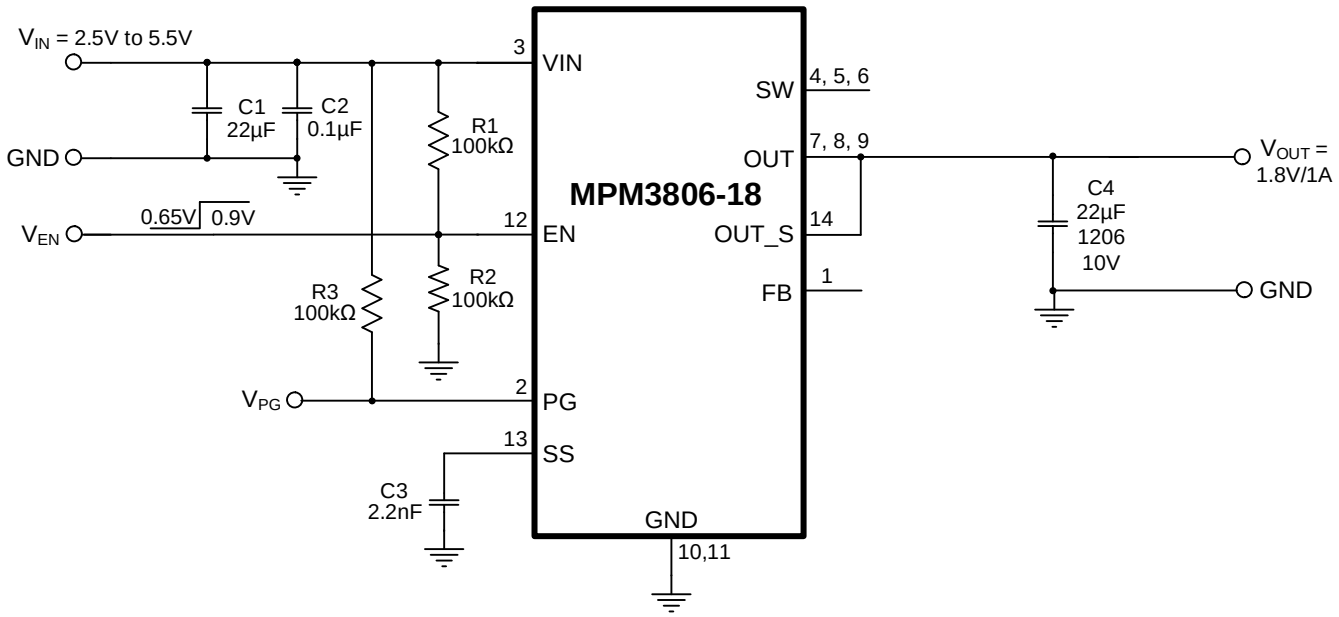

Figure 14: Typical Application (Fixed Output, V_{OUT} = 1.8V)

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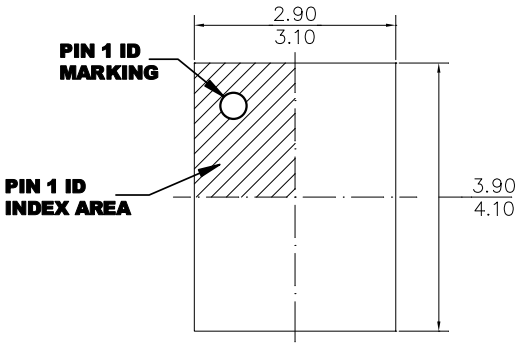
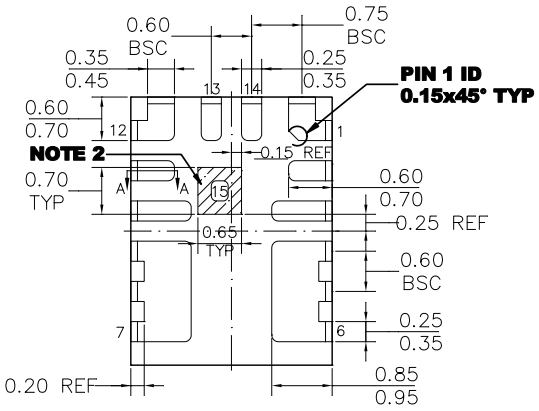
PACKAGE INFORMATION

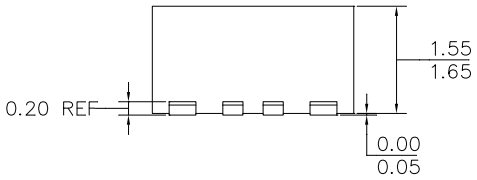
QFN-15 (3mmx4mmx1.6mm)
Wettable Flank



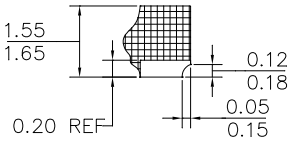
TOP VIEW



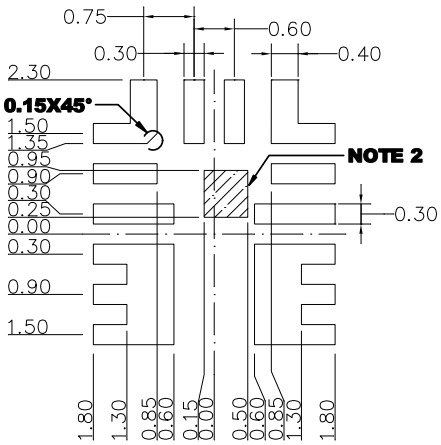
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) THE LEAD SIDE IS WETTABLE.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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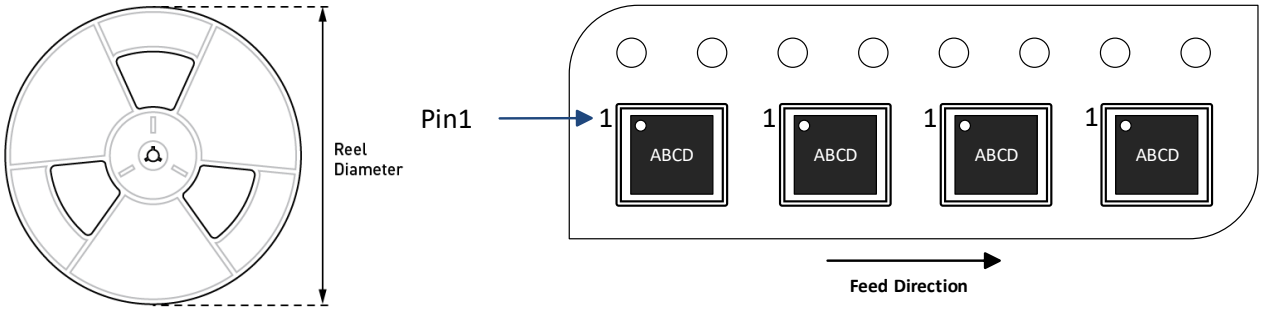
CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3806GLE-AEC1-Z	QFN-15 (3mmx4mmx1.6mm)	2500	N/A	N/A	13in	12mm	8mm
MPM3806GLE-12-AEC1-Z							
MPM3806GLE-18-AEC1-Z							

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/7/2022	Initial Release	-

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