MP2276

8A, 2.7-16V Input, High-Efficiency Synchronous Step-down Converter with Programmable Current Limit and Soft Start Time Selectable Frequency and Mode of Operation

The Future of Analog IC Technology

DESCRIPTION

The MP2276 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. It offers a very compact solution that achieves up to 8A of continuous output current with excellent load and line regulation over a wide input supply range. The MP2276 operates at high efficiency over a wide output current load range.

The MP2276 uses constant-on-time (COT) control for fast transient response and eased loop stabilization.

Output voltage start-up is controlled by an internal 1.7ms timer, which can be increased by adding a capacitor on SS/TRK. An open-drain power good (PG) signal indicates when the output is within its nominal voltage range.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MP2276 requires a minimal number of readily available, standard, external components and is available in a QFN-14 (2mmx3mm) package.

FEATURES

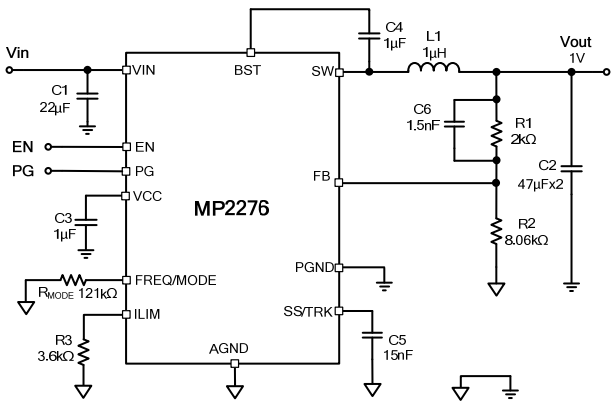
- Wide 2.7V to 16V Input Voltage Range
- 8A Continuous Output Current
- 24mΩ/10mΩ Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Adaptive Constant-On-Time (COT) for Ultrafast Transient Response
- Stable with Zero ESR Output Capacitor
- Programmable Current Limit
- Selectable Forced CCM or Pulse-Skip Operation at Light Load
- Excellent Load Regulation
- Programmable Soft-Start Time from 1.7ms
- Pre-Bias Start-Up
- Selectable 600kHz, 1100kHz, or 2000kHz Switching Frequency
- Hiccup Over-Current Protection (OCP)
- Auto-Retry Over-Voltage Protection (OVP) and Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN-14 (2mmx3mm) Package

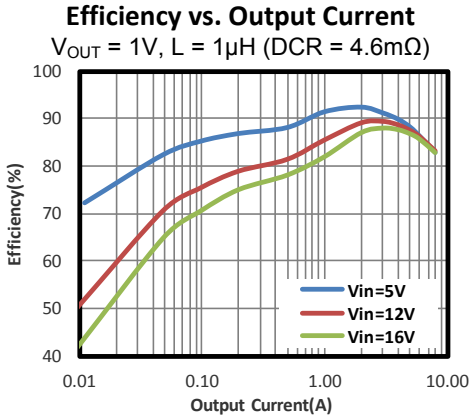
APPLICATIONS

- Digital Set-Top Boxes
- Flat-Panel TV and Monitors
- Distributed Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2276GD	QFN-14 (2mmx3mm)	*See Below*

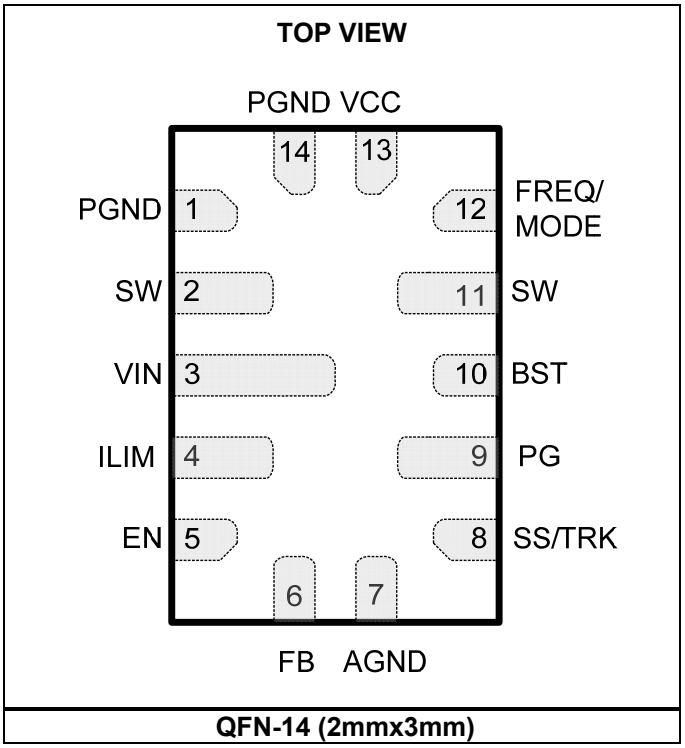
* For Tape & Reel, add suffix –Z (e.g. MP2276GD–Z)

TOP MARKING

AUM
YWW
LLL

AUM: Product code of MP2276GD
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx3mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 18V
V_{SW} (DC) .....-0.3V to VIN + 0.3V
V_{SW} (25ns).....-5V to 25V
V_{BST} ..... V_{SW} + 4V
VCC 4V
EN current (I_{EN}) 300µA
All other pins .....-0.3V to VCC + 0.3V
Continuous power dissipation (T_A = +25°C) (2)
..... 2.7W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (VIN).....2.7V to 16V(4)
Output voltage (V_{OUT}).....0.8V to 6V
EN current (I_{EN}) 100µA
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance

QFN-14 (2mmx3mm)	***θ_{JA}***	***θ_{JC}***	
EV2276-D-00A	40	10	°C/W
JESD51-7	46	9	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) For VIN≤3.3V application, please connect VIN to VCC directly. And 2.7V is only a typical value for minimum supply voltage at VIN falling.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C [5], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VIN Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		0	1	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 0.82V		600		μA
MOSFETs						
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 3.3V		24		mΩ
LS switch on resistance	LS_{RDS-ON}	VCC = 3V		10		mΩ
Current Limit						
Current limit threshold	V_{LIM}			1.2		V
I_{ILIM} to I_{OUT} ratio	I_{ILIM}/I_{OUT}	I_{OUT} ≥ 2A	36	40	44	μA/A
Low-side negative current limit	$I_{LIM\ NEG\ 10}$			-4		A
Negative current limit timeout [6]	$t_{NCL\ Timer}$			80		ns
Timer						
Switching frequency	f_{SW}	FREQ/MODE = AGND	900	1100	1300	kHz
		FREQ/MODE = 60.4kΩ to AGND	530	600	790	kHz
Minimum on time [6]	$T_{ON\ MIN}$				50	ns
Minimum off time [6]	$T_{OFF\ MIN}$				180	ns
Over-Voltage (OVP) and Under-Voltage Protection (UVP)						
OVP threshold	V_{OVP}		111%	116%	121%	V_{REF}
UVP threshold	V_{UVP}		75%	80%	85%	V_{REF}
Soft Start (SS)						
Soft-start time	t_{SS}	C_{SS} = 3.3nF, V_{OUT} from 10% to 90%		1.7		ms
Error Amplifier (EA)						
Feedback voltage	V_{FB}	T_A = 25°C	792	800	808	mV
Enable (EN)						
Enable input rising threshold	VIH_{EN}		1.15	1.21	1.27	V
Enable hysteresis	V_{EN-HYS}			220		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		μA
Soft shutdown discharge FET	$R_{ON\ DISCH}$			80		Ω
VCC Regulator						
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.65	2.8	2.95	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}			280		mV
VCC output voltage	V_{CC}			3.00		V
VCC load regulation		I_{CC} = 5mA		0.5		%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, T_J = -40°C to +125°C [5], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal shutdown [6]	T_{SD}			150		°C
Thermal shutdown hysteresis [6]	$T_{SD\ HYS}$			20		°C
Power Good (PG)						
Power good high threshold	$PG_{Vth\ Hi\ Rise}$	FB from low to high	87.5%	92.5%	97.5%	V_{REF}
Power good low threshold	$PG_{Vth\ Lo\ Rise}$	FB from low to high	111%	116%	121%	V_{REF}
	$PG_{Vth\ Lo\ Fall}$	FB from high to low	75%	80%	85%	V_{REF}
Power good low to high delay	PG_{Td}		0.7	1.0	1.3	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.4	V
Power good leakage current	$I_{PG\ LEAK}$	V_{PG} = 3V			3	µA
Power good low-level output voltage	V_{OL_100}	VIN = 0V, pull PG up to 3.3V through a 100kΩ resistor		650	900	mV
	V_{OL_10}	VIN = 0V, pull PG up to 3.3V through a 10kΩ resistor		800	1050	

NOTES:

5) Not tested in production, guaranteed by over-temperature correlation.
6) Guaranteed by engineering sample characterization.

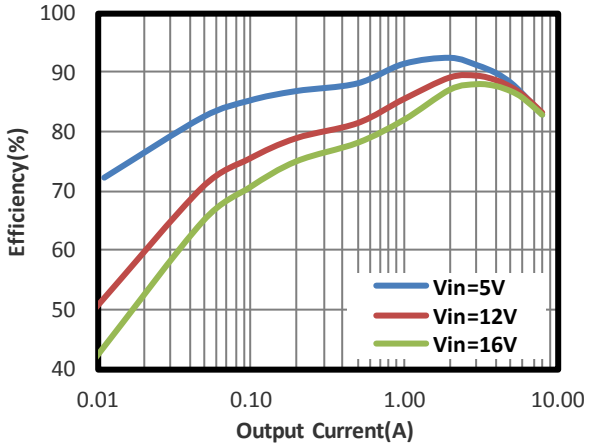
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

VIN = 12V, V_{OUT} = 1V, L = 1µH, F_{SW} = 600kHz, pulse-skip mode, T_A = +25°C, unless otherwise noted.

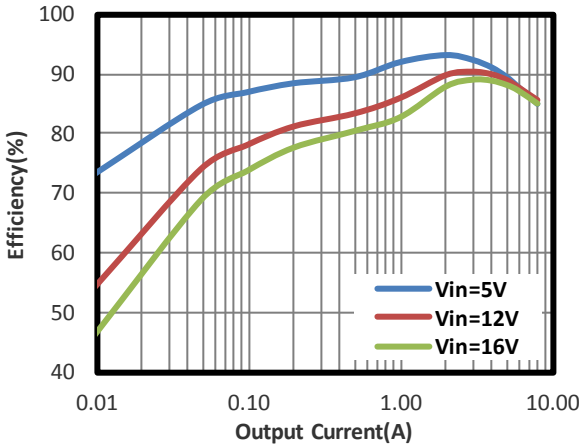
Efficiency vs. Output Current

V_{OUT} = 1V, L = 1µH (DCR = 4.6mΩ)



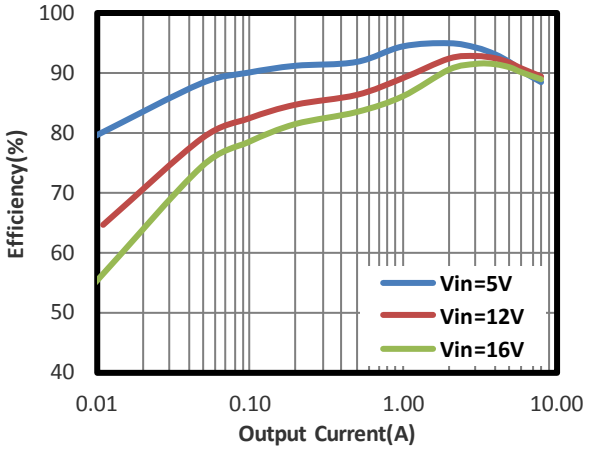
Efficiency vs. Output Current

V_{OUT} = 1.2V, L = 1µH (DCR = 4.6mΩ)



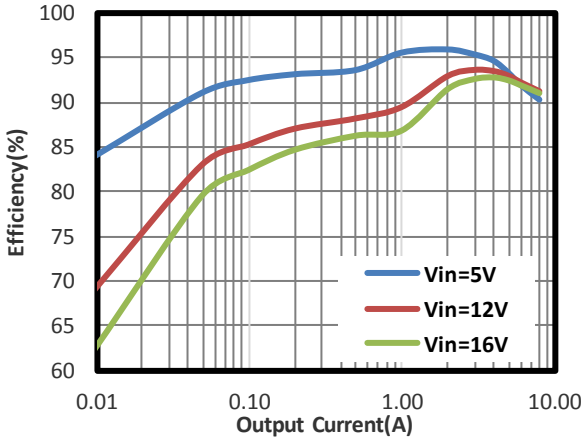
Efficiency vs. Output Current

V_{OUT} = 1.8V, L = 1.5µH (DCR = 4.3mΩ)



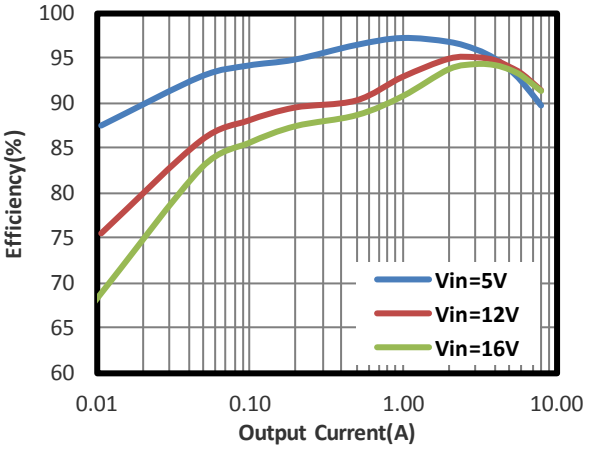
Efficiency vs. Output Current

V_{OUT} = 2.5V, L = 1.5µH (DCR = 4.3mΩ)



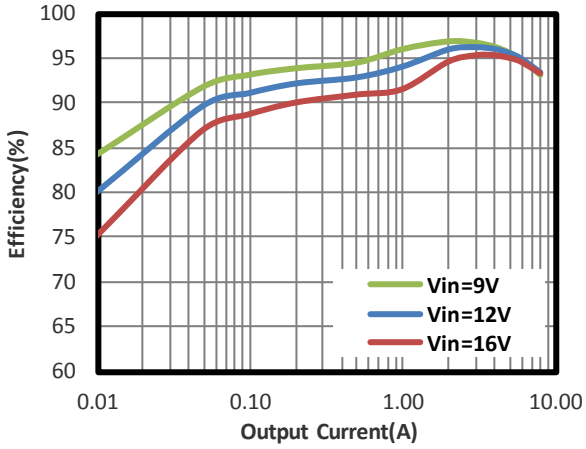
Efficiency vs. Output Current

V_{OUT} = 3.3V, L = 2.2µH (DCR = 11.4mΩ)



Efficiency vs. Output Current

V_{OUT} = 5V, L = 2.2µH (DCR = 11.4mΩ)

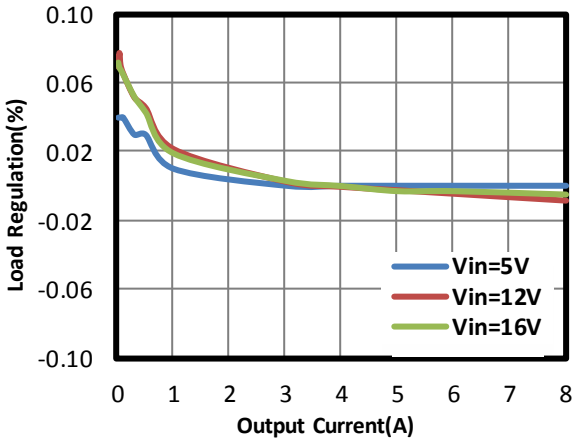


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

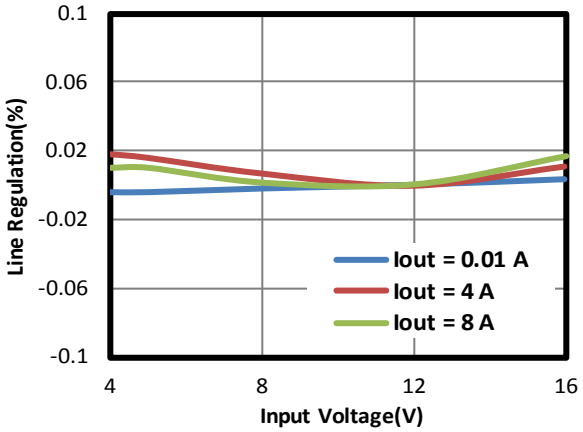
TYPICAL CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1V, L = 1µH, F_{SW} = 600kHz, pulse-skip mode, T_A = +25°C, unless otherwise noted.

Load Regulation

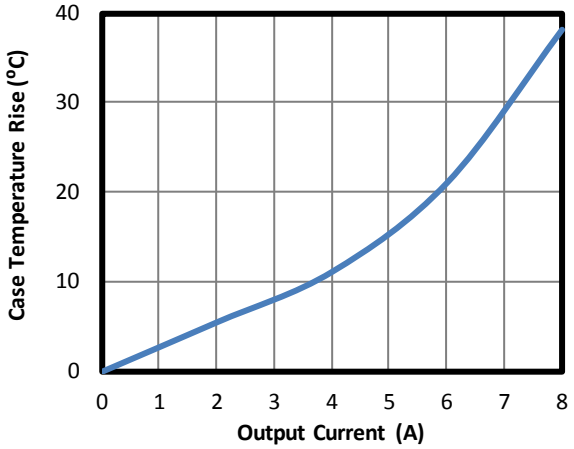


Line Regulation



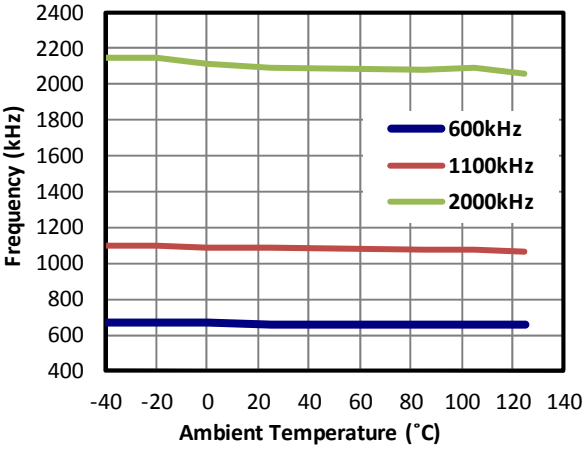
Case Temperature Rise vs. Output Current

4-Layer PCB, Size is 7.75cmx8.13cm

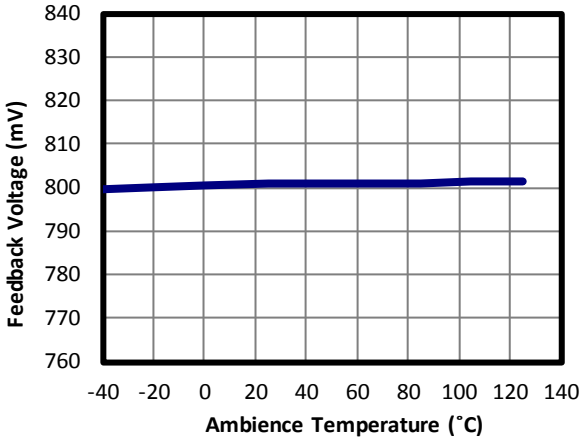


Switching Frequency vs. Temperature

Forced CCM, No Load

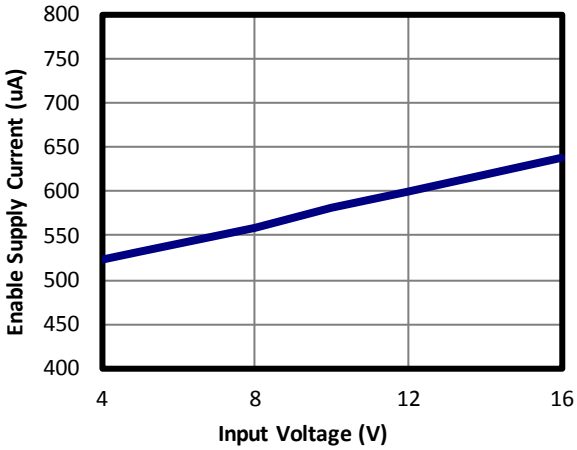


FB Voltage vs. Temperature



Enable Supply Current vs. Input Voltage

V_{FB} = 0.82V, V_{EN} = 2V



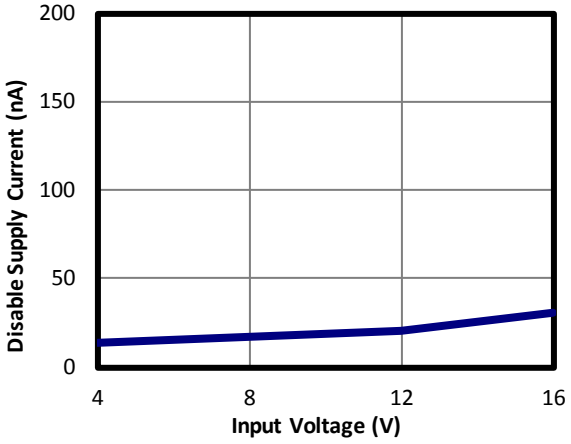
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1V, L = 1µH, F_{SW} = 600kHz, pulse-skip mode, T_A = +25°C, unless otherwise noted.

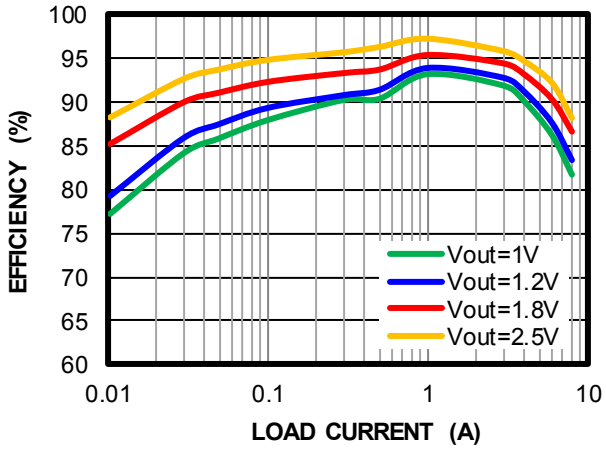
Disabled Supply Current vs. Input Voltage

V_{EN} = 0V



Efficiency vs. Output Current

V_{IN}=3.3V, VCC=VIN, L=0.68µH (DCR=3.1mΩ)



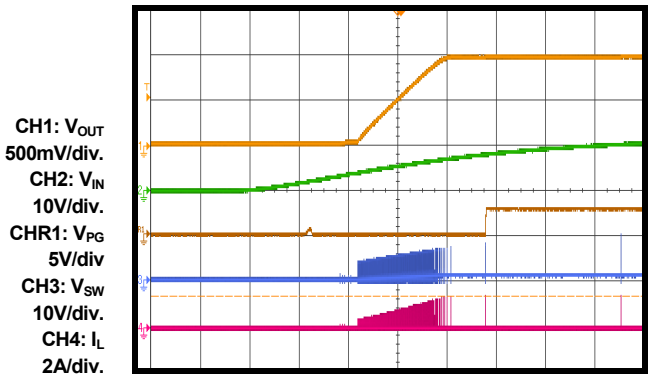
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section. VIN = 12V, V_{OUT} = 1V, L = 1µH, F_{SW} = 600kHz, pulse-skip mode, T_A = +25°C, unless otherwise noted.

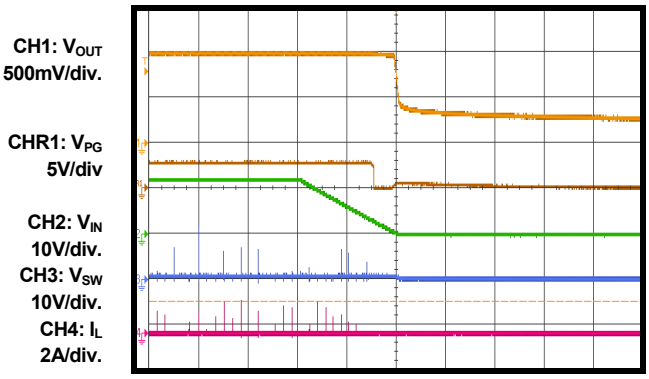
Start-Up through Input Voltage

I_{OUT} = 0A



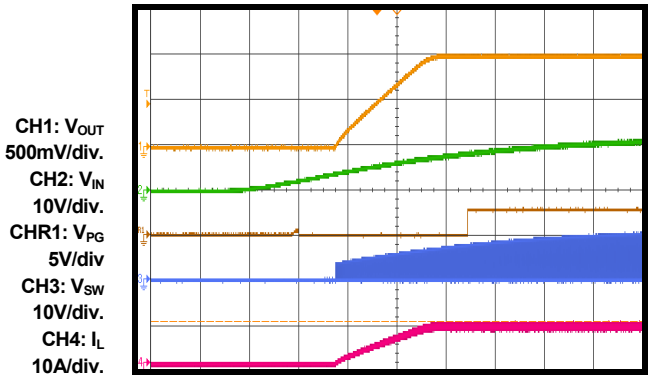
Shutdown through Input Voltage

I_{OUT} = 0A



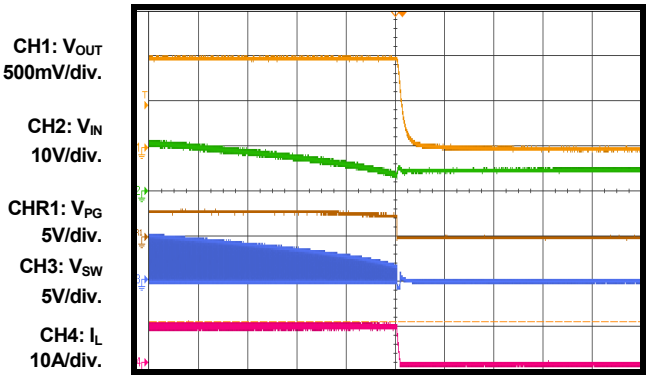
Start-Up through Input Voltage

I_{OUT} = 8A



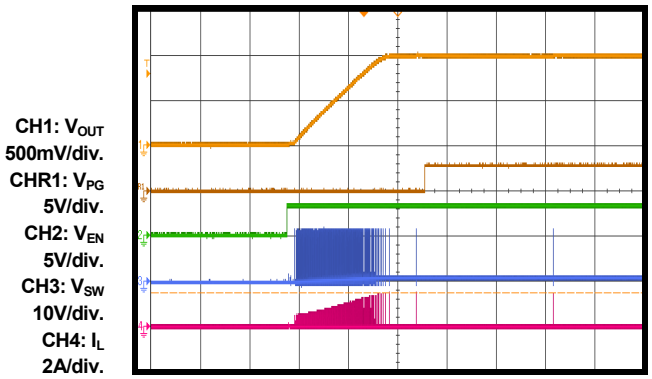
Shutdown through Input Voltage

I_{OUT} = 8A



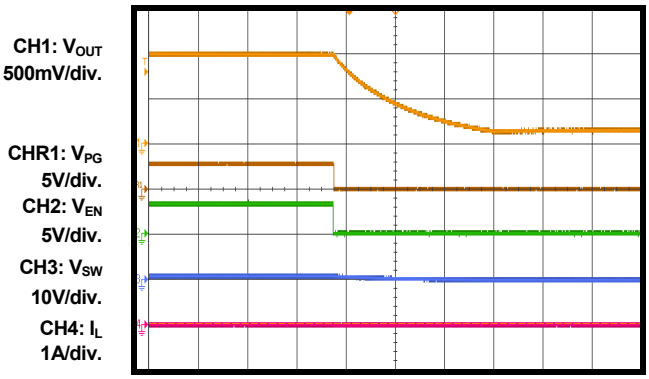
Start-Up through Enable

I_{OUT} = 0A



Shutdown through Enable

I_{OUT} = 0A



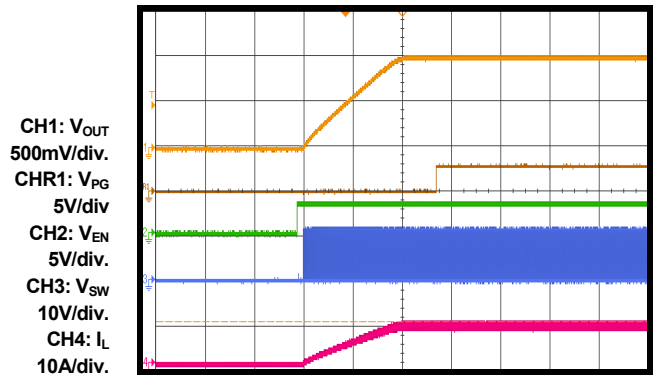
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section. VIN = 12V, V_{OUT} = 1V, L = 1µH, F_{SW} = 600kHz, pulse-skip mode, T_A = +25°C, unless otherwise noted.

Start-Up through Enable

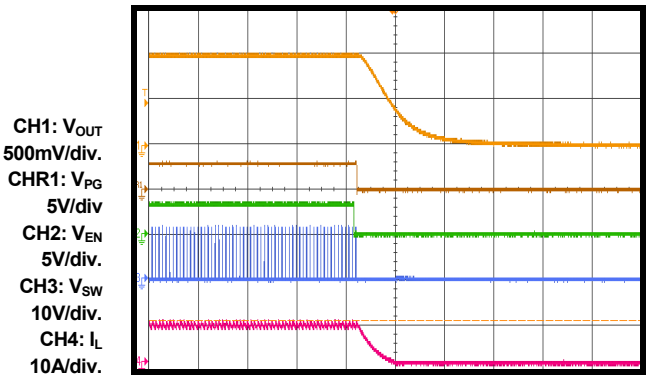
I_{OUT} = 8A



1ms/div.

Shutdown through Enable

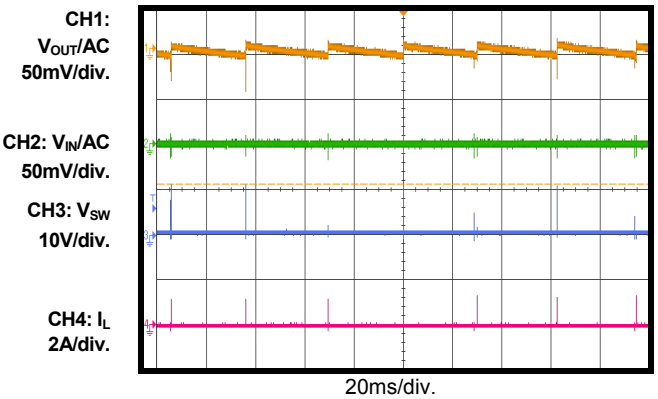
I_{OUT} = 8A



20µs/div.

Input/Output Ripple

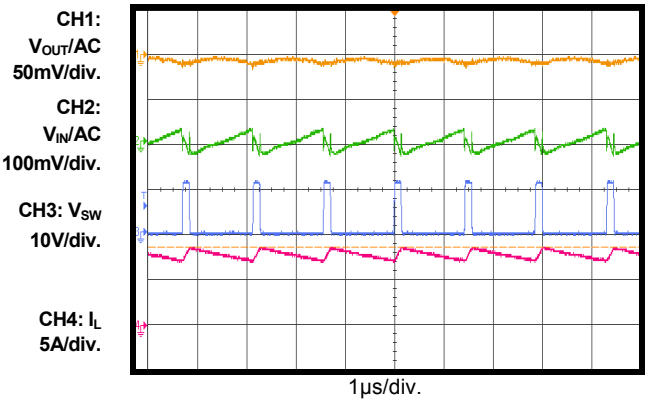
I_{OUT} = 0A



20ms/div.

Input/Output Ripple

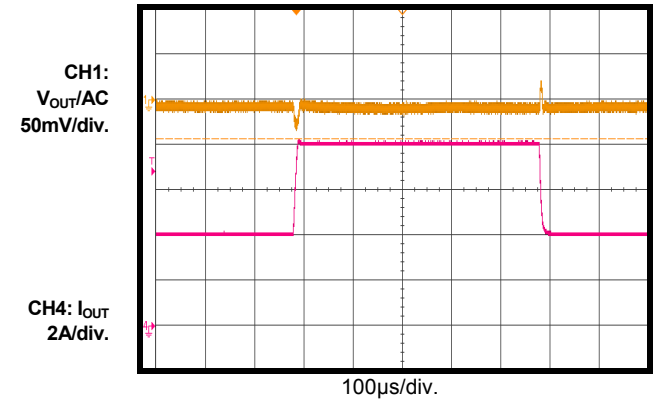
I_{OUT} = 8A



1µs/div.

Transient Response

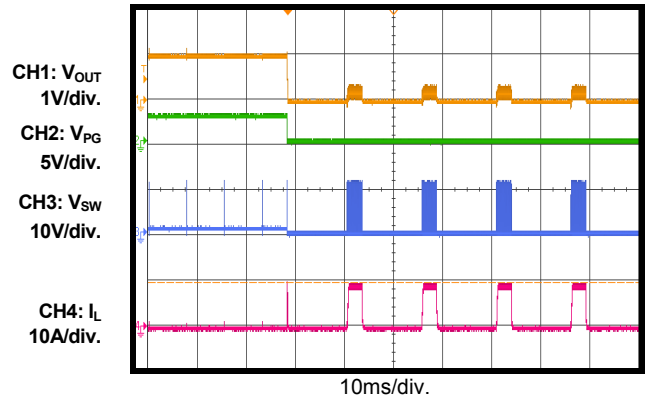
I_{OUT} = 4A - 8A, Slew Rate = 2.5A/µs by Eload



100µs/div.

Short-Circuit Entry

I_{OUT} = 0A



10ms/div.

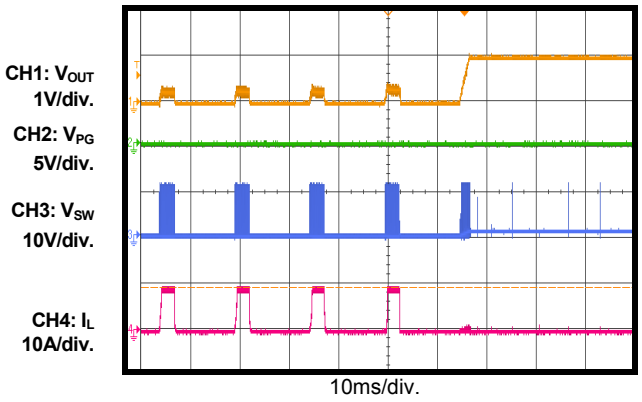
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section. VIN = 12V, V_{OUT} = 1V, L = 1µH, F_{SW} = 600kHz, pulse-skip mode, T_A = +25°C, unless otherwise noted.

Short-Circuit Recovery

I_{OUT} = 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1, 14	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during PCB layout. Connect using wide PCB traces.
2, 11	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW negative during the off-time. Connect using wide PCB traces.
3	VIN	**Supply voltage.** VIN supplies power to the internal MOSFET and regulator. Decouple the input rail with an input capacitor. Connect using wide PCB traces and multiple vias.
4	ILIM	**Current limit.** Connect a resistor from ILIM to ground to set the current limit trip point.
5	EN	**Enable.** EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN.
6	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage. Place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
7	AGND	**Analog ground.** Select AGND as the control circuit reference point.
8	SS/TRK	**External tracking voltage input.** The output voltage tracks this input signal. Decouple SS/TRK with a ceramic capacitor as close to it as possible. Ceramic capacitors with X7R or X5R grade dielectrics are recommended for their stable temperature characteristics. The capacitance of this capacitor determines the soft-start time. See the Soft Start section on page 15 for details.
9	PG	**Power good output.** PG is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate high if the output voltage is within regulation. There is a delay of about 1ms from the time FB ≥ 92.5% to PG pulling high.
10	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
12	FREQ/MODE	**Operation mode selection.** Program FREQ/MODE to select CCM or pulse-skip mode and the operating switching frequency. See Table 1 on page 15 for details.
13	VCC	**Internal 3V LDO output.** VCC supplies power to the driver and control circuits. Decouple VCC with a minimum 1μF ceramic capacitor as close to it as possible. Ceramic capacitors with X7R or X5R grade dielectrics are recommended for their stable temperature characteristics.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

BLOCK DIAGRAM

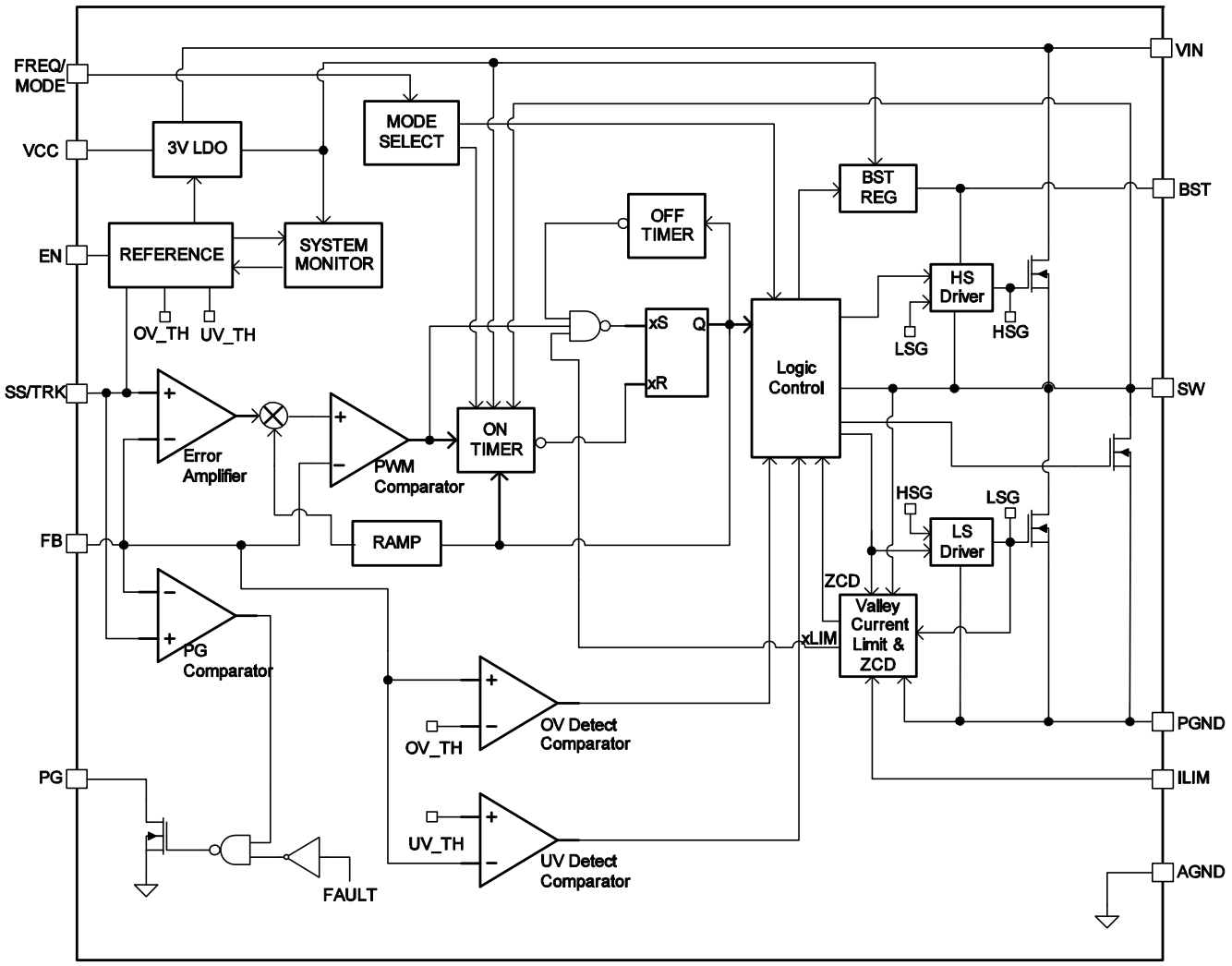


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

OPERATION

Constant-On-Time (COT) Control

The MP2276 employs constant-on-time (COT) control to achieve a fast load transient response. Figure 2 shows details of the control stage of the MP2276.

The operational amplifier (AMP) corrects any error voltage between FB and V_{REF}. The MP2276 can use AMP to provide excellent load regulation over the entire load range, whether it is operating in forced continuous conduction mode (CCM) or pulse-skip mode.

The MP2276 has internal RAMP compensation to support low ESR MLCC output capacitor solutions. The adaptive internal RAMP is optimized so that the MP2276 is stable in the entire operating input/output voltage range with a proper design of the output L/C filter.

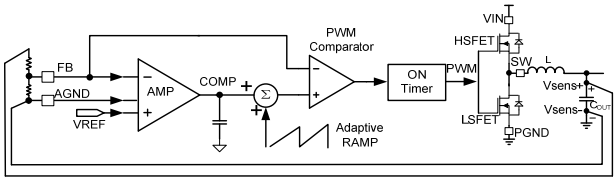


Figure 2: COT Control

Pulse-Width Modulation (PWM) Operation

Figure 3 shows how the pulse-width modulation (PWM) signal is generated. AMP corrects any error between FB and REF and generates a fairly smooth DC voltage (COMP). The internal RAMP is superimposed onto COMP. The superimposed COMP is compared with the FB signal. Whenever FB drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) turns on and remains on for a fixed turn-on time. The fixed on time is determined by the input voltage, output voltage, and selected switching frequency. After the on period elapses, the HS-FET turns off. The HS-FET turns on again when FB drops below the superimposed COMP. By repeating this operation, the MP2276 regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

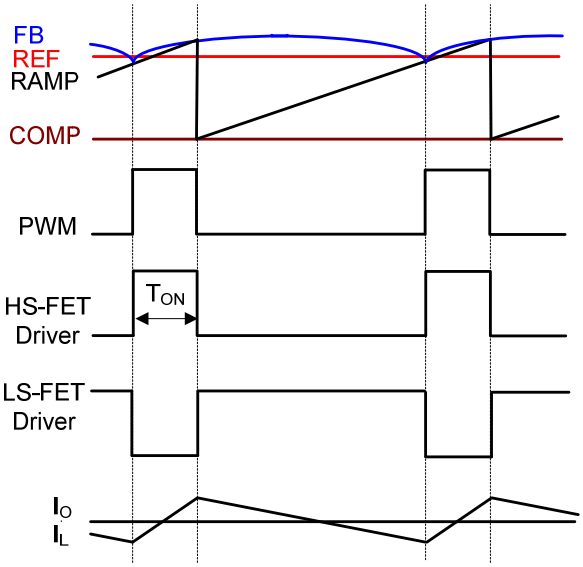


Figure 3: Heavy-Load Operation (PWM)

Continuous Conduction Mode (CCM) Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps (see Figure 3). The MP2276 can also be configured to operate in forced CCM operation when the output current is low. See the FREQ/MODE Selection section on page 15 for details.

In CCM operation, the switching frequency is fairly constant (PWM mode), so the output ripple remains almost constant throughout the entire load range.

Pulse-Skip Operation

At light-load condition, the MP2276 can be configured to work in pulse-skip mode to optimize efficiency. When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the MP2276 transitions from CCM to pulse-skip mode if the MP2276 is configured so. See the FREQ/MODE Selection section on page 15 for details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Figure 4 shows pulse-skip mode operation at light-load condition. When FB drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse-skip mode operation, FB does not reach the superimposed COMP when the inductor current approaches zero. The LS-FET driver turns into tri-state (Hi-Z) when the inductor current reaches zero. Therefore, the output capacitors discharge slowly to PGND through the FB resistors (R1 and R2). At light-load condition, the HS-FET is not turned on as frequently in pulse-skip mode as it is in forced CCM. As a result, the efficiency in pulse-skip mode is improved greatly compared to that in forced CCM operation.

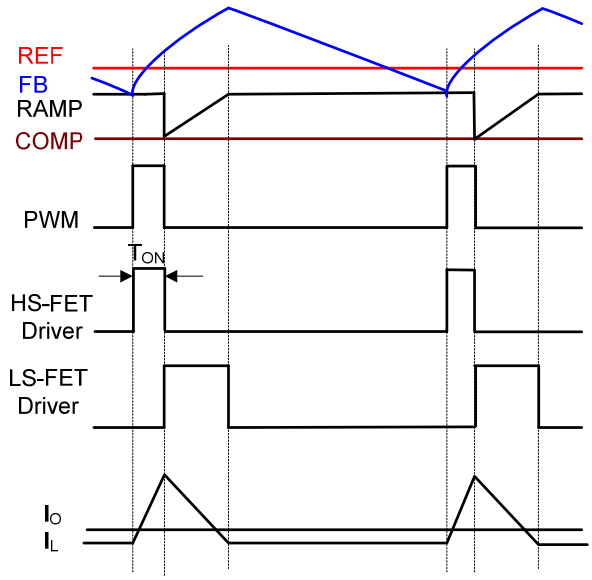


Figure 4: Pulse Skip in Light Load

As the output current increases from the light-load condition, the time period the current modulator regulates in becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

Where F_{SW} is the switching frequency.

The MP2276 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MP2276 can be configured to operate in forced CCM even in light-load condition (see Table 1).

FREQ/MODE Selection

The MP2276 provides both forced CCM operation and pulse-skip operation in light-load condition. The MP2276 has three options for switching frequency selection: 600kHz, 1100kHz, and 2000kHz. Select the operation mode under light-load condition and the switching frequency by choosing the resistance value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1: FREQ/MODE Selection

MODE	Light-Load Mode	Switching Frequency
AGND	Forced CCM	1100kHz
30.1kΩ (±20%) to AGND	Forced CCM	2000kHz
60.4kΩ (±20%) to AGND	Forced CCM	600kHz
121kΩ (±20%) to AGND	Pulse Skip	600kHz
243kΩ (±20%) to AGND	Pulse Skip	2000kHz
VCC	Pulse Skip	1100kHz

Soft Start (SS)

The minimum soft-start time is limited to 1.7ms. This can be increased by choosing the capacitor between SS/TRK and AGND. A minimum value of 3.3nF for this capacitor is always required to stabilize the reference voltage.

The capacitance of this capacitor can be determined with Equation (2) and Equation (3):

$$C_{SS}(nF) = 3.3 - 22 \quad (t_{SS} = 1.7ms) \quad (2)$$

$$C_{SS}(nF) = \frac{t_{ss}(ms) x 10\mu A}{0.8V} \quad (t_{SS} > 1.7ms) \quad (3)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Output Voltage External Reference

SS/TRK can be used as an analog input pin to accept an external reference. When an external voltage signal is connected to SS/TRK, it acts as a reference for the MP2276 output voltage. The FB voltage (V_{FB}) follows this external voltage signal exactly. The soft-start settings are ignored. The SS/TRK input signal can be in the range of 0.3V to 1.4V. During the initial start-up, SS/TRK must first reach 800mV or above to ensure proper operation. Afterward, SS/TRK can be any value between 0.3V and 1.4V. If the external reference is added before start-up, it should be no more than 1.2V to avoid triggering under-voltage protection (UVP).

Pre-Bias Start-Up

The MP2276 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the high-side and low-side switches until the internal soft-start voltage exceeds the sensed output voltage at FB.

Output Voltage Discharge

When the MP2276 is disabled through EN, the output voltage discharge mode is enabled. Both the HS-FET and the LS-FET are latched off. A discharge MOSFET connected between SW and GND is turned on to discharge the output voltage. The typical switch on resistance of this MOSFET is about 80Ω. Once V_{FB} drops below 10% of V_{REF}, the discharge MOSFET is turned off.

Current Sense and Over-Current Protection (OCP)

The MP2276 features an on-die current sense and programmable positive current limit threshold. The current limit is active when the MP2276 is enabled. During the LS-FET on state, the SW current (inductor current) is sensed and mirrored to ILIM with the ratio of G_{CS}. By using a resistor (R_{ILIM}) from ILIM to AGND, the ILIM voltage (V_{ILIM}) is proportional to the SW cycle-by-cycle current. The HS-FET is only allowed to turn on whenever V_{ILIM} is below the internal over-current protection (OCP) voltage threshold (V_{OCP}) during the LS-FET on state to limit the SW ripple valley current cycle-by-cycle.

Calculate the current limit threshold setting from R_{ILIM} with Equation (4):

$$R_{ILIM}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_s})} \quad (4)$$

Where V_{OCP} is 1.2V, G_{CS} is 40μA/A, and I_{LIM} is the desired output current limit (A).

During an over-current condition, the average inductor current is less than the output load current, and the output capacitor must supply the extra current. Eventually, the output voltage drops. Once the output voltage drops to the under-voltage protection (UVP) threshold, the MP2276 enters hiccup mode to restart the part periodically. If the MP2276 detects an over-current condition for 31 consecutive cycles, even if the output voltage is above the UVP level, it enters hiccup mode. The average short-circuit current is reduced greatly to alleviate the thermal issue and protect the regulator. The MP2276 exits hiccup mode once the under-voltage (UV) condition is removed.

Negative Inductor Current Limit

When LS-FET detects a -4A current, the MP2276 turns off the LS-FET for 80ns to limit the negative current.

Under -Voltage Protection (UVP)

The MP2276 monitors the output voltage by connecting FB to the tap of a resistor divider to detect an under-voltage condition. If V_{FB} drops below 80% of V_{REF}, under-voltage protection (UVP) is triggered. The MP2276 enters hiccup protection mode to restart the part periodically. The MP2276 exits UVP when V_{FB} recovers to more than 92.5% of V_{REF}.

Output Sinking Mode (OSM)

The MP2276 uses output sinking mode (OSM) to regulate the output voltage to the targeted value. When V_{FB} is above 105% of V_{REF}, but is below the OVP threshold, OSM is triggered. During OSM operation, the LS-FET remains on until it reaches the -4A negative current limit. After hitting -4A, the LS-FET is turned off momentarily for 80ns and is then turned on again. The MP2276 continues this operation until V_{FB} drops below 102.5% of V_{REF}. Once it does, the MP2276 exits OSM after 15 consecutive cycles of forced CCM.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Over-Voltage Protection (OVP)

The MP2276 monitors the output voltage using FB connected to the tap of a resistor divider to detect an over-voltage condition. If V_{FB} exceeds 116% of V_{REF}, OVP is triggered. The controller enters a dynamic regulation period. During this period, the low-side negative current limit increases to -8A. The LS-FET remains on until it triggers the low-side negative current limit. After hitting the low-side negative current limit, the LS-FET is turned off momentarily for 80ns and is then turned on again. This discharges the output to keep it within the normal range. The MP2276 exits this regulation period when V_{FB} falls below 102.5% of V_{REF}.

Over-Temperature Protection (OTP)

The MP2276 has over-temperature protection (OTP). The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. There is a hysteresis of about 20°C. Once the junction temperature drops to about 130°C, soft start is initiated.

Power Good (PG)

The MP2276 has a power good (PG) output. PG is the open drain of a MOSFET. Connect PG to VCC or another external voltage source less than 3.6V through a pull-up resistor (typically 100kΩ). After applying the input voltage, the MOSFET turns on so that PG is pulled to GND before the internal soft-start voltage is ready. After V_{FB} reaches 92.5% of V_{REF}, PG is pulled high after a 1ms delay.

When V_{FB} drops to 80% of V_{REF} (UV) or exceeds 116% of V_{REF} (OV), PG is pulled low. Once V_{FB} rises back to its nominal voltage window (rises to 92.5% of V_{REF} for UV, drops to 102.5% of V_{REF} for OV), PG goes high again.

If the input supply fails to power the MP2276, PG is pulled low, even though it is tied to an external DC source through a pull-up resistor. The relationship between the PG voltage and the pull-up current is shown in Figure 5.

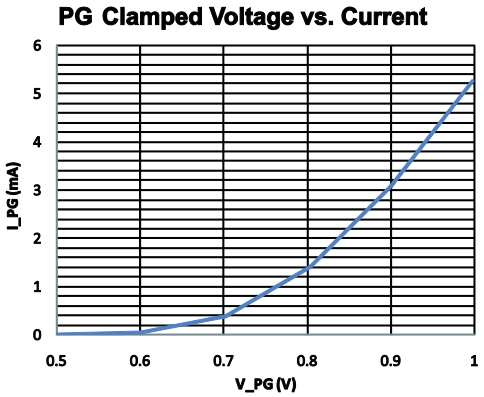


Figure 5: PG Clamped Voltage vs. Pull-Up Current

Enable (EN) Configuration

The MP2276 turns on when EN goes high. The MP2276 turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MP2276.

EN is clamped internally using a 4V series Zener diode (see Figure 6). Connect the EN input through a pull-up resistor to VIN to limit the EN input current to less than 100μA to prevent damage to the Zener diode. For example, if connecting a 300kΩ pull-up resistor to 16VIN, then I_{Zener} = (16V - 4V) / 300kΩ = 40μA.

The MP2276 provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage at which the MP2276 is enabled. This is highly recommended for applications where there is no dedicated EN control logic signal to avoid possible UVLO bouncing during power-up and power-down. The resistor divider values can be determined with Equation (5):

$$V_{IN_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (5)$$

Where VIH_{EN} is 1.21V, typically. R_{UP} and R_{DOWN} should be chosen to limit the EN input current below 100μA.

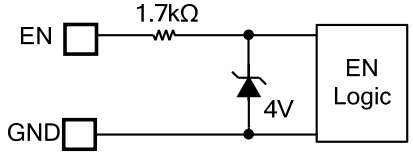


Figure 6: Zener Diode between EN and GND

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

APPLICATION INFORMATION

Output Voltage Setting

Choose a proper value for R1 in the range of 1kΩ to 100kΩ. Then determine R2 with Equation (6):

$$R_2(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_1(k\Omega) \quad (6)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) is needed in parallel with R1. R1 and C_{FF} form an extra zero to the system, which helps improve loop responses. R1 and C_{FF} are chosen so that the zero is located around 20kHz - 60kHz.

Table 2 lists the recommended resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages (6)

V_{OUT}(V)	R1(kΩ)	R2(kΩ)
1	2	8.06
1.2	2	4.02
1.8	10	8.06
2.5	10	4.7
3.3	10	3.16
5	10	1.91

NOTE:

5) For additional component parameters, please refer to the Typical Application Circuits on page 21 to page 22.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (8):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets any input voltage ripple requirement.

Estimate the input voltage ripple with Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (10):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (10)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAPs. Estimate the output voltage ripple with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (11)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

For POSCAPs, the ESR dominates the switching frequency impedance. For simplification, the output ripple can be approximated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. Generally, select an inductor value that allows the inductor peak-to-peak ripple current to be 30% to 40% of the maximum switch current limit. Also design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value with Equation (14):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (15):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 7 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP2276.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. Place as many PGND vias as possible as close to the MP2276 as possible to minimize both parasitic impedance and thermal resistance.
5. Place a VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place a BST capacitor as close to BST and SW as possible.
8. Use a trace width of 20 mils or higher to route the path.
9. Use a 1μF bootstrap capacitor.

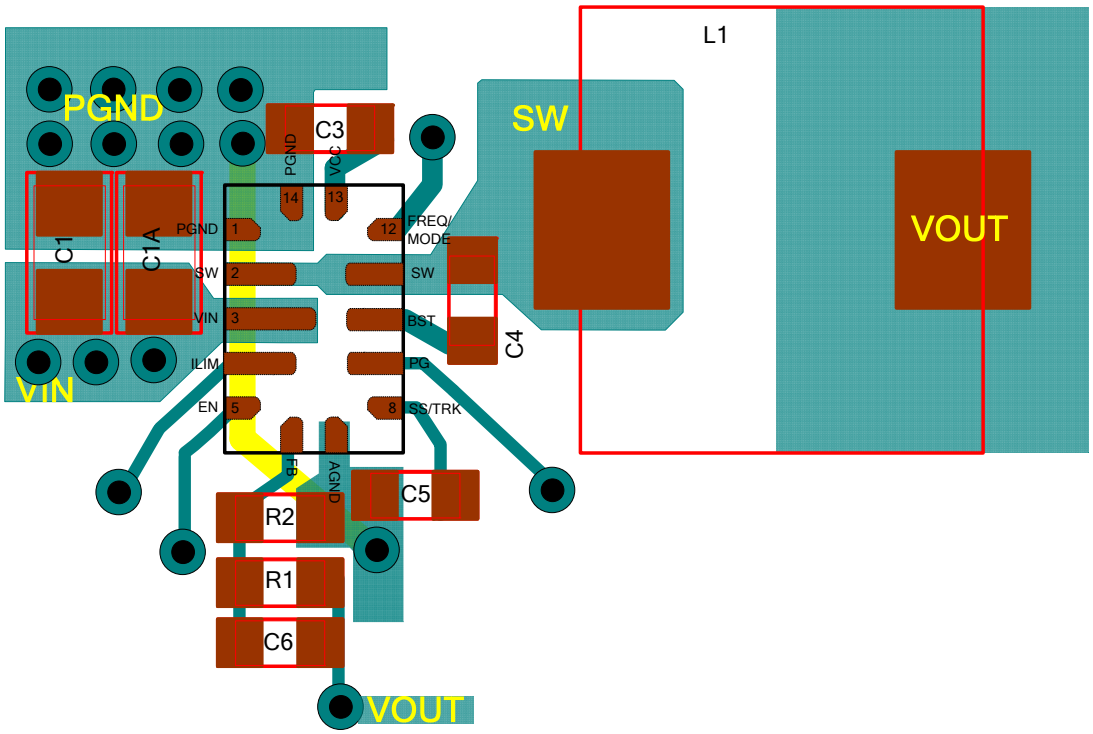


Figure 7: Recommended Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Design Example

Table 3 shows a design example following the application guidelines for the specifications below.

Table 3: Design Example

V_{IN}	3.3V, 12V
V_{OUT}	1V
I_O	8A

The detailed application schematics are shown in Figure 8 through Figure 17. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

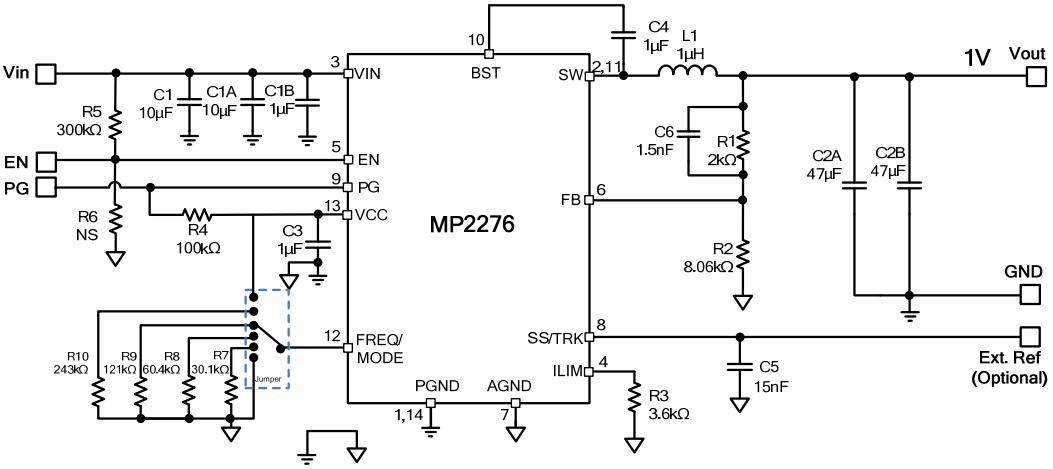


Figure 8: VIN = 4V - 16V, V_{OUT} = 1V, I_{OUT} = 8A, F_{SW} = 600kHz

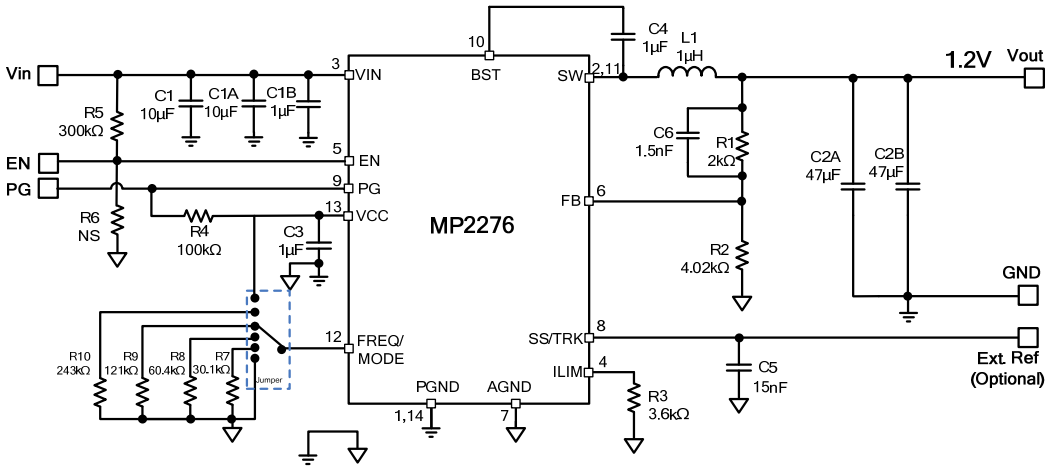


Figure 9: VIN = 4V - 16V, V_{OUT} = 1.2V, I_{OUT} = 8A, F_{SW} = 600kHz

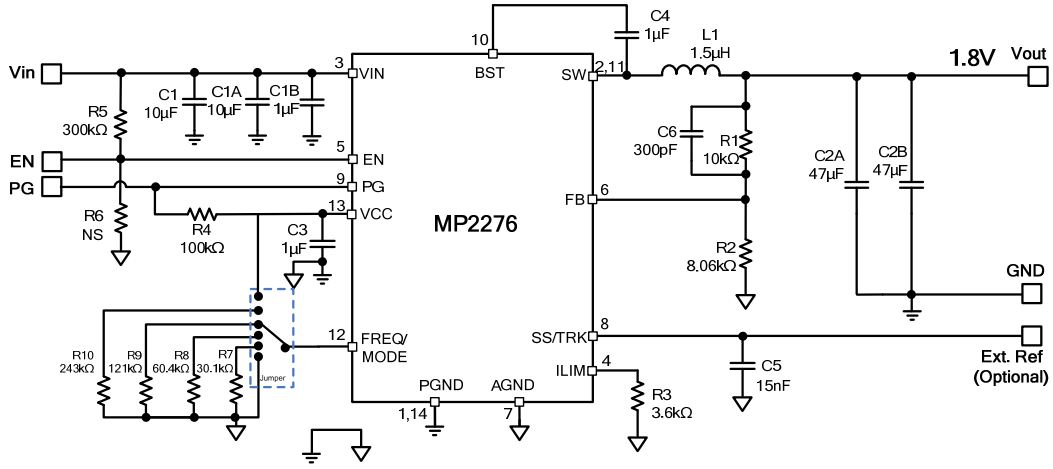


Figure 10: VIN = 4V - 16V, V_{OUT} = 1.8V, I_{OUT} = 8A, F_{SW} = 600kHz

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

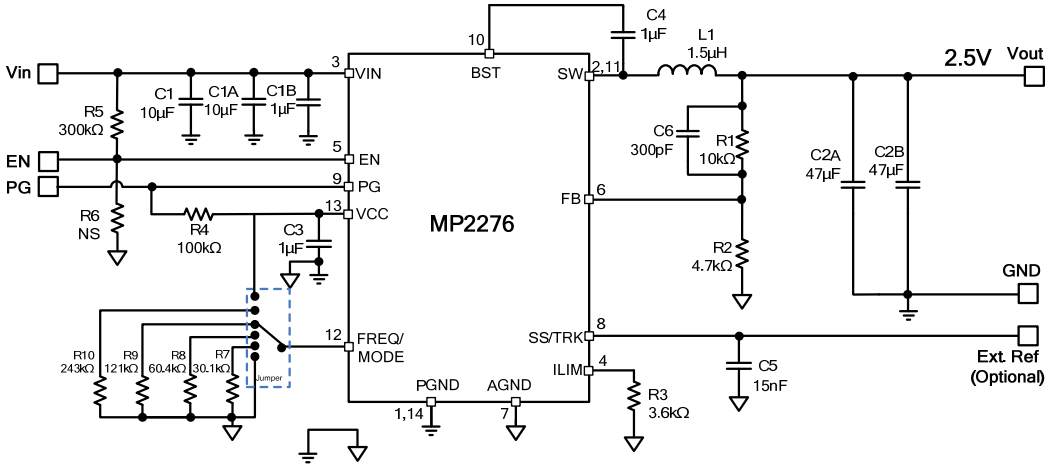


Figure 11: VIN = 4V - 16V, V_{OUT} = 2.5V, I_{OUT} = 8A, F_{SW} = 600kHz

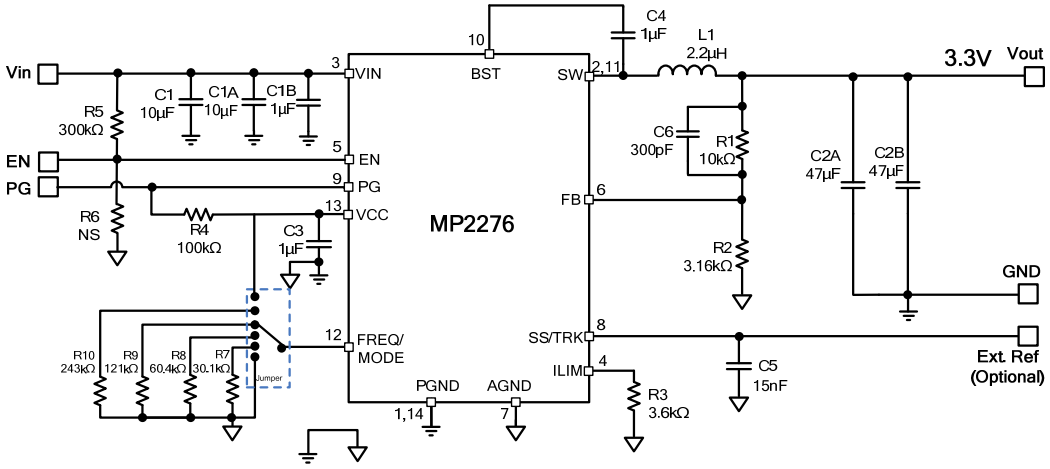


Figure 12: VIN = 4.5V - 16V, V_{OUT} = 3.3V, I_{OUT} = 8A, F_{SW} = 600kHz

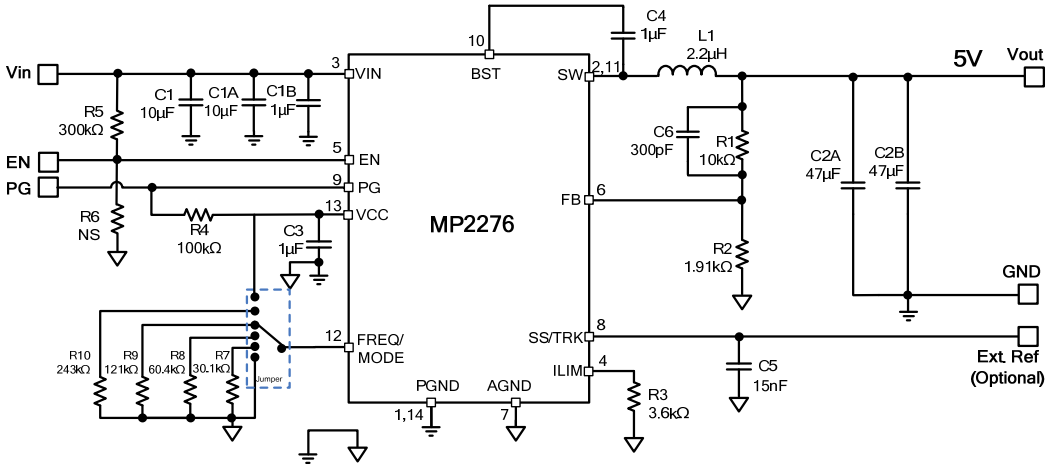


Figure 13: VIN = 6V - 16V, V_{OUT} = 5V, I_{OUT} = 8A, F_{SW} = 600kHz

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

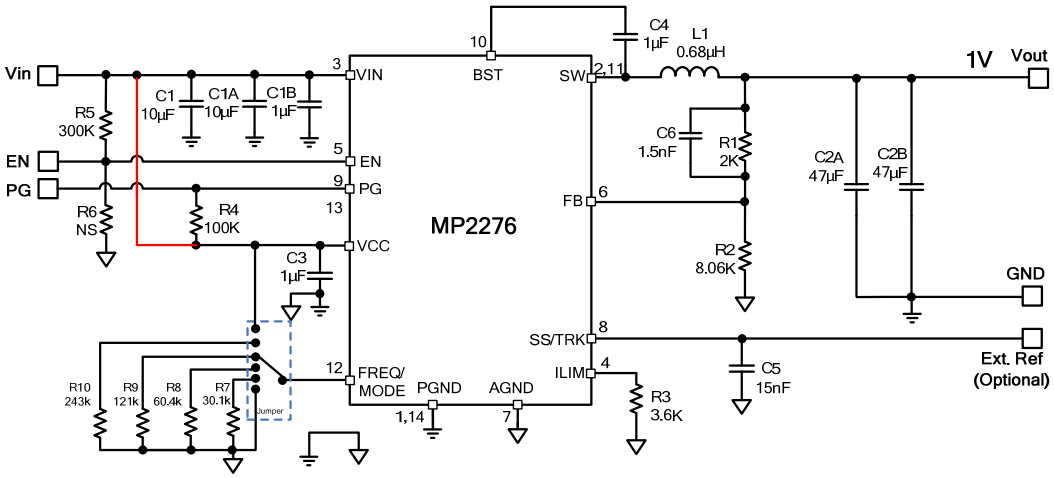


Figure 14: VIN = 3.3V, V_{OUT} = 1V, I_{OUT} = 8A, F_{SW} = 600kHz

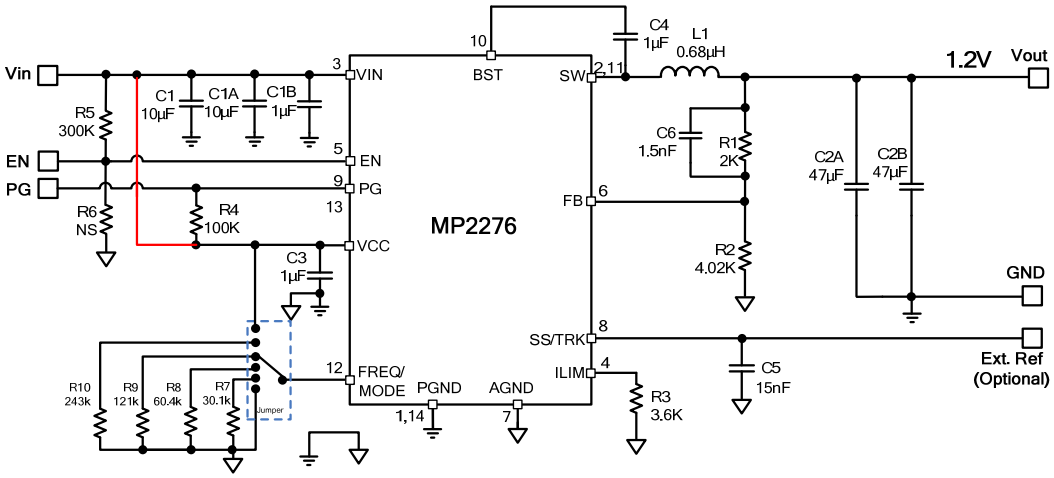


Figure 15: VIN = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 8A, F_{SW} = 600kHz

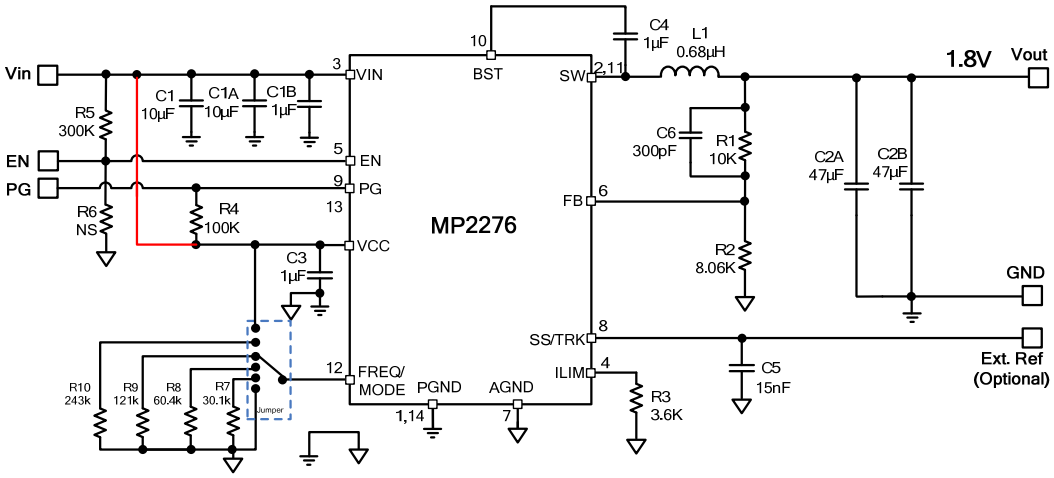


Figure 16: VIN = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 8A, F_{SW} = 600kHz

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

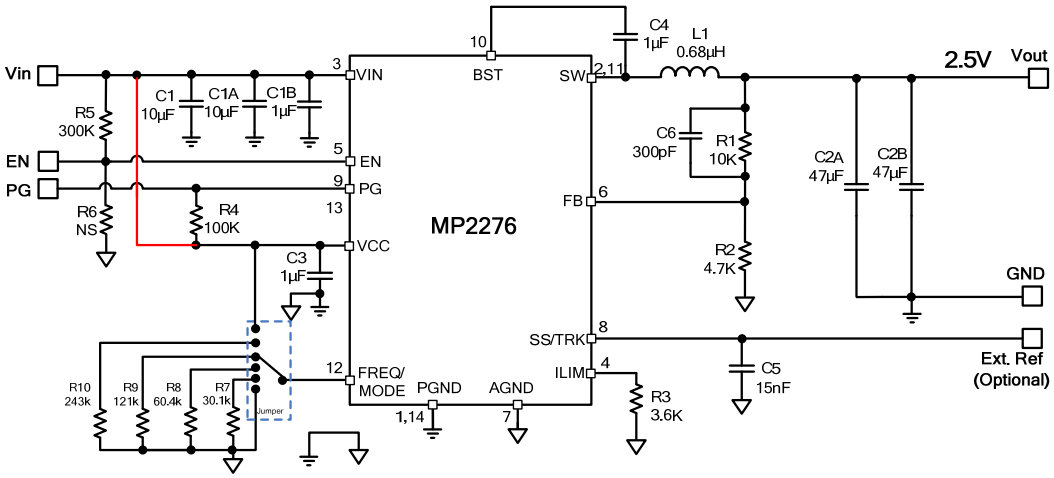
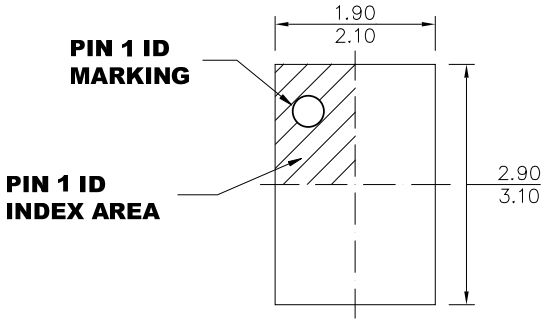


Figure 17: VIN = 3.3V, V_{OUT} = 2.5V, I_{OUT} = 8A, F_{SW} = 600kHz

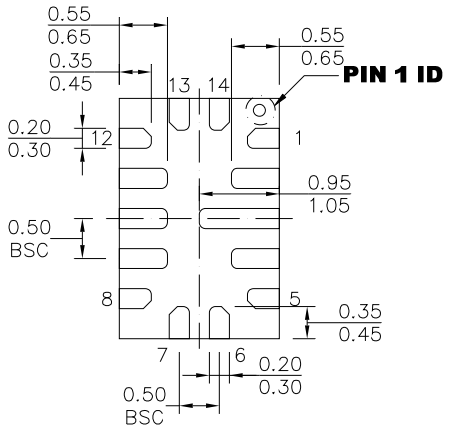
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PACKAGE INFORMATION

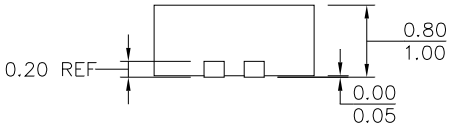
QFN-14 (2mmx3mm)



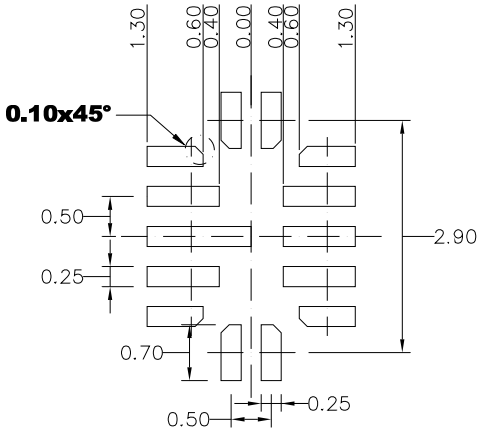
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,5,8 AND PIN12 HAVE THE SAME SHAPE.
2) LAND PATTERNS OF PIN2,4,9,10 AND PIN11 HAVE THE SAME SHAPE.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.