MP2321

19V, 2A, 40µA I_Q, High-Efficiency, Constant-On-Time, Step-Down Converter in a QFN (2mmx3mm) Package

The Future of Analog IC Technology

DESCRIPTION

The MP2321 is a fully-integrated, high-efficiency, synchronous, step-down, switch-mode converter with 40µA of quiescent current. The MP2321 achieves 2A of continuous output current over a wide input supply range with excellent load and line regulation and can operate with high efficiency over a wide output current load range. The MP2321 is optimized for battery-operated applications and applications requiring high light-load efficiency.

With constant-on-time (COT) control, the MP2321 provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP2321 requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-14 (2mmx3mm) package.

FEATURES

- 4V to 19V Operating Input Range
- 2A Output Current
- 40µA Quiescent Current
- Output Adjustable from 0.6V
- 110mΩ/40mΩ High-Side/Low-Side $R_{DS(ON)}$ for Internal Power MOSFETs
- Power Good Indicator
- Programmable Soft-Start Time
- Forced PWM or Auto PFM/PWM Mode Selectable
- Programmable Switching Frequency
- Thermal Shutdown
- Short-Circuit Protection: Hiccup Mode
- Available in a QFN-14 (2mmx3mm) Package

APPLICATIONS

- Tablet PCs
- Solid State Drives
- Gaming
- Battery-Operated Applications

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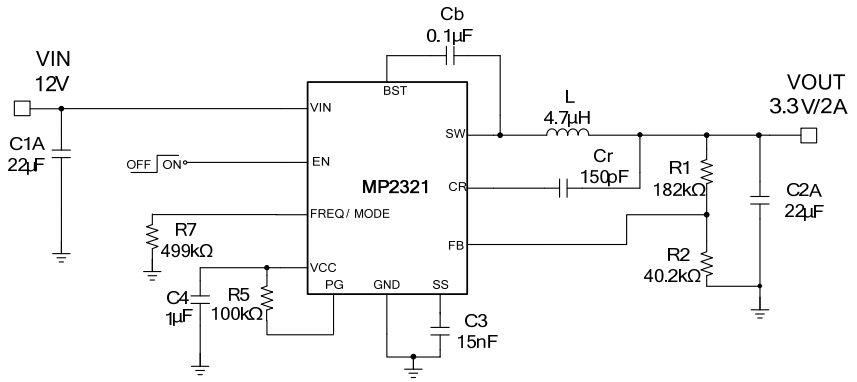
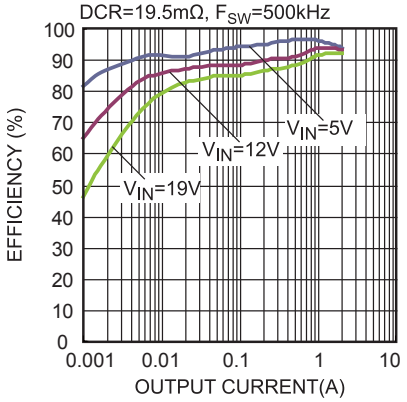
TYPICAL APPLICATION



Efficiency vs. Output Current

Auto PFM/PWM, V_{OUT}=3.3V, L=4.7µH, DCR=19.5mΩ, F_{SW}=500kHz



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2321GD	QFN-14 (2mmx3mm)	*See Below*

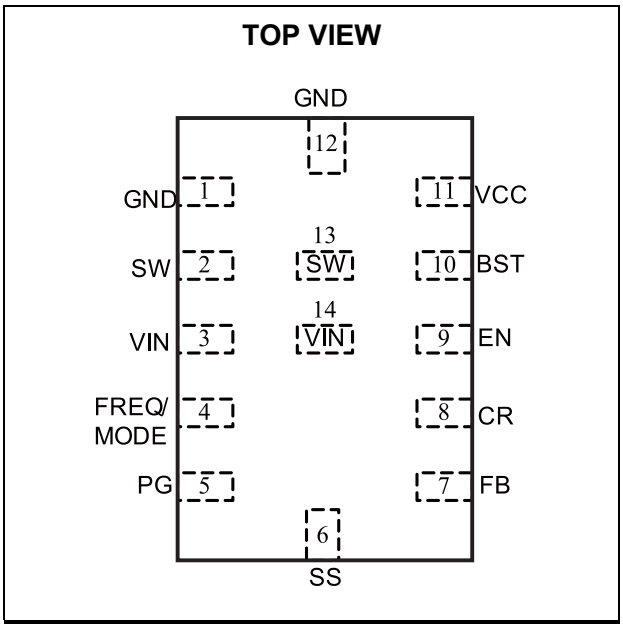
* For Tape & Reel, add suffix –Z (e.g. MP2321GD–Z)

TOP MARKING

AQDY
LLL

AQD: Product code of MP2321GD
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

VIN ..... +21V
V_{SW} ..... -0.3V (-5V < 10ns) to VIN + 0.3V (23V < 10ns)
V_{BST} ..... V_{SW} + 6V
All other pins ..... -0.3V to +6V (2)
Continuous power dissipation (3)
QFN-14 (2mmx3mm) 1.8W
Junction temperature ..... +150°C
Lead temperature ..... +260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply voltage (VIN) ..... 4V to 19V
Output voltage (V_{OUT}) ..... 0.6V to VIN * D_{MAX} (5)
Operating junction temp. (T_J) ....-40°C to +125°C

Thermal Resistance (6)

	θ_{JA}	θ_{JC}	
QFN-14 (2mmx3mm)	70	15 ...	°C/W

NOTES:

1) Exceeding these ratings may damage the device
2) For details on EN's ABS max rating, please refer to the Enable Control section on page 15.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) For details on D_{MAX}, see the High Duty Cycle Condition section on page 13.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C (7), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		0.1	1	µA
Supply current (quiescent)	I_Q	V_{EN} = 5V, V_{FB} = 0.7V, T_J = 25°C		40	55	µA
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		3.5	3.7	3.9	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			200		mV
HS switch on resistance	$HS_{RDS(ON)}$			110		mΩ
LS switch on resistance	$LS_{RDS(ON)}$			40		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	1	µA
High-side MOSFET current limit	I_{LIMIT}	Duty = 40%, T_J = -40°C to +125°C	2.7	4	6	A
		Duty = 40%, T_J = 25°C	3	4	6	
Low-Side MOSFET current limit	I_{LIMIT}	PWM mode, sink current		1.5		A
One-shot on timer (8)	T_{ON}	R_{REQ} = 180k from FREQ/MODE to GND		230		ns
Minimum on time (8)	T_{ON_min}			90		ns
Minimum off time	T_{OFF_min}			150		ns
Feedback voltage	V_{FB}	T_J = -40°C to +125°C	591	600	609	mV
		T_J = 25°C	594	600	606	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS}		4	8	11	µA
EN input high voltage			1.6			V
EN input low voltage					0.4	V
EN input current	I_{EN}	V_{EN} = 2V		2		µA
		V_{EN} = 0V		0		
Power good UV rising threshold	$PGUV_{Vth_Hi}$			0.9		V_{FB}
Power good UV falling threshold	$PGUV_{Vth_Lo}$			0.85		V_{FB}
Power good OV rising threshold	$PGOV_{Vth_Hi}$		1.2	1.3	1.4	V_{FB}
Power good OV falling threshold	$PGOV_{Vth_Lo}$		1	1.1	1.2	V_{FB}
Power good delay	PG_{Td}			140		µs
Power good sink current capability	V_{PG}	Sink 1mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			50	nA
Thermal shutdown (8)	T_{SD}			150		°C
Thermal shutdown hysteresis (8)	T_{SD_HYS}			20		°C

NOTES:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Not tested in production. Guaranteed by design and engineering sample characterization test.

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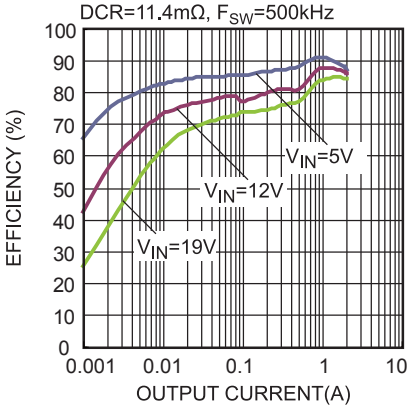
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12V, V_{OUT} = 1.2V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

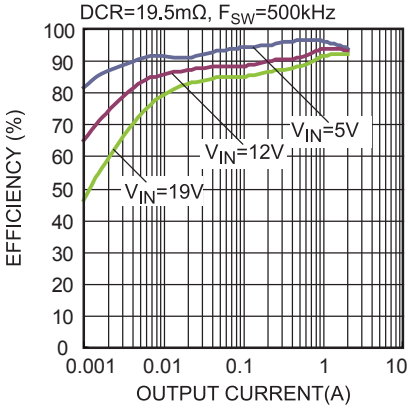
Efficiency vs. Output Current

Auto PFM/PWM, V_{OUT}=1.2V, L=2.2µH, DCR=11.4mΩ, F_{SW}=500kHz



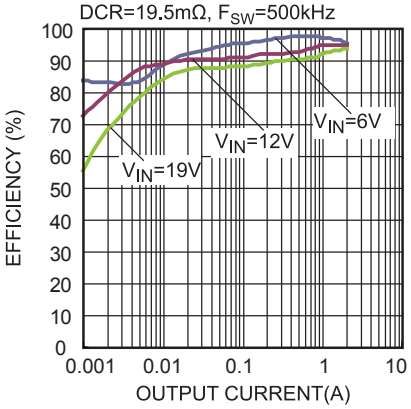
Efficiency vs. Output Current

Auto PFM/PWM, V_{OUT}=3.3V, L=4.7µH, DCR=19.5mΩ, F_{SW}=500kHz



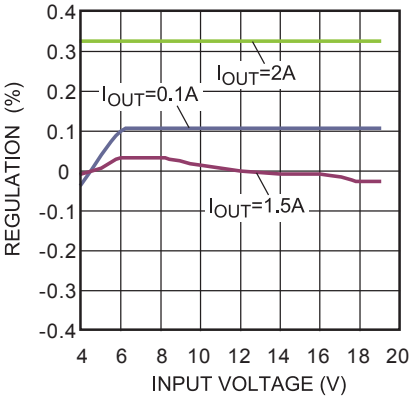
Efficiency vs. Output Current

Auto PFM/PWM, V_{OUT}=5V, L=4.7µH, DCR=19.5mΩ, F_{SW}=500kHz



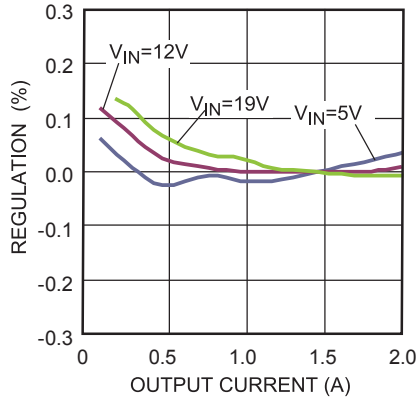
Line Regulation

V_{IN}=4V to 19V



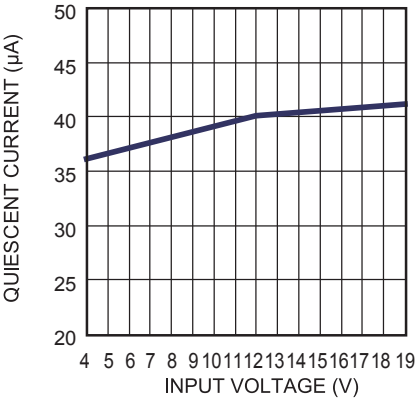
Load Regulation

V_{IN}=5V to 19V



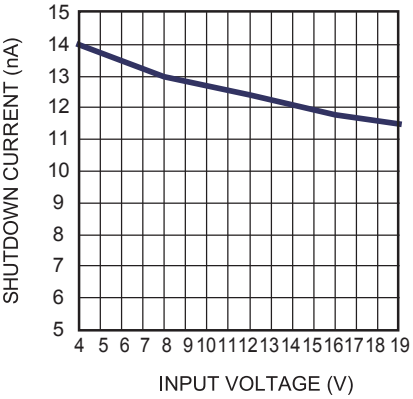
Quiescent Current vs. Input Voltage

V_{IN}=4 to 19V,V_{FB}=0.7V

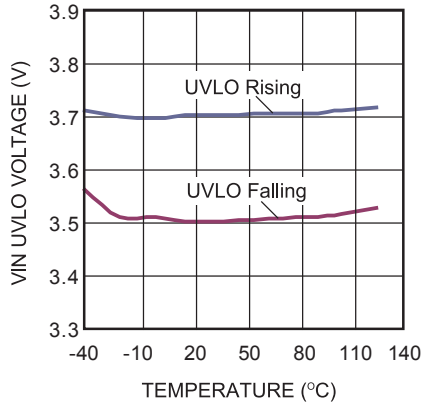


Shutdown Current vs. Supply voltage

V_{IN}=4 to19V,V_{EN}=0V

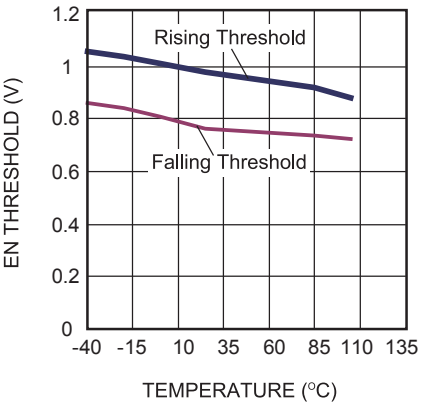


VIN UVLO vs. Temperature



EN Rising Threshold vs. Temperature

V_{IN}=12V



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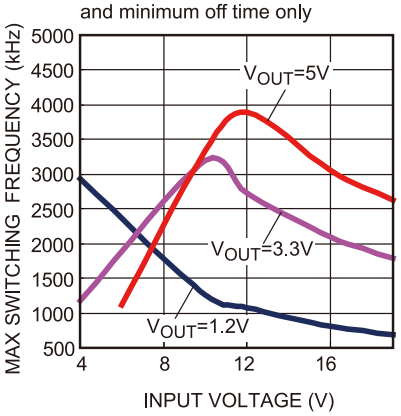
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1.2V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

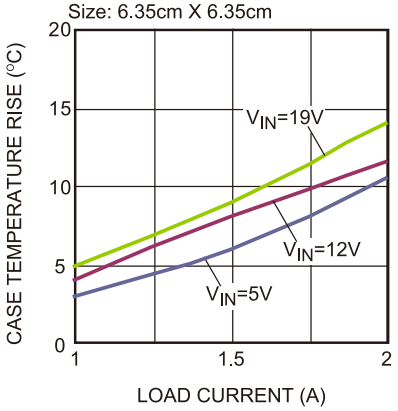
Max Frequency vs. Input Voltage

Consider the minimum on time and minimum off time only



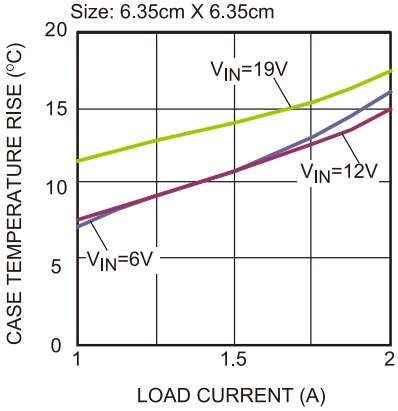
Case Temperature Rise vs. I_{OUT}

V_{OUT}=1.2V, I_{OUT}=1A to 2A, 4 Layers PCB, Size: 6.35cm X 6.35cm



Case Temperature Rise vs. I_{OUT}

V_{OUT}=5V, I_{OUT}=1A to 2A, 4 Layers PCB, Size: 6.35cm X 6.35cm



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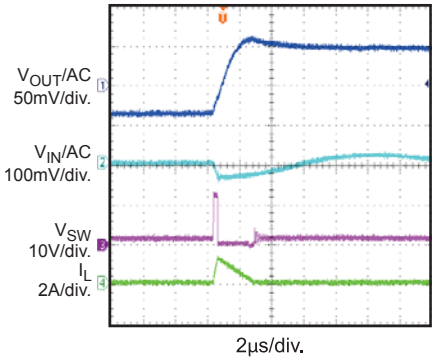
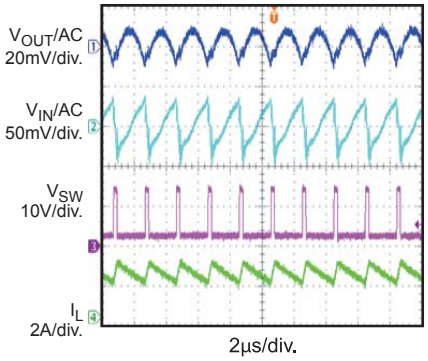
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1.2V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

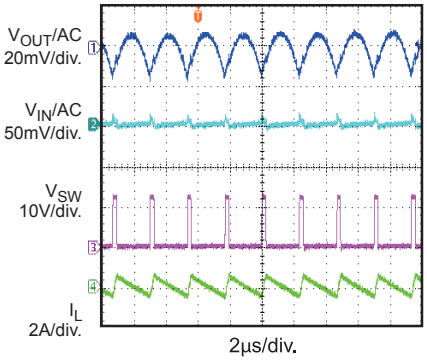
Input/Output Ripple
Auto PFM/PWM, I_{OUT}=0A



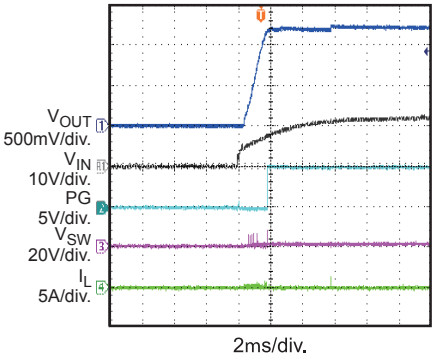
Input/Output Ripple
I_{OUT} = 2A



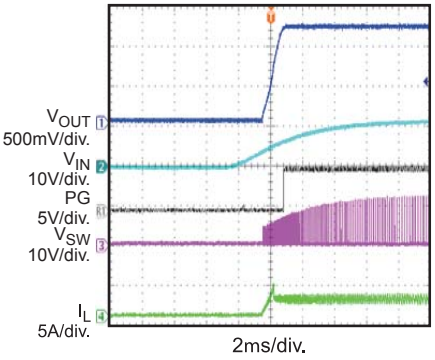
Input/Output Ripple
Forced PWM, I_{OUT}=0A



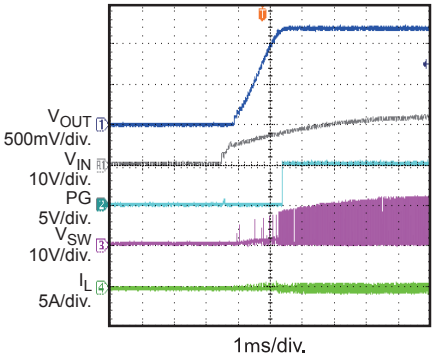
Start-Up through VIN
Auto PFM/PWM, I_{OUT}=0A



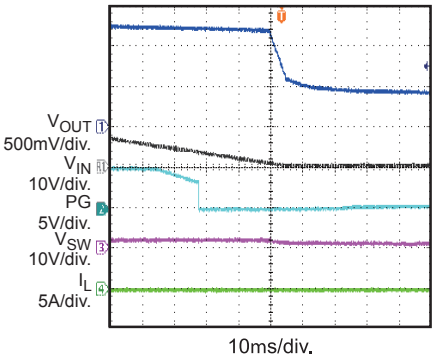
Start-Up through VIN
I_{OUT} = 2A



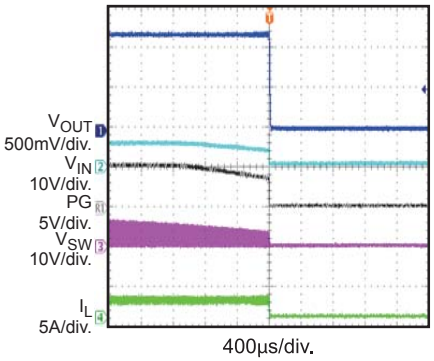
Start-Up through VIN
Forced PWM, I_{OUT}=0A



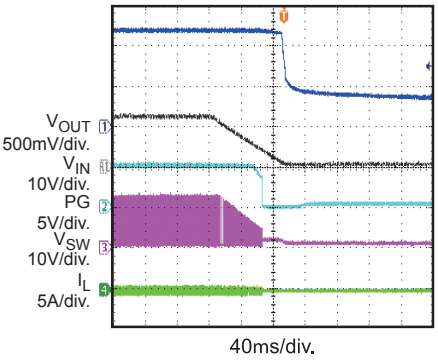
Shutdown through VIN
Auto PFM/PWM, I_{OUT}=0A



Shutdown through VIN
I_{OUT} = 2A



Shutdown through VIN
Forced PWM, I_{OUT}=0A



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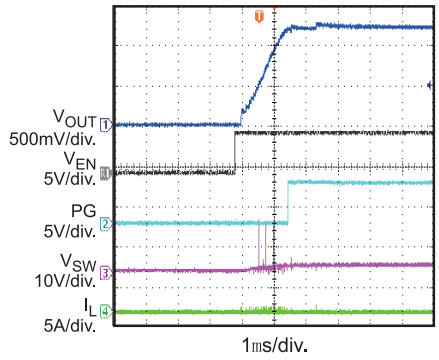
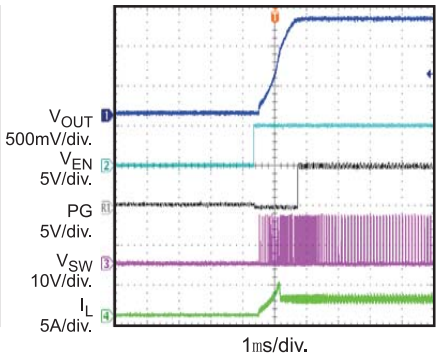
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1.2V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

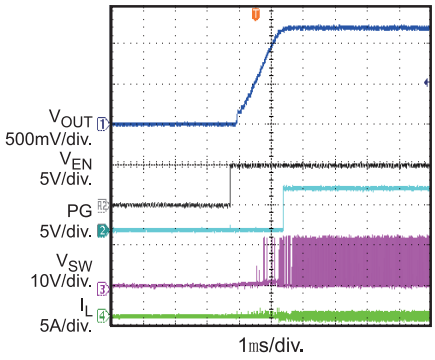
Start-Up through EN
Auto PFM/PWM, I_{OUT}=0A



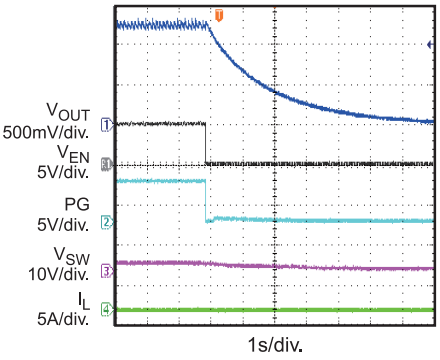
Start-Up through EN
I_{OUT} = 2A



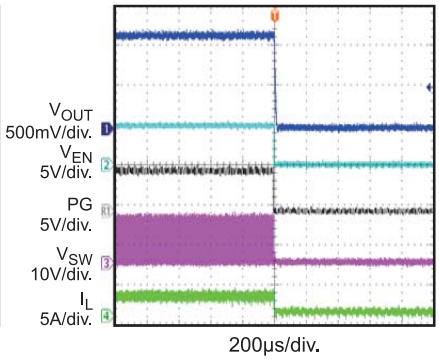
Start-Up through EN
Forced PWM, I_{OUT}=0A



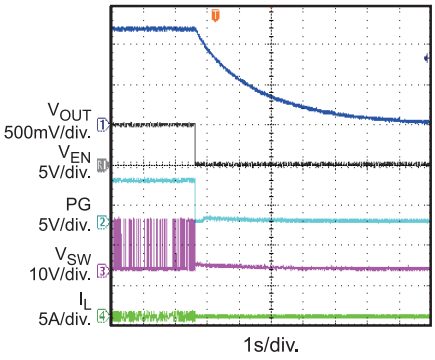
Shutdown through EN
Auto PFM/PWM, I_{OUT}=0A



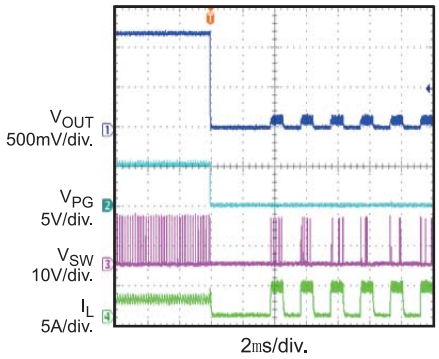
Shutdown through EN
I_{OUT} = 2A



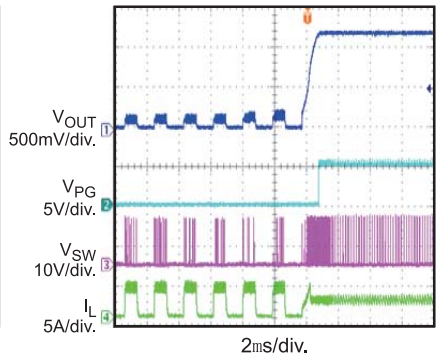
Shutdown through EN
Forced PWM, I_{OUT}=0A



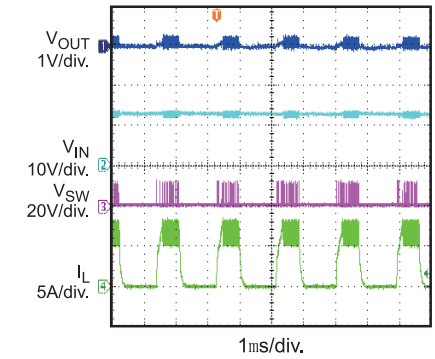
Short-Circuit Entry
I_{OUT}=2A



Short-Circuit Recovery
I_{OUT} = 2A



Short-Circuit Steady



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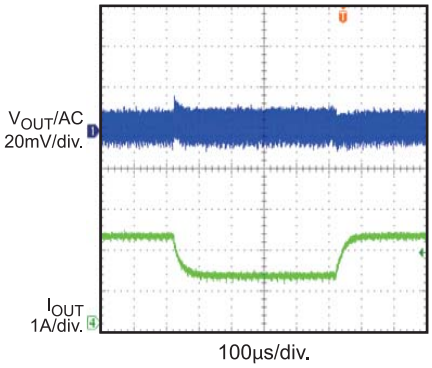
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1.2V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

Load Transient

I_{OUT}=1A to 2A, 250mA/µs



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PIN FUNCTIONS

Package Pin #	Name	Description
1, 12	GND	**System ground.** GND is the reference ground for the regulated output voltage. GND requires special consideration during PCB layout.
2, 13	SW	**Switch output.** Connect SW using wide PCB traces.
3, 14	VIN	**Supply voltage.** The MP2321 operates from a 4V to 19V input rail. A capacitor (C1) is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
4	FREQ/MODE	**Frequency set during CCM operation.** Connect a resistor to VIN to set the switching frequency and operate the MP2321 in forced PWM mode. Connect a resistor to GND to set the switching frequency and operate the MP2321 in auto PFM/PWM mode. Do not float FREQ/MODE.
5	PG	**Power good output.** The output of PG is an open drain that goes high if the FB voltage is within 90% to 110% of V_{REF}. There is a 140μs delay when PG goes high. Note: If PG is pulled up to an external voltage, PG will not de-assert (Logic low) if EN is low or if input power is off. It is recommended that PG is pulled up to VCC pin and in this case PG will de-assert (Logic low) when EN is Low or if input power is off. Refer to Applications section for additional details.
6	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time to avoid start-up inrush current.
7	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider connected between the output and GND.
8	CR	**Internal ramp adjust.** Connect a capacitor from V_{OUT} to CR to adjust the internal ramp amplitude. This can be used to improve transient performance.
9	EN	**Enable.** Set EN = 1 to enable the MP2321. For automatic start-up, connect EN to VIN with a pull-up resistor.
10	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
11	VCC	**Internal bias supply.** VCC is an internal 5V LDO output. Decouple VCC with a 1μF ceramic capacitor placed as close to VCC as possible.

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BLOCK DIAGRAM

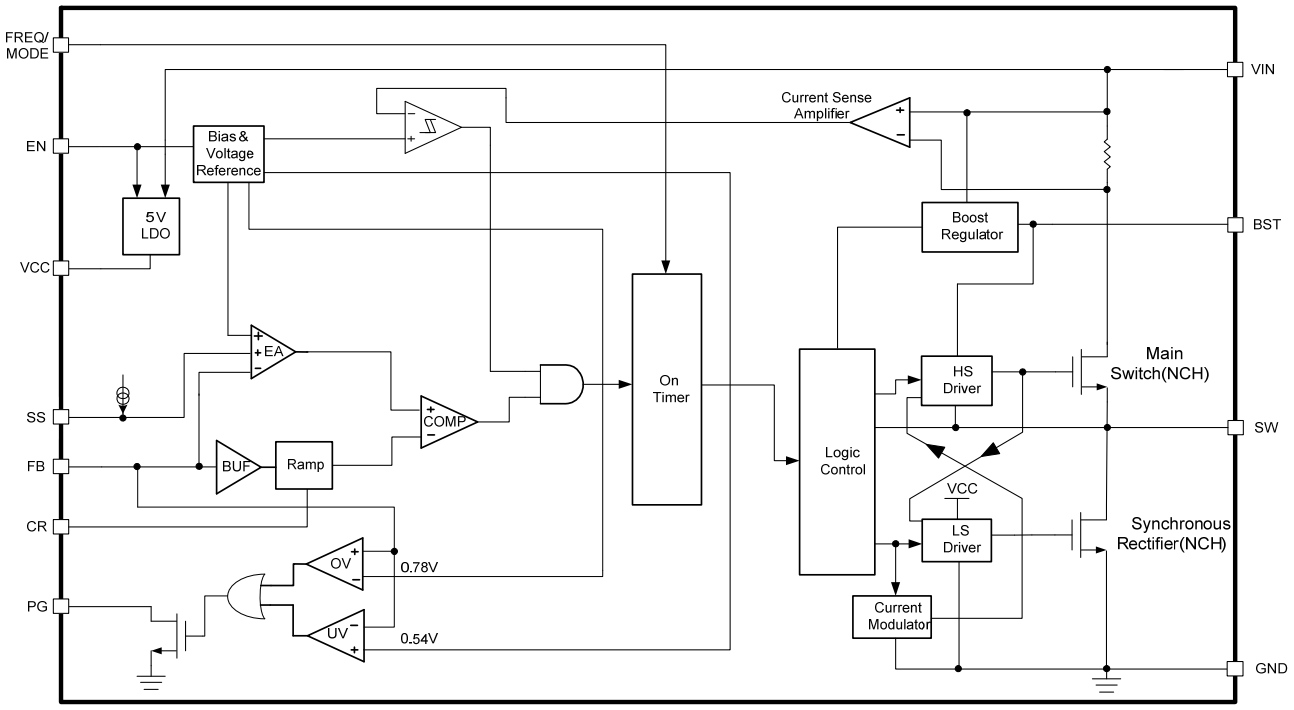

Figure 1: Functional Block Diagram

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OPERATION

PWM Operation

The MP2321 is a fully-integrated, synchronous, rectified, step-down, switch-mode converter. The MP2321 uses constant-on-time (COT) control to provide fast transient response and easy loop compensation. Figure 2 shows the simplified ramp compensation block.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{Ramp}) is lower than the error amplifier output voltage (V_{EAO}), which indicates insufficient output voltage. The input voltage and the frequency-set resistor determine the high-side MOSFET turn-on time (T_{ON}). After the on period elapses, the HS-FET enters the off state. By cycling HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. Shoot-through occurs when the HS-FET and LS-FET are both turned on at the same time, causing a dead short between the input and GND. Shoot-through reduces efficiency dramatically. The MP2321 prevents shoot-through by generating a dead-time (DT) internally between HS-FET off and LS-FET on, and LS-FET off and HS-FET on. The MP2321 enters either heavy-load operation or light-load operation depending on the output current.

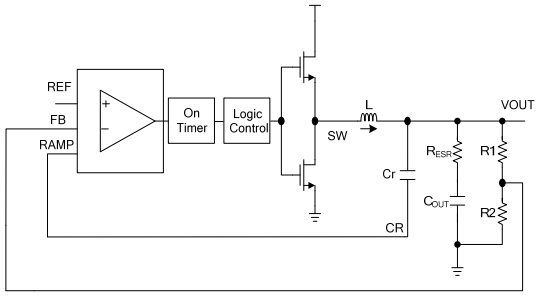

Figure 2: Simplified Ramp Compensation Block

MODE Selection

Connect a resistor (R6) from FREQ/MODE to VIN to set the switching frequency and operate the MP2321 in forced pulse-width modulation (PWM) mode (see Figure 3). Connect a resistor (R7) from FREQ/MODE to GND to set the switching frequency and operate the MP2321 in auto PWM or pulse-frequency modulation (PFM) mode.

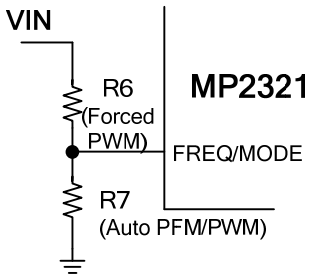

Figure 3: Mode Selection

Switching Frequency

The MP2321 uses constant-on-time (COT) control. There is no dedicated oscillator in the IC. The input voltage is forward fed into the on-time one-shot timer through the frequency resistor. The duty ratio is kept as V_{OUT}/VIN, and the switching frequency is fairly constant over the input voltage range. The approximate typical switching frequency can be determined with Equation (1):

$$F_{SW}(KHz) = \frac{10^6}{T_{on}(ns) \times \frac{V_{IN}(V)}{V_{OUT}(V)}} \quad (1)$$

T_{ON} is slightly different in forced PWM mode and auto PFM/PWM mode. Approximate the typical T_{ON} value in forced PWM mode with Equation (2):

$$T_{ON_PWM} = \frac{14.5 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} + T_{DELAY_PWM}(ns) \quad (2)$$

Approximate the typical T_{ON} value in auto PFM/PWM mode with Equation (3):

$$T_{ON_PFM} = \frac{13 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} + T_{DELAY_PFM}(ns) \quad (3)$$

Where T_{DELAY_PWM} and T_{DELAY_PFM} are the comparator delay. The typical values are approximately 15ns and 10ns, respectively.

When the MP2321 enters continuous conduction mode (CCM), the duty ratio changes slightly from light load to full load due to the power loss. The frequency changes slightly from light load to full load, even in CCM. Because of the minimum on time and minimum off time, the switching frequency is limited.

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The maximum frequency can be calculated by Equation (4) and Equation (5). Choose the lower value of the two as the maximum frequency:

$$F_{SW\text{-}max}(KHz) = \frac{10^6}{T_{on\text{-}min}(ns) \times \frac{V_{IN}(V)}{V_{OUT}(V)}} \quad (4)$$

$$F_{SW\text{-}max}(KHz) = \frac{(V_{IN}(V)-V_{OUT}(V)) \times 10^6}{T_{off\text{-}min}(ns) \times V_{IN}(V)} \quad (5)$$

Where the Ton-min typical value is 90ns, and the Toff-min typical value is 150ns. For example, if VIN = 12V, and V_{OUT} = 1.2V, then the maximum frequency is about 1.1MHz. The MP2321 is optimized to operate at a high switching frequency with high efficiency. High switching frequency allows small LC filter components to be used to save system PCB space.

Forced PWM Operation

When the MP2321 works in forced PWM mode, the MP2321 enters CCM, where the HS-FET and LS-FET repeat the on/off operation, even if the inductor current goes to zero or a negative value. The switching frequency (F_{SW}) is fairly constant. Figure 4 shows the timing diagram during this operation.

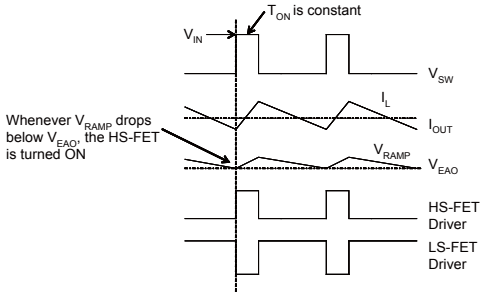

Figure 4: Forced PWM Operation

Light-Load Operation

When the MP2321 works in auto PFM/PWM mode and during light-load operation, the MP2321 automatically reduces the switching frequency to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high-Z). Therefore, the output capacitors discharge slowly to GND through LS-FET, R1, and R2. This operation greatly improves device efficiency when the output current is low (see Figure 5).

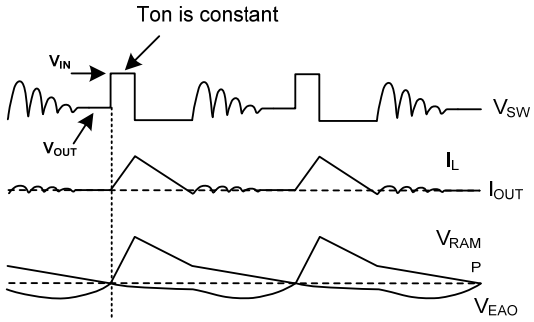

Figure 5: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does in heavy-load condition. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with Equation (6):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (6)$$

The device resumes PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

High Duty Cycle Condition

The MP2316 extends the on time when the output voltage loses regulation when the input voltage is close to the output voltage. The switching frequency drops correspondingly to achieve a larger duty cycle to keep the output regulated.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, Cb, L1, and C2A (see Figure 6). If VIN - V_{SW} exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across Cb.

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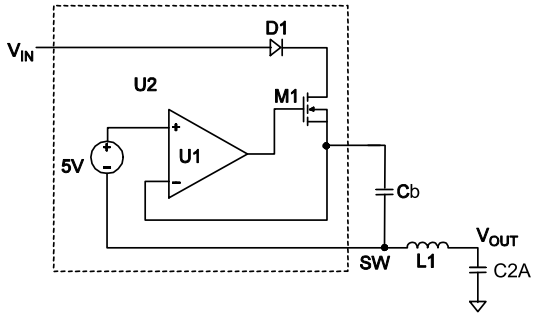

Figure 6: Bootstrap Charging Circuit

Ramp with Small ESR Output Capacitor

When the output capacitors are ceramic, the ESR ripple is not high enough to stabilize the system, so external ramp compensation is needed.

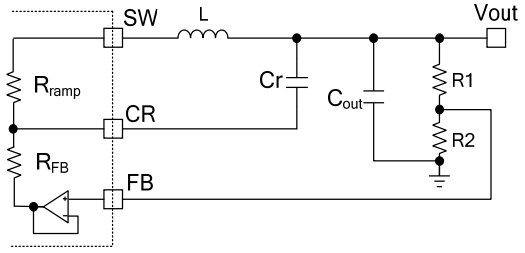

Figure 7: Simplified External Ramp Circuit in PWM Mode with Small ESR Capacitor

Figure 7 shows simplified external ramp compensation for PWM mode. Chose the external ramp (Cr) to meet the condition in Equation (7):

$$\frac{1}{2\pi \times F_{sw} \times C_r} < \frac{1}{5} R_{FB} \quad (7)$$

Where R_{FB} is set to 90kΩ internally. Then calculate I_{Ramp} with Equation (8):

$$I_{Rramp} = I_{Cr} + I_{RFB} \approx I_{Cr} \quad (8)$$

V_{ramp} on the V_{CR} can be estimated with Equation (9):

$$V_{ramp} = \frac{V_{in} - V_{out}}{R_{ramp} \times C_r} \times T_{on} \quad (9)$$

Where R_{Ramp} is set to 900kΩ internally.

As shown in Equation (9), if there is instability in PWM mode, Cr can be reduced. If Cr cannot be reduced further due to limitation from Equation (7), then add an external resistor between SW and CR to reduce the equivalent R_{Ramp}. Set V_{Ramp} to about 20mV - 40mV for stable PWM operation.

Table 1 below lists recommended Cr values for different output voltages. The recommended Cr value in Table 1 is based on a 500kHz switching frequency, selected output inductor, and 22μF output capacitors.

Table 1: Cr Selection for Common Output Voltages

V_{OUT} (V)	L (μH)	Cr (pF)	
		VIN = 12V	VIN = 5V
1.0	2.2	82	82
1.2	2.2	100	100
1.5	3.3	120	82
1.8	3.3	120	56
2.5	3.3	150	56
3.3	4.7	150	56
5	4.7	100	56 (9)

NOTE:

9) When VOUT = 5V, VIN should be higher than 6V.

The Cr value may vary with a different input voltage, output voltage, output inductor, output capacitor, and frequency set. If the design spec is not the same as shown in Table 1, the Cr value must be adjusted accordingly. Refer to Equation (9) as a design guide.

In skip mode, the stability is determined mainly by the V_{EAO} ripple. A V_{Ramp} value chosen in PWM operation is reasonable for skip mode.

Soft Start (SS)

The MP2321 employs a soft start (SS) mechanism to ensure smooth output ramping during power up. When EN goes high, an internal current source (8μA) charges up the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage rises above V_{REF}, it continues to ramp up until the REF voltage takes over. At this point, the soft start finishes, and the MP2321 enters steady state operation. The SS capacitor value can be determined with Equation (10):

$$C_{ss}(nF) = \frac{T_{ss}(ms) \times I_{ss}(uA)}{V_{REF}(V)} \quad (10)$$

If the output capacitance is large, do not set the SS time to be too short. Otherwise, the current limit can be easily reached during SS. A minimum value of 4.7nF is recommended if the output capacitance is larger than 330μF.

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Pre-Bias Start-Up

The MP2321 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start capacitor voltage exceeds the sensed output voltage at FB, the MP2321 begins working.

Power Good (PG)

PG is an open drain output. PG requires a pull-up resistor (e.g.: 100kΩ). PG is pulled to GND before SS is ready. After the FB voltage reaches 90% of V_{REF}, PG is pulled high after a 140μs delay. When the FB voltage drops below 85% of V_{REF}, PG is pulled low.

Note: If PG is pulled up to an external voltage, PG will not de-assert (Logic low) if EN is low or if Vin < 0.8V (typ). If PG is pulled up to the VCC pin, PG will de-assert (Logic low) if either EN is Low or if Vin < 0.8V (typ). If connecting two or more PG together, please refer to Application section.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP2321 has a cycle-by-cycle over-current limit control. During HS-FET on, the inductor current is monitored. When the sensed inductor current reaches the peak current limit, the HS limit comparator is triggered. The MP2321 enters over-current protection (OCP) mode immediately, turns the HS-FET off, and turns the LS-FET on. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold, typically 50% below the reference. Once UV is triggered, the MP2321 enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the over-current condition still remains after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to the regulation level. OCP is a non-latch protection.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 6.5V series Zener diode. Connect the EN input through a pull-up resistor to the voltage on VIN. The pull-up resistance must be large enough to limit the EN current below 100μA. For example, with 12V connected to VIN, $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage below 6V to prevent damage to the Zener diode.

Under-Voltage Lockout (UVLO) Protection

The MP2321 has under-voltage lockout protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP2321 powers up. The MP2321 shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is a non-latch protection.

Thermal Shutdown

The MP2321 employs thermal shutdown by monitoring the junction temperature of the IC internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is a non-latch protection. There is a hysteresis of about 20°C. Once the junction temperature drops below 130°C, the MP2321 starts up.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, but a large R2 makes the FB noise sensitive. Then R1 can be determined with Equation (11):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (11)$$

Where V_{REF} is 0.6V, typically. The feedback circuit is shown in Figure 8.

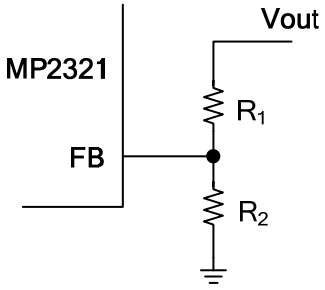

Figure 8: Feedback Network

Table 2 lists recommended resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages (10)

VOUT (V)	R1 (kΩ)	R2 (kΩ)
1.0	27	40.2
1.2	40.2	40.2
1.5	60.4	40.2
1.8	80.6	40.2
2.5	127	40.2
3.3	182	40.2
5	294	40.2

NOTE:

10) The feedback resistors in Table 2 are optimized for 500kHz of switching frequency. The detailed schematics are shown in the typical application circuit section.

Setting the Frequency

Set forced PWM mode switching frequency by connecting a resistor (R6) from VIN to FREQ/MODE and leaving R7 not stuffed (NS) (see Figure 9). Refer to the MODE Selection section on page 12 for more detail.

Determine R6 with Equation (12):

$$R6(k\Omega) = \frac{\left[\frac{Vo \times 10^6}{F_{SW}(kHz) \times V_{IN}} - T_{Delay_PWM}(ns)\right] \cdot (V_{IN} - 0.4)}{14.5} \quad (12)$$

Where T_{Delay_PWM} is about 15ns.

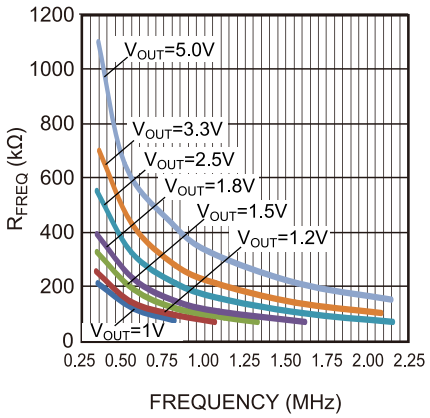

Figure 9: R6 vs. Forced PWM Mode Switching Frequency

Set the auto PFM/PWM mode switching frequency by connecting a resistor (R7) from FREQ/MODE pin to ground and leaving R6 not stuffed (NS) (see Figure 10). Determine R7 with Equation (13):

$$R7(k\Omega) = \frac{\left[\frac{Vo \times 10^6}{F_{SW}(kHz) \times V_{IN}} - T_{Delay_PFM}(ns)\right] \cdot (V_{IN} - 0.4)}{13} \quad (13)$$

Where T_{Delay_PFM} is about 10ns.

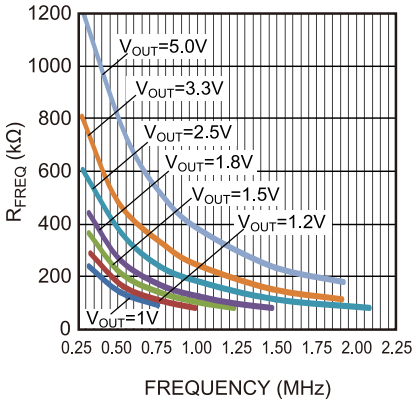

Figure 10: R7 vs. Auto PFM/PWM Mode Switching Frequency

Equation (12) and Equation (13) show the typical switching frequency calculation formulas. The actually frequency changes slightly at different load currents and different input voltages.

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Selecting the Inductor

An inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. An inductor with a larger value results in less ripple current and lower output ripple voltage. However, a larger inductor also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be 30% to 40% of the maximum output current and the peak inductor current to be below the maximum switch current limit. The inductance value can be calculated with Equation (14):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (15):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (16):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (16)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (17):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (17)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (18):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (18)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (19):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (19)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (20):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (20)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (21):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (21)$$

The output voltage ripple caused by the ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through the capacitor Cr.

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (22):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (22)$$

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A larger output capacitor can also achieve a better load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (23):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (23)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{ss} is the soft-start time.

PG Pull-Up

It is recommended that PG is pulled up to VCC for proper operation. If PG is pulled up to external voltage or if connecting two or more PG together, connect a diode from PG to EN as shown in Fig.11 and Fig.12. In this case PG will de-assert low when EN signal is low. But PG will not de-assert low when input power is off and EN signal is high condition.

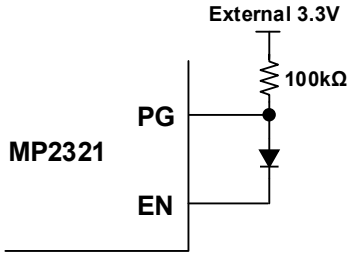

Figure 11: PG Pull up to external power supply with enable control signal --- Single PG Output

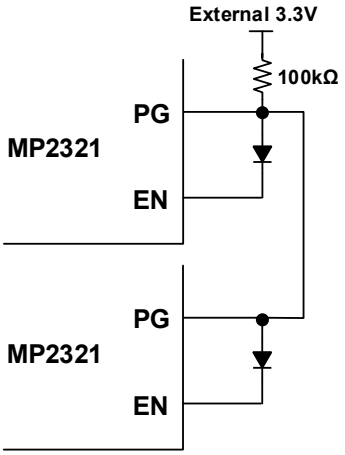

Figure 12: PG Pull up to external power supply with enable control signal --- PG parallel Output

External Bootstrap Diode

The BST voltage may become insufficient in particular conditions. In this case, an external bootstrap diode can be added to enhance the efficiency of the regulator and help prevent BST voltage insufficiency in light-load PFM operation. BST voltage insufficiency is more likely to occur at either of the following conditions:

- VIN is low
- Duty cycle is large: D = $\frac{V_{OUT}}{V_{IN}}$ > 65%

In these cases, if the BST voltage is insufficient, the output ripple voltage may become extremely large at light-load condition or show poor efficiency at heavy-load condition. Add an external BST diode from VCC to BST (see Figure 13).

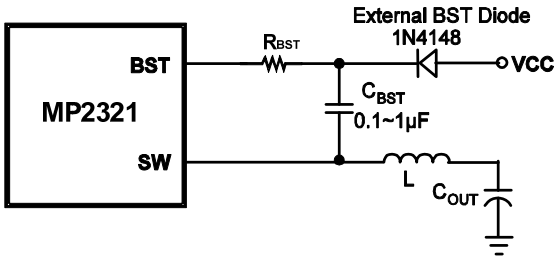

Figure 13: Optional External Bootstrap Diode

The recommended external BST diode is IN4148.

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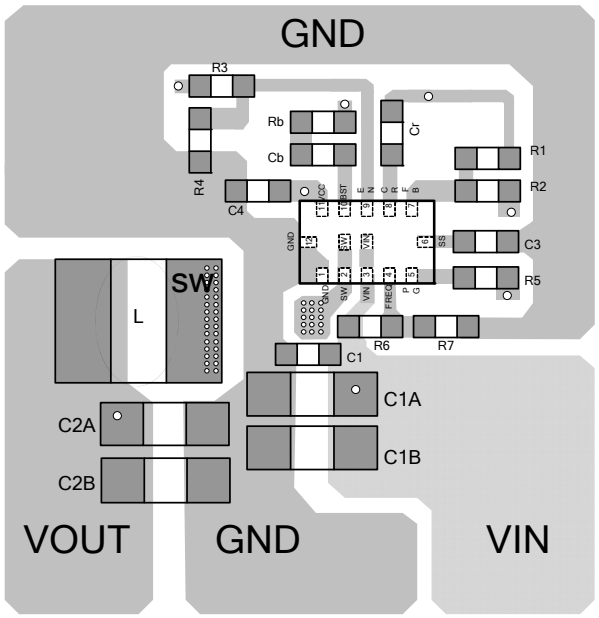
PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 14 and follow the guidelines below.

1. Place the high current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to IN and GND as possible.
3. Place the mode/frequency circuit close to the part.
4. Place the external feedback resistors next to FB.
5. Keep the switching node (SW) short and away from the feedback network.

For better performances, it is recommended to use four-layer boards. Figure 14 shows the top and bottom layers (Inner 1 and Inner 2 are both GND).



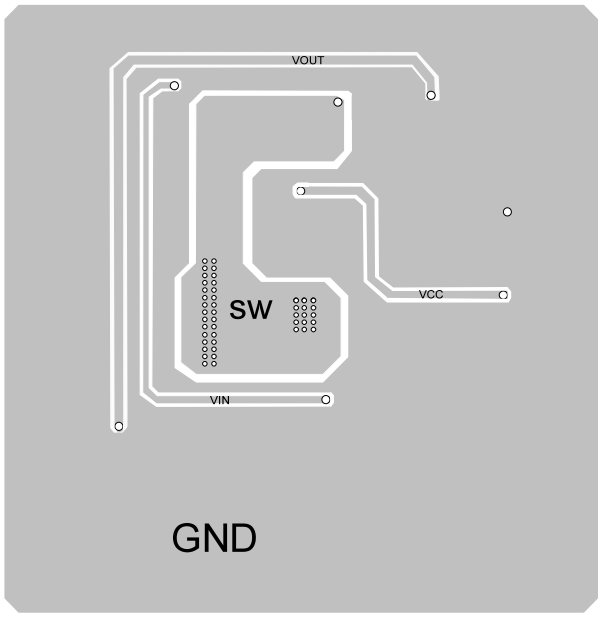


Figure 14: Sample Board Layout

Design Example

Table 3 shows a design example when ceramic capacitors are applied.

Table 3: Design Example

V_{IN}	12V
V_{OUT}	1.2V
I_{OUT}	2A

The detailed application schematic is shown in Figure 15 through Figure 21. The typical performance and waveforms are shown in the Typical Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

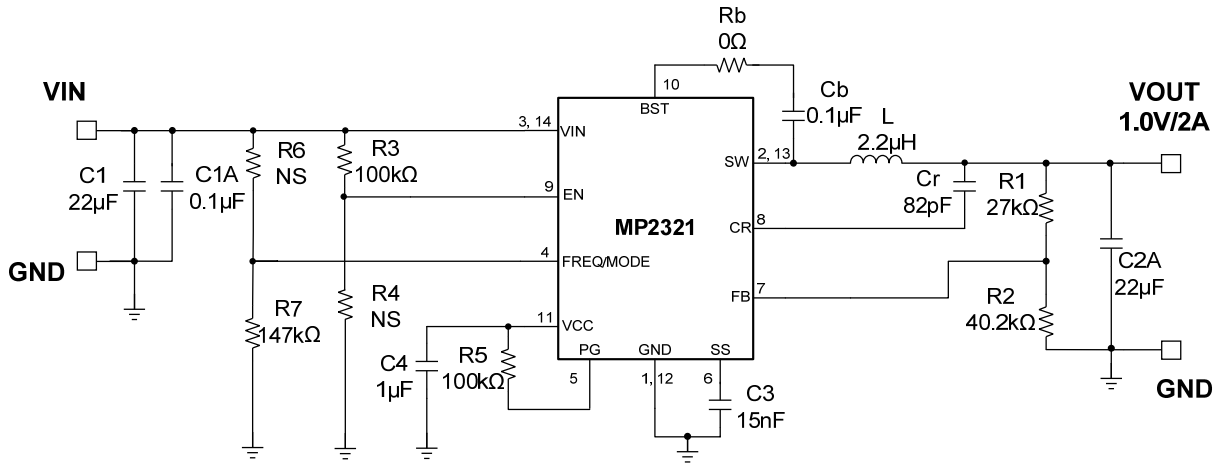

Figure 15: VIN = 12V, V_{OUT} = 1.0V, I_{OUT} = 2A, F_S = 500kHz

NOTE:

a. Use R6 = 130kΩ to set forced PWM. Use R7 = 147kΩ to set auto PFM/PWM. The recommended R6 and R7 values are based on Equation (12) and Equation (13) and optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

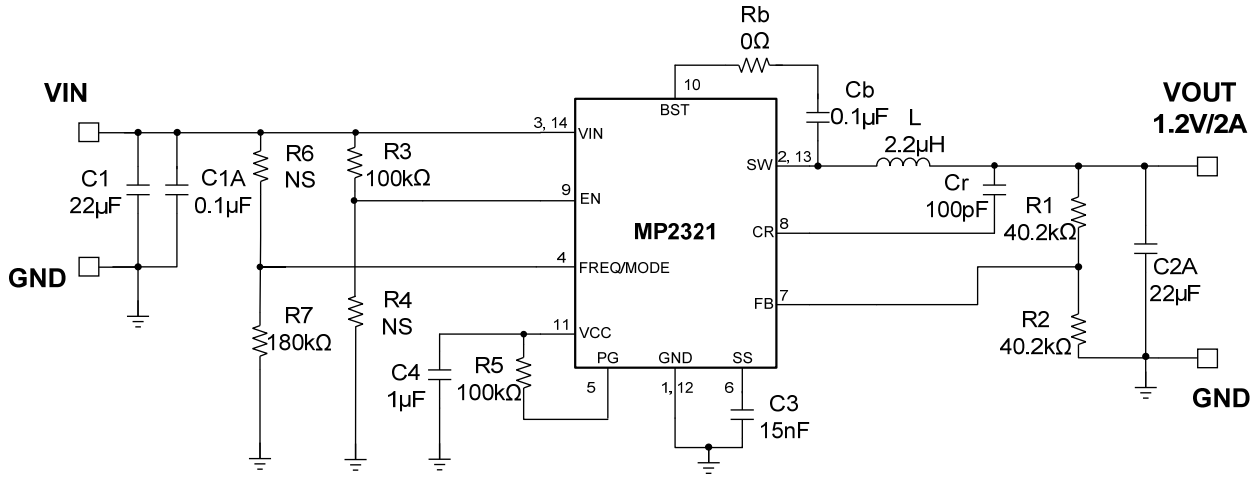

Figure 16: VIN = 12V, V_{OUT} = 1.2V, I_{OUT} = 2A, F_S = 500kHz

NOTE:

a. Use R6 = 158kΩ to set forced PWM. Use R7 = 180kΩ to set auto PFM/PWM. The recommended R6 and R7 values are based on Equation (12) and Equation (13) and optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

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TYPICAL APPLICATION CIRCUITS *(continued)*

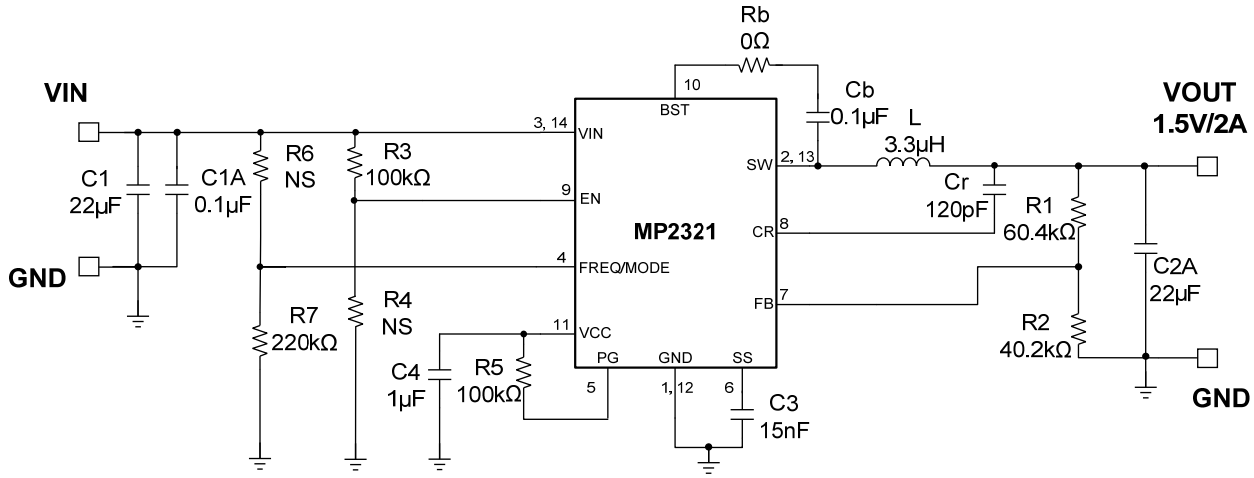

Figure 17: VIN = 12V, V_{OUT} = 1.5V, I_{OUT} = 2A, F_S = 500kHz

NOTE:

a. Use R6 = 196kΩ to set forced PWM. Use R7 = 220kΩ to set auto PFM/PWM. The recommended R6 and R7 values are based on Equation (12) and Equation (13) and optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

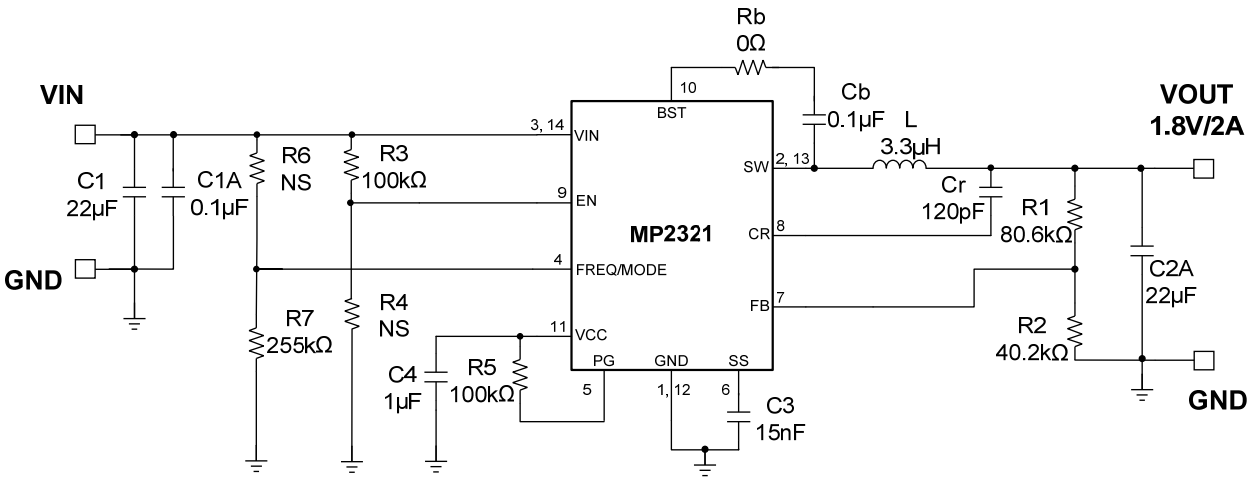

Figure 18: VIN = 12V, V_{OUT} = 1.8V, I_{OUT} = 2A, F_S = 500kHz

NOTE:

a. Use R6 = 243kΩ to set forced PWM. Use R7 = 255kΩ to set auto PFM/PWM. The recommended R6 and R7 values are based on Equation (12) and Equation (13) and optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

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TYPICAL APPLICATION CIRCUITS *(continued)*

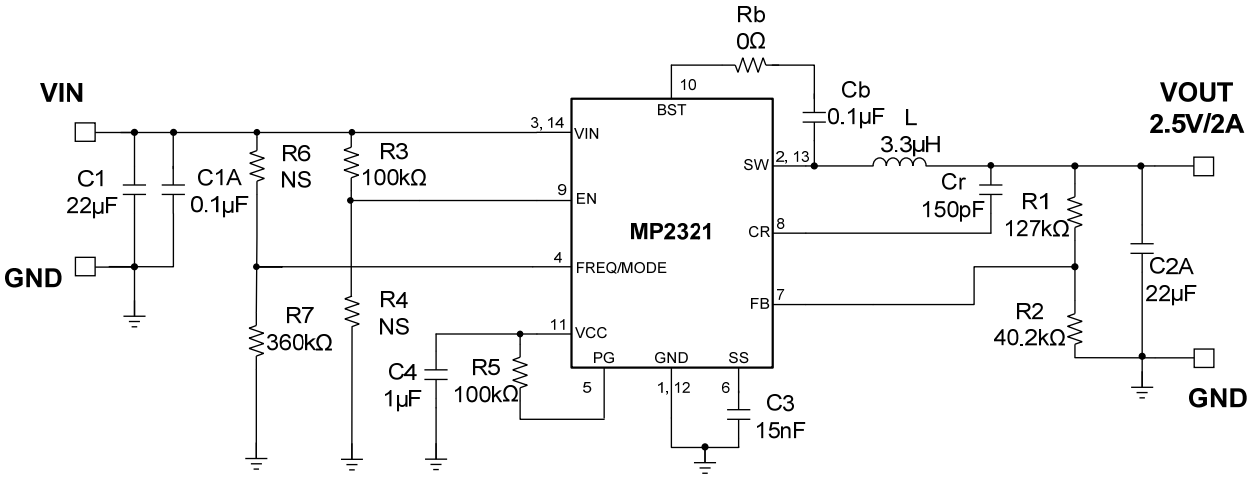

Figure 19: VIN = 12V, V_{OUT} = 2.5V, I_{OUT} = 2A, F_S = 500kHz

NOTE:

a. Use R6 = 348kΩ to set forced PWM. Use R7 = 360kΩ to set auto PFM/PWM. The recommended R6 and R7 values are based on Equation (12) and Equation (13) and optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

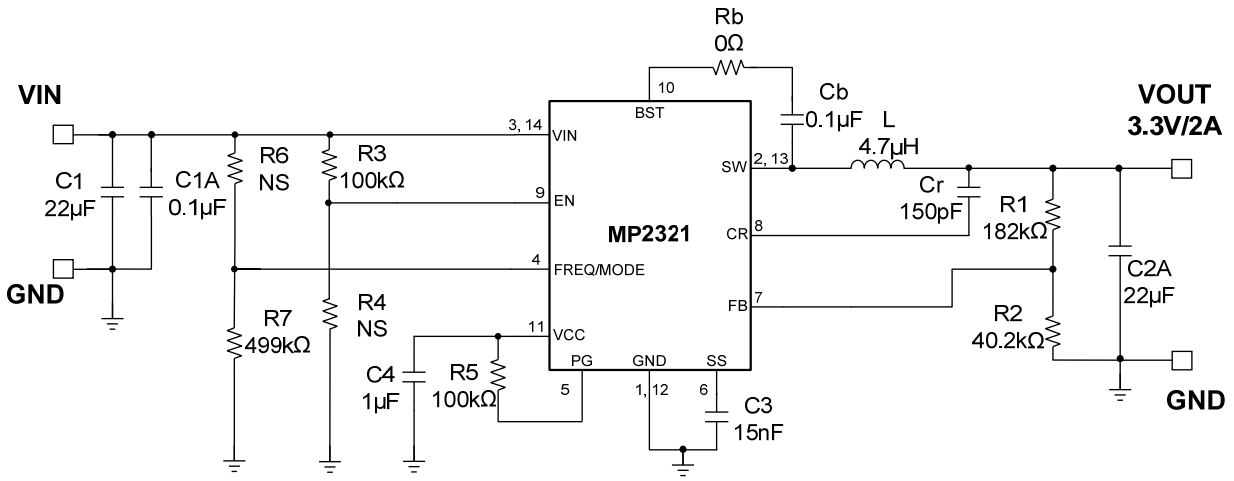

Figure 20: VIN = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, F_S = 500kHz

NOTE:

a. Use R6 = 453kΩ to set forced PWM. Use R7 = 499kΩ to set auto PFM/PWM. The recommended R6 and R7 values are based on Equation (12) and (13) and optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

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TYPICAL APPLICATION CIRCUITS *(continued)*

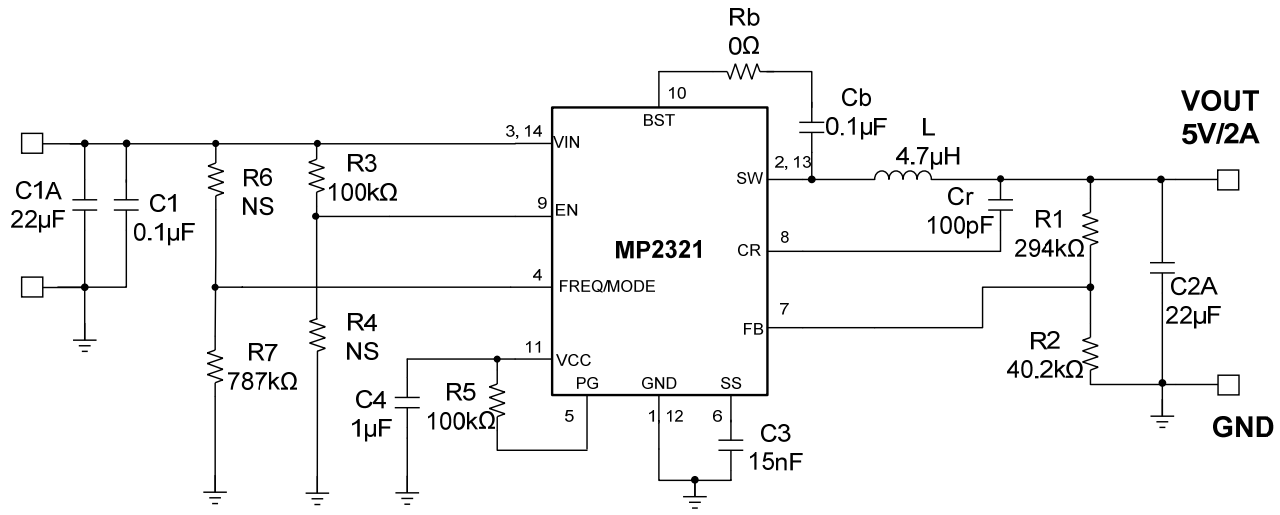

Figure 21: VIN = 12V, V_{OUT} = 5V, I_{OUT} = 2A, F_S = 500kHz

NOTE:

a. Use R6 = 715kΩ to set forced PWM. Use R7 = 787kΩ to set auto PFM/PWM. The recommended R6 and R7 values are based on Equation (12) and Equation (13) and optimized according to test results.

b. Recommend to pull-up PG to IC VCC pin. If need pull-up PG to external power supply, please refer to the PG description in application information section.

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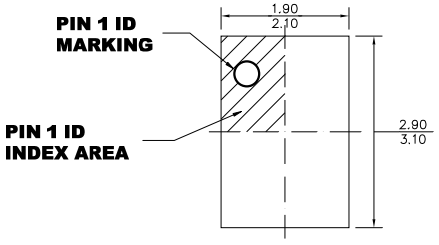
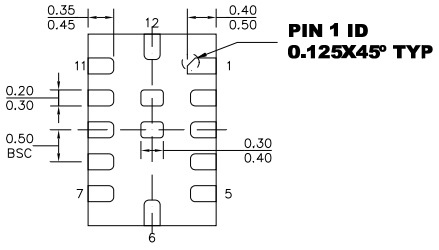
PACKAGE INFORMATION

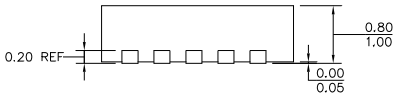
QFN-14 (2mmX3MM)



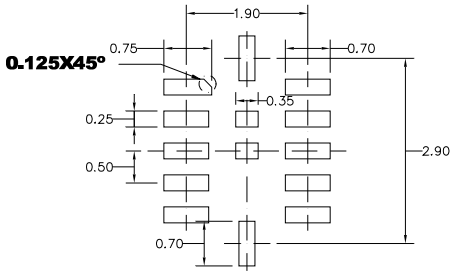
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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