MP8759

26V, 8A, Low I_Q, High-Current, Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP8759 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. It offers a very compact solution that achieves 8A of continuous output current and 10A peak output current with excellent load and line regulation over a wide input supply range.

The MP8759 operates with high efficiency over a wide output-current load range based on MPS' proprietary switching loss reduction technique and internal low $R_{DS(ON)}$ power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

Full protection features include over-current limit, over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The converter requires a minimum number of external components and is available in a QFN-12 (2mmx3mm) package.

FEATURES

- Wide 4.5V to 26V Operating Input Range
- Output Adjustable from 0.6V
- Ultrasonic Mode (USM)
- 117μA Low Quiescent Current
- 8A Continous Output Current
- 10A Peak Output Current
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop
- 1% Reference Voltage
- Internal Soft Start
- Output Discharge
- 700kHz Switching Frequency
- OCP, OVP, UVP (Hiccup), and Thermal Shutdown
- Available in a QFN-12 (2mmx3mm) Package

APPLICATIONS

- Laptop Computer
- Tablet PC
- Networking Systems
- Flat-Panel Television and Monitors
- Distributed Power Systems

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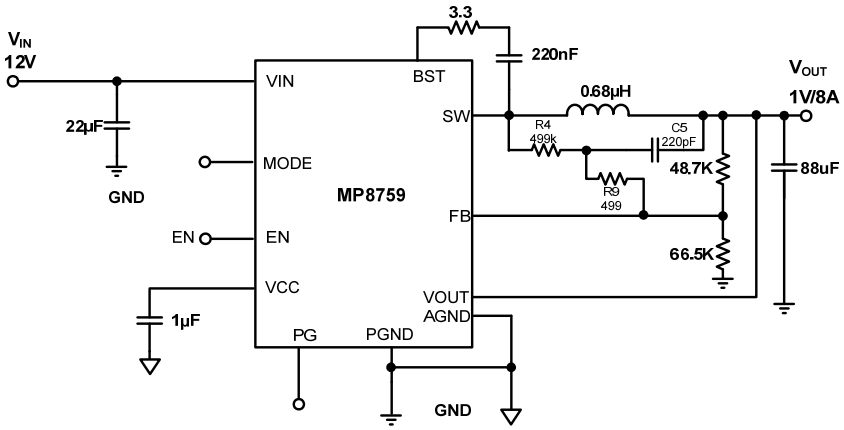
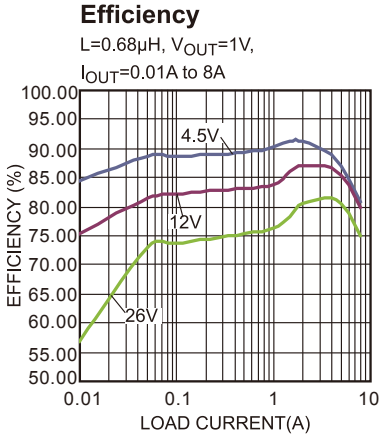
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8759GD	QFN-12 (2mmx3mm)	*See Below*

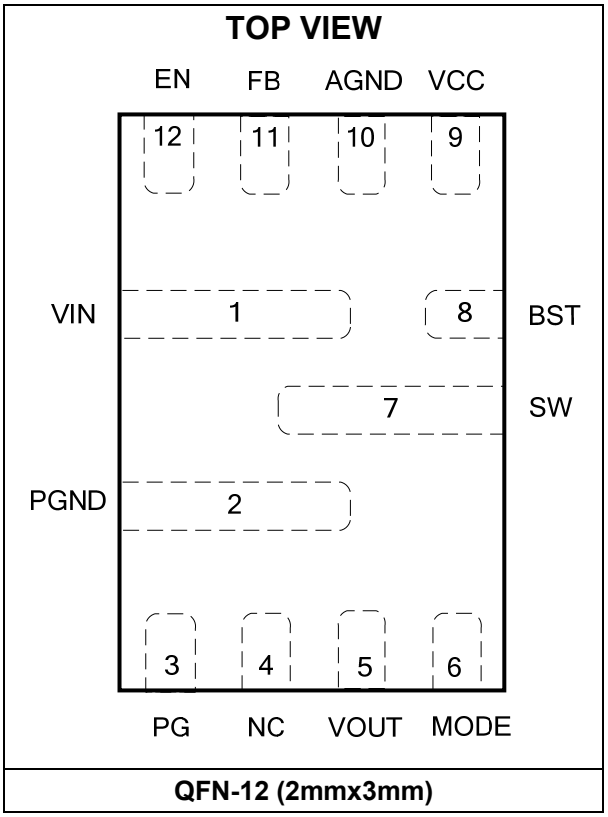
* For Tape & Reel, add suffix –Z (e.g. MP8759GD–Z)

TOP MARKING

AQQ
YWW
LLL

AQQ: Product code of MP8759GD
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}).....26V
V_{SW}..... -0.6V to V_{IN} + 0.3V
V_{SW} (25ns)..... -3.6V to V_{IN} + 4.5V
V_{BST}..... V_{SW} + 4.5V
V_{OUT}.....-0.3V to 6.5V
All other pins..... -0.3V to +4.5V
Continuous power dissipation (T_A = +25°C) **(2)**
QFN-12 (2mmx3mm)..... 1.8W
Junction temperature..... .150°C
Lead temperature.....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}).....4.5V to 24V
Output voltage (V_{OUT})..... 0.6V to 5.5V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4)

	Θ_{JA}	Θ_{JC}	
QFN-12 (2mmx3mm)	70	15	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		1	2	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 3.3V, VOUT = 5.5V		117	135	μA
MOSFET						
High-side switch-on resistance	$HS_{RDS(ON)}$			25		mΩ
Low-side switch-on resistance	$LS_{RDS(ON)}$			12		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
Low-side valley current limit	I_{LIMIT}		10.5	12	13.5	A
Switching Frequency and Timer						
Switching frequency	F_S			700		kHz
Constant on timer	T_{ON}	V_{IN} = 10V, V_{OUT} = 5V, forced PWM mode		710		ns
Minimum on time[5]	T_{ON_Min}			50		ns
Minimum off time[5]	T_{OFF_Min}			250		ns
Ultrasonic Mode (USM)						
Ultrasonic mode operation period	T_{USM}		20	30	40	μs
Over-Voltage (OVP) and Under-Voltage Protection (UVP)						
OVP rising threshold	V_{OVP_RISING}		117%	122%	127%	V_{REF}
OVP falling threshold	$V_{OVP_FALLING}$		112%	117%	122%	V_{REF}
UVP-1 threshold	V_{UVP-1}		70%	75%	80%	V_{REF}
UVP-1 deglitch timer[5]	T_{UVP-1}			50		μs
UVP-2 threshold	V_{UVP-2}		45%	50%	55%	V_{REF}
Reference and Soft Start (SS)						
Feedback voltage	V_{REF}		594	600	606	mV
Soft-start time	T_{SS}	VOUT 10% to 90%		1.2		ms
MODE						
PWM mode input logic low threshold	V_{MODE_H}		2.6			V
PFM with USM threshold	V_{MODE_MID}		1.2		1.9	V
PFM without USM threshold	V_{MODE_L}				0.4	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable and UVLO						
Enable rising threshold	V_{EN_H}		1.15	1.25	1.35	V
Enable hysteresis	V_{EN-HYS}			100		mV
Enable input current	I_{EN}	V_{EN} = 2V		5		µA
		V_{EN} = 0V		0		
VIN under-voltage lockout threshold rising	VIN_{VTH}		4	4.25	4.5	V
VIN under-voltage lockout threshold hysteresis	VIN_{HYS}			250		mV
VCC Regulator						
VCC regulator	V_{CC}		3.5	3.6	3.7	V
VCC load regulation		I_{CC} = 5mA		5		%
Power Good (PG)						
PG when FB rising (good)	$PG_{Rising(Good)}$	V_{FB} rising, percentage of V_{FB}		95		%
PG when FB falling (fault)	$PG_{Falling(Fault)}$	V_{FB} falling, percentage of V_{FB}		85		
PG when FB rising (fault)	$PG_{Rising(Fault)}$	V_{FB} rising, percentage of V_{FB}		115		
PG when FB falling (good)	$PG_{Falling(Good)}$	V_{FB} falling, percentage of V_{FB}		105		
Power good low-to-high delay	PG_{Td}			500		µs
EN low to power good low delay	$PG_{Td\ EN\ low}$				1	µs
Power good sink-current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			5	µA
Thermal Protection						
Thermal shutdown(5)	T_{SD}			150		°C
Thermal shutdown hysteresis(5)	T_{SD-HYS}			25		°C

NOTE:

5) Guaranteed by engineering sample characterization.

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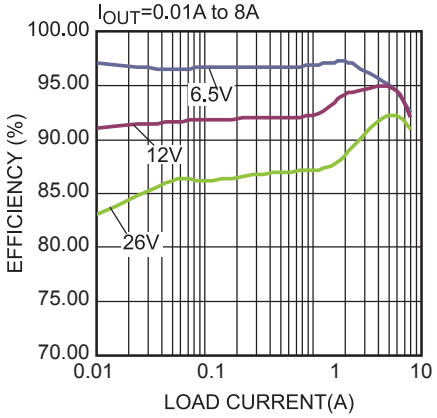
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH/3.1mΩ, f_S = 700kHz, T_A = +25°C, PFM mode, unless otherwise noted.

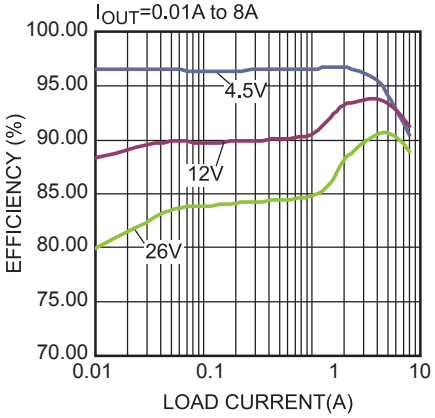
Efficiency

L=1.5µH, V_{OUT}=5V,
I_{OUT}=0.01A to 8A



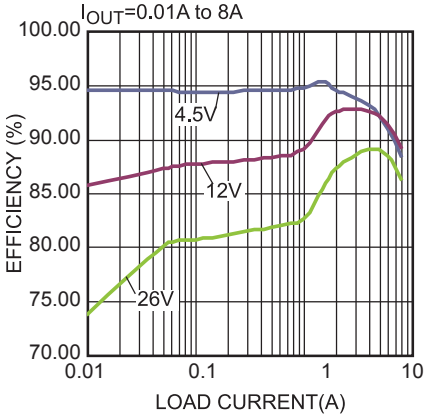
Efficiency

L=1.5µH, V_{OUT}=3.3V,
I_{OUT}=0.01A to 8A



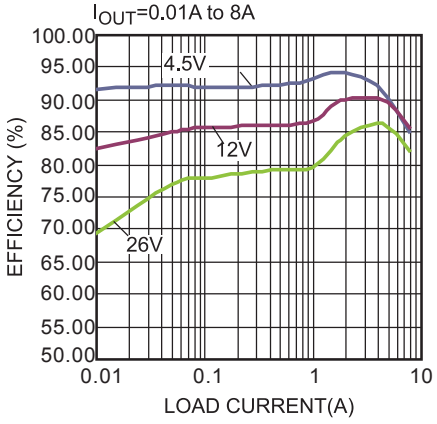
Efficiency

L=1.2µH, V_{OUT}=2.5V,
I_{OUT}=0.01A to 8A



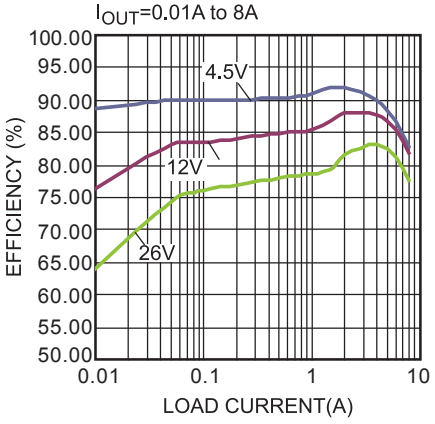
Efficiency

L=0.95µH, V_{OUT}=1.8V,
I_{OUT}=0.01A to 8A



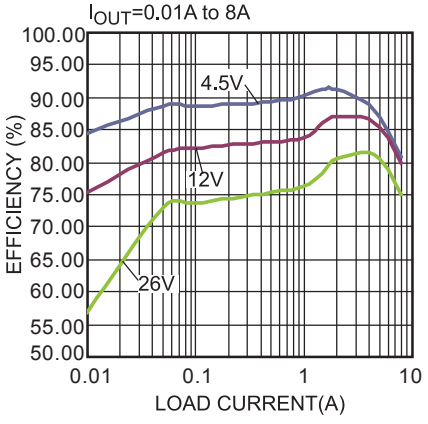
Efficiency

L=0.95µH, V_{OUT}=1.2V,
I_{OUT}=0.01A to 8A



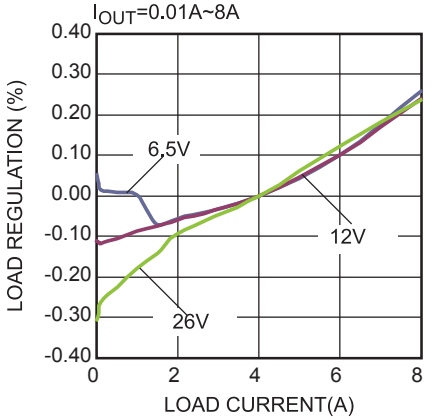
Efficiency

L=0.68µH, V_{OUT}=1V,
I_{OUT}=0.01A to 8A



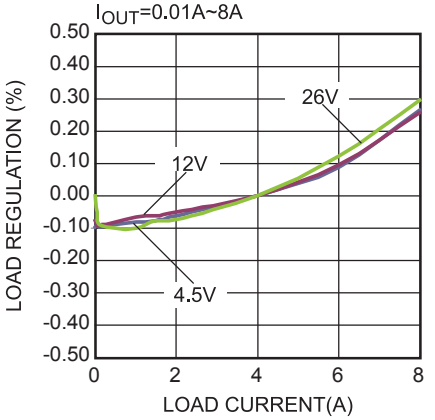
Load Regulation

V_{OUT}=5V, V_{IN}=6.5V~26V,
I_{OUT}=0.01A~8A



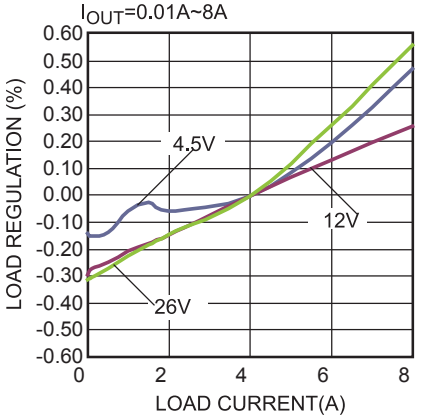
Load Regulation

V_{OUT}=3.3V, V_{IN}=4.5V~26V,
I_{OUT}=0.01A~8A



Load Regulation

V_{OUT}=2.5V, V_{IN}=4.5V~26V,
I_{OUT}=0.01A~8A



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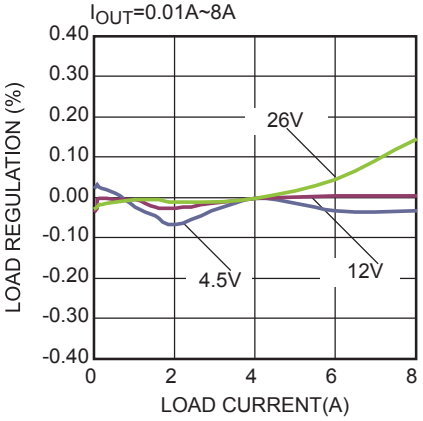
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH/3.1mΩ, f_S = 700kHz, T_A = +25°C, PFM mode, unless otherwise noted.

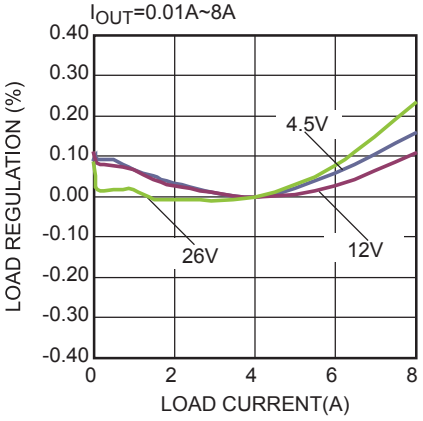
Load Regulation

V_{OUT}=1.8V, V_{IN}=4.5V~26V,
I_{OUT}=0.01A~8A



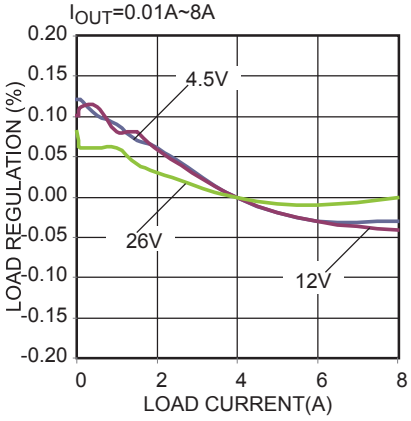
Load Regulation

V_{OUT}=1.2V, V_{IN}=4.5V~26V,
I_{OUT}=0.01A~8A

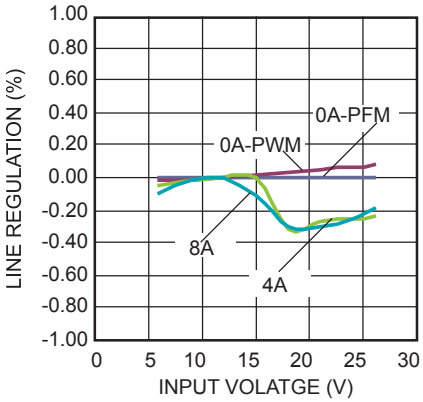


Load Regulation

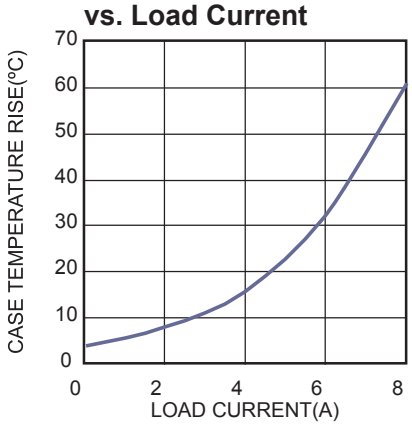
V_{OUT}=1V, V_{IN}=4.5V~26V,
I_{OUT}=0.01A~8A



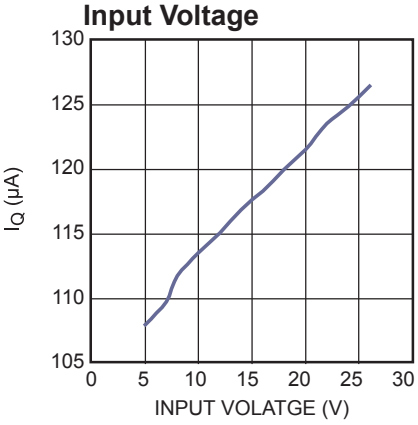
Line Regulation



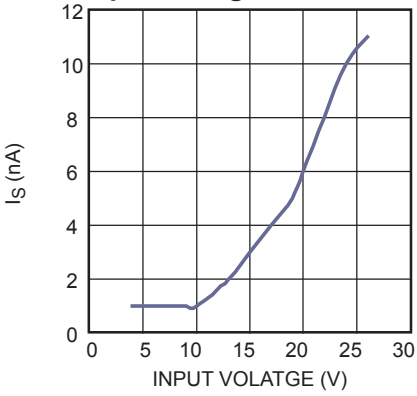
Case Temperature Rise vs. Load Current



Quiescent Current vs. Input Voltage



Shutdown Current vs. Input Voltage



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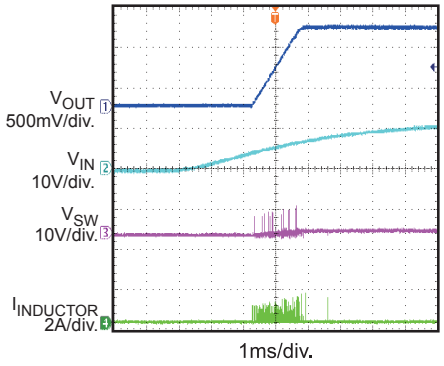
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH/3.1mΩ, f_S = 700kHz, T_A = +25°C, PFM mode, unless otherwise noted.

Start-Up through Input Voltage

I_{OUT}=0A



Shutdown through Input Voltage

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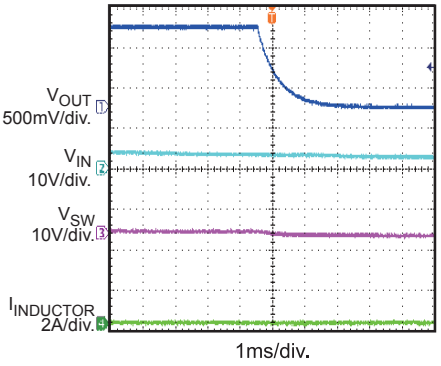
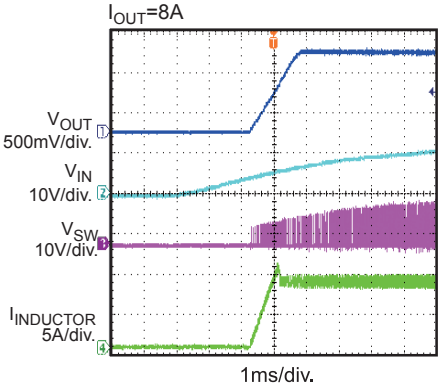


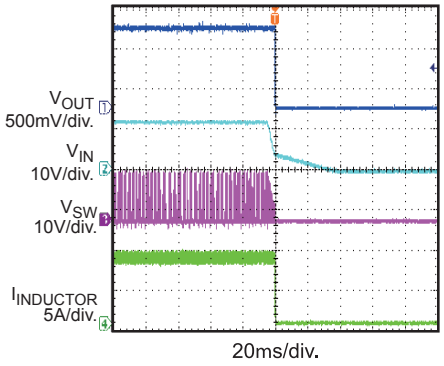
Start-Up through Input Voltage

I_{OUT}=8A



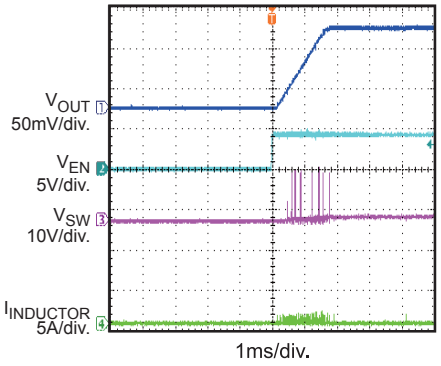
Shutdown through Input Voltage

I_{OUT}=8A



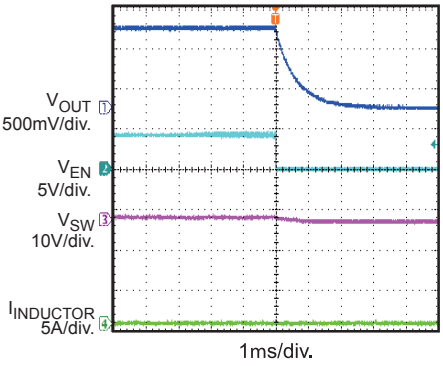
Start-Up through Enable

I_{OUT}=0A



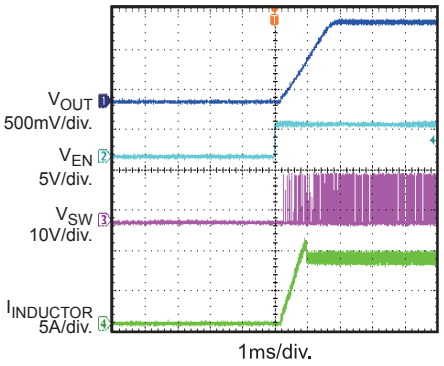
Shutdown through Enable

I_{OUT}=0A



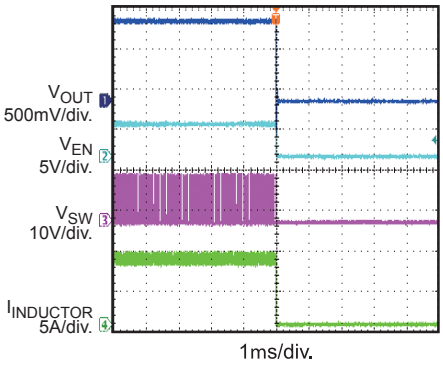
Start-Up through Enable

I_{OUT}=8A



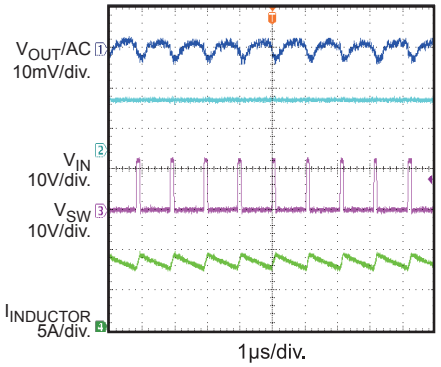
Shutdown through Enable

I_{OUT}=8A



Output Ripple

I_{OUT}=8A



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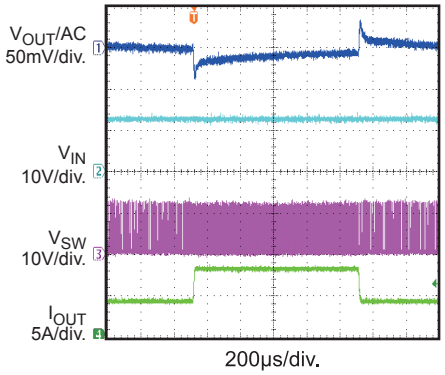
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

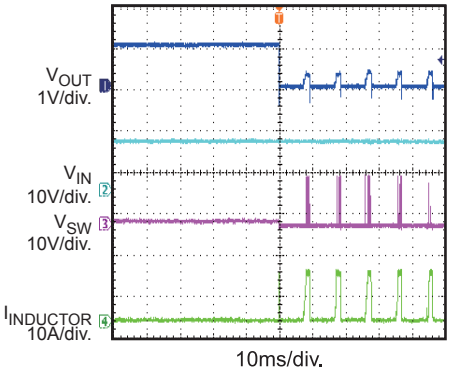
V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH/3.1mΩ, f_S = 700kHz, T_A = +25°C, PFM mode, unless otherwise noted.

4A to 8A Load Transient



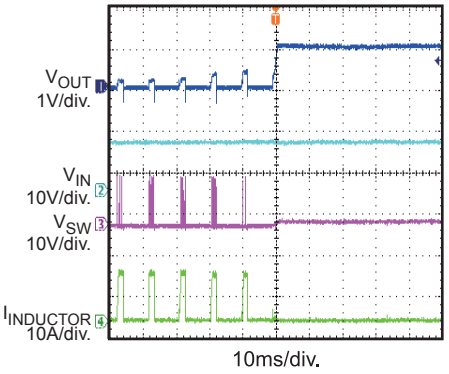
Short-Circuit Entry

I_{OUT}=0A



Short-Circuit Recovery

I_{OUT}=0A



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PIN FUNCTIONS

PIN #	Name	Description
1	VIN	**Supply voltage.** VIN supplies power for internal MOSFET and regulator. The MP8759 operates from a 4.5V to 26V input rail. Decouple the input rail with an input capacitor. Use wide PCB traces and multiple vias to make the connection. Applied at least two layers for this input trace.
2	PGND	**Power ground.** Connect using wide PCB traces and multiple vias large enough to handle the load current.
3	PG	**Power good output.** The output of PG is an open-drain signal. PG is high if the output voltage is higher than 95% or lower than 105% of the nominal voltage.
4	NC	**Do not connect.** NC must be left floating.
5	VOUT	**VOUT is used to sense the output voltage of the buck regulator.** Connect VOUT to the output capacitor of the regulator directly. Keep the VOUT sensing trace far away from the SW node. Vias should also be avoided on the VOUT sensing trace. A trace larger than 25mil is required.
6	MODE	**USM, PFM, PWM mode selection.** Pull MODE higher than 2.6V to operate the MP8759 in forced PWM mode. Float MODE to operate the MP8759 in PFM mode with ultrasonic mode (USM) at light load. Connect MODE to ground to operate the MP8759 in PFM mode without USM.
7	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the PWM duty cycle on time. The inductor current drives SW negative during the off-time. The on resistance of the low-side switch and the internal diode fixes the negative voltage. Use wide and short PCB traces to make the connection. Keep the SW pattern area minimized.
8	BST	**Bootstrap.** A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
9	VCC	**Internal VCC LDO output.** The driver and control circuits are powered by VCC. Decouple with a minimum 1μF ceramic capacitor placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
10	AGND	**Signal logic ground.** AGND is the Kelvin connection to PGND.
11	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider connected between output and GND.
12	EN	**Enable.** EN is a digital input that turns the regulator on or off. When the power supply of the control circuit is ready, drive EN high to turn on the regulator. Drive EN low to turn off the regulator.

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BLOCK DIAGRAM

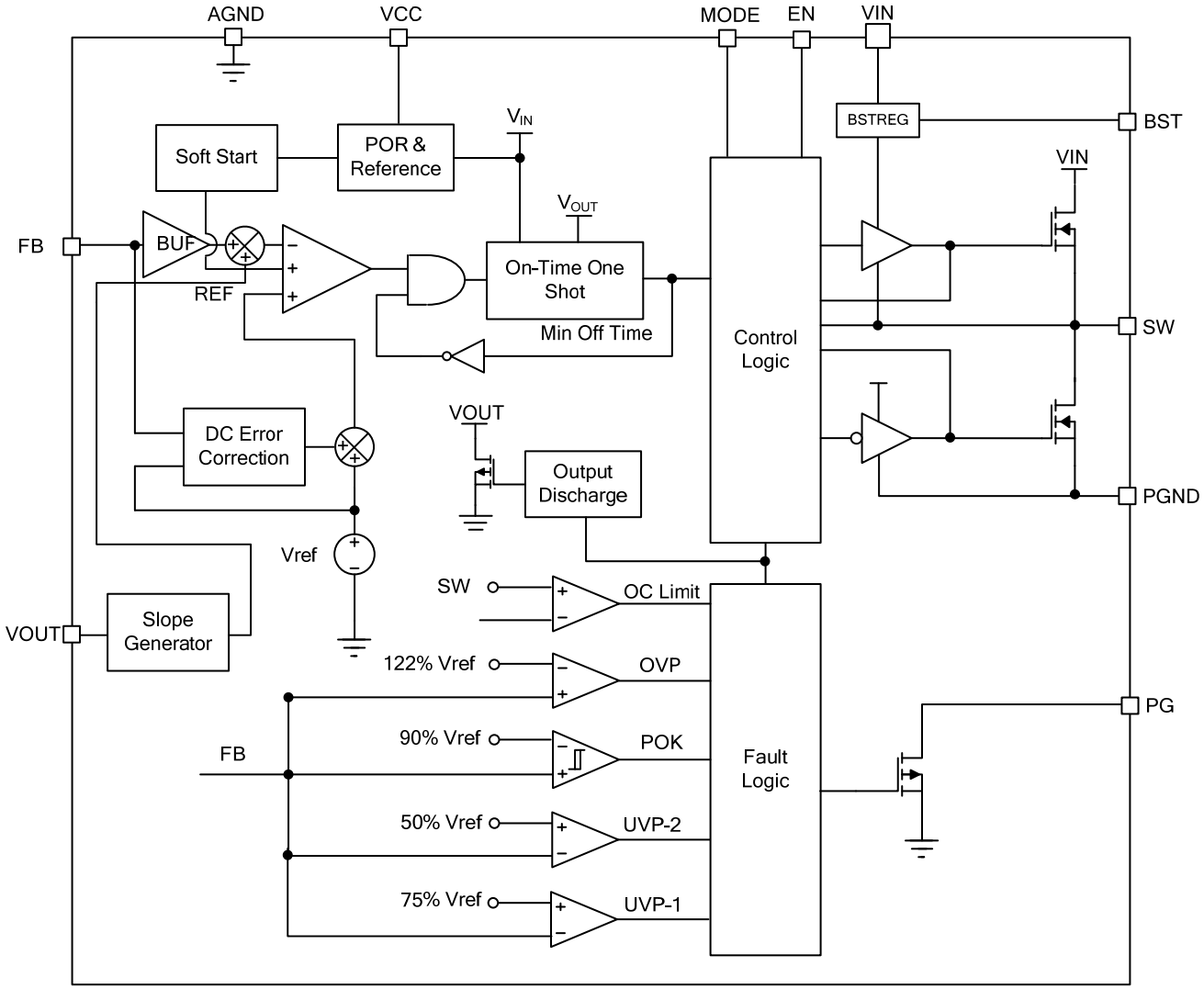

Figure 1: Functional Block Diagram

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OPERATION

PWM Operation

The MP8759 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide a fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. It is turned on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called a shoot-through. To avoid a shoot-through, a dead time (DT) is generated internally between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves the jitter performance without affecting line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until the next period.

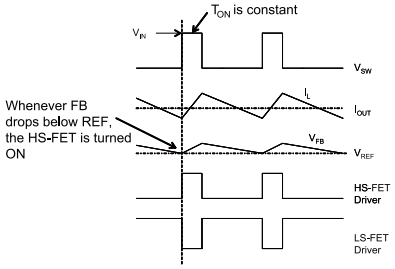

Figure 2: Heavy-Load Operation

In CCM operation, the switching frequency is in pulse-width modulation (PWM) mode and is fairly constant.

Light-Load Power Save Mode

The inductor current decreases as the load decreases. If MODE is floating or pulled to ground, once the inductor current reaches zero, the operation switches from continuous conduction mode (CCM) to discontinuous conduction mode (DCM).

The power save mode operation is shown in Figure 3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by a one-shot on-timer, as shown in Equation 1. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, V_{FB} does not reach V_{REF} while the inductor current is approaching zero. The LS-FET driver switches to tri-state (high-Z) whenever the inductor current reaches zero. As a result, the efficiency at light load is greatly improved. In light-load condition, the HS-FET is not turned on as frequently as in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the MP8759 reduces the switching frequency to achieve high efficiency.

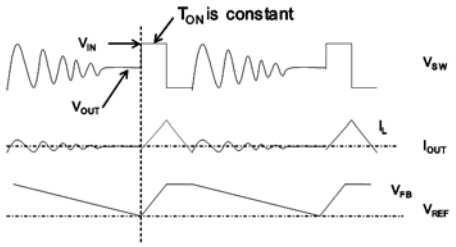

Figure 3: Light-Load Operation

As the output current increases from light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, so the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds critical levels. Afterward, the

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switching frequency stays fairly constant over the output current range.

DC Auto-Tune Loop

The MP8759 applies DC auto-tune loop to balance the DC error between V_{FB} and V_{REF} by adjusting the comparator input REF to make V_{FB} follow V_{REF}. This is a slow loop, so the load and line regulation improve without affecting the transient performance. The relationship between V_{FB}, V_{REF}, and REF is shown in Figure 4.

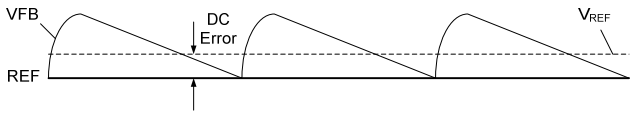

Figure 4: DC Auto-Tune Loop Operation

External Ramp for Low Output Voltage

The MP8759 uses an internal ramp compensation control scheme to improve stability with a pure ceramic output capacitor. In some operating cases, the internal ramp amplitude is not sufficient to make the loop stable with ceramic capacitors. Therefore, an extra external ramp around 20mV is needed for loop stabilization. Please refer to the Component Selection section in page 15 for details.

Large Duty Operation

The MP8759 can support larger duty operations with its internal T_{ON} extension function. When the part detects that FB is lower than V_{REF}, and VIN - VOUT < 2V, T_{ON} and the duty cycle can be extended. T_{ON} stops extending if FB is greater than REF or if T_{ON} meets its limitation.

Light-Load Ultrasonic Mode (USM)

Ultrasonic mode (USM) is used to keep the switching frequency above audible frequency areas during light-load or no-load conditions.

Once the part detects that both the HS-FET and LS-FET are off for about 30µs, T_{ON} shrinks to keep VOUT under regulation with optimal efficiency. If the load continues reducing, then the part discharges VOUT to ensure that FB is smaller than 102% of the internal reference. The HS-FET turns on again once the internal FB reaches V_{REF} and then stops switching.

USM is selected by the MODE setting. Float MODE to operate the MP8759 in PFM mode with USM in light-load condition.

Configuring the EN Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator.

To start up the MP8759 automatically, pull EN up to the input voltage through a resistive voltage divider. Please refer to the UVLO Protection Section on page 14 for details.

MODE Selection

MODE is used to select the MP8759's working mode. Pull MODE higher than 2.6V to operate the MP8759 in forced PWM mode. Float MODE to operate the MP8759 in PFM mode with USM at light load. Connect MODE to ground to operate the MP8759 in PFM mode without USM.

Soft Start (SS)

The MP8759 employs a soft-start (SS) mechanism to ensure a smooth output during power-up. When EN rises high, the internal reference voltage and the output voltage ramp up gradually. Once the reference voltage reaches its target value, the soft start finishes and the circuit enters steady-state operation.

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the internal FB node.

Power Good (PG)

The MP8759 uses a power good (PG) output to indicate whether the output voltage of the buck regulator is ready or not. PG is the open drain of the MOSFET and should be connected to VCC or another voltage source through a resistor (e.g.: 100k). After the input voltage is applied, the MOSFET is turned on and PG is pulled to GND before SS is ready. Once the FB voltage reaches 95% of V_{REF}, PG is pulled high after a 500µs delay. When the FB voltage drops to 85% of V_{REF}, PG is pulled low. When the output voltage is higher than 115% of the internal reference, PG is pulled low. PG rises high again after the output voltage drops below 105% of the internal reference voltage.

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Over-Current Protection (OCP)

The MP8759 has a cycle-by-cycle over-current limiting control. The current-limit circuit employs a valley current-sensing algorithm. The part uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, PWM is not allowed to initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node so that GND should be connected to the source terminal of the bottom MOSFET.

Since the comparison is done during the HS-FET off and LS-FET on states, the OC trip level sets the valley level of the inductor current. Thus, the load current at the over-current threshold (I_{OC}) can be calculated with Equation (2):

$$I_{OC} = I_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor; and the output voltage can fall off. As a result, the device encounters the under-voltage protection threshold and hiccup.

Over-/Under-Voltage Protection (OVP/UVP)

The MP8759 monitors the output voltage to detect over-voltage and under-voltage. Once the feedback voltage rises higher than 122% of the feedback voltage, the OVP comparator output goes high and the circuit turns off the HS-FET driver. The LS-FET driver turns on, acting as a current source. The output is then discharged to remain within the normal range. The MP8759 exits this regulation period when the feedback voltage falls below 117% of the reference voltage.

When the feedback voltage falls below 75% of the V_{REF} but is higher than 50%, the UVP-1 comparator output goes high, and the part attempts to restart with hiccup mode periodically for about 50μs if the feedback voltage remains in this range.

When the feedback voltage falls below 50% of V_{REF}, the UVP-2 comparator output goes high and the part enters hiccup mode directly after the comparator and logic delay.

Under-Voltage Lockout (UVLO) Protection

The MP8759 can start up only when VIN is higher than the under-voltage lockout (UVLO) rising threshold voltage. The MP8759 shuts down when VIN is lower than its falling threshold. The UVLO protection is non-latch off.

If an application requires a higher under-voltage lockout (UVLO), use EN to adjust the input voltage UVLO by adding two external resistors (see Figure 5).

It is recommended to use the resistor divider to set the EN voltage above the EN rising threshold and below the 4.5V absolute maximum rating. The rising threshold should be set to provide enough hysteresis to allow for any input supply variations.

To avoid an excessive sink current on EN, keep the EN resistor (R_{UP}) in the range of 1MΩ - 2MΩ. A typical pull-up resistor is 1.5MΩ. The R_{DOWN} value can then be determined by R_{UP} and a 600kΩ internal pull-down resistor.

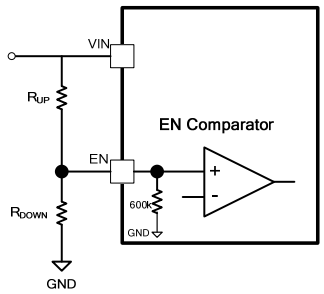

Figure 5: Adjustable UVLO

Connecting EN directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source. The EN voltage must not exceed the 4.5V absolute maximum rating to avoid damaging the IC.

Thermal Shutdown

The MP8759 employs thermal shutdown. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is a non-latch protection. There is a hysteresis of about 25°C. Once the junction temperature drops to about 125°C, a soft start is initiated.

Output Discharge

When EN is low, the MP8759 discharges the output using an internal 6Ω MOSFET.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage with an E-Capacitor or POS Capacitor

For applications that use an electrolytic capacitor or POS capacitor with a controlled ESR output is set as an output capacitor, external compensation is not need. The output voltage is set by feedback resistors R1 and R2 (see Figure 6).

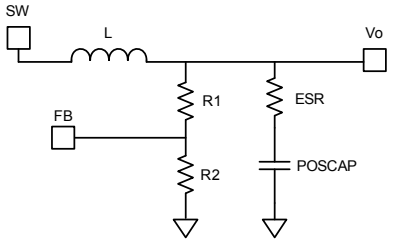

Figure 6: Simplified Circuit of POS Capacitor

The value for R2 must be chosen carefully since a small R2 value leads to considerable quiescent current loss, while a value that is too large makes FB noise sensitive. R2 is recommended to be within 5kΩ - 100kΩ. Typically, set the current through R2 between 5μA - 30μA to create a good balance between the system stability and no-load loss. Considering the output ripple, calculate R1 with Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (3)$$

Setting the Output Voltage with a Pure Ceramic Output Capacitor

The MP8759 employs internal ramp compensation. When the internal compensation is enough for a stable operation with the ceramic output capacitors, the external resistor divider is used to set VOUT. First, choose a value for R2. Then R1 can be determined with Equation (4):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (4)$$

The feedback circuit is shown in Figure 7.

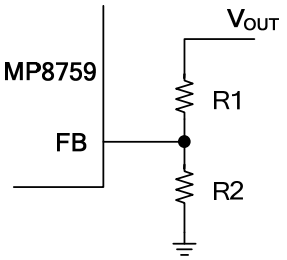

Figure 7: Feedback Network

When the internal ramp compensation is not enough to stabilize the loop with a pure ceramic capacitor, an extra external voltage ramp around 20mV should be added to FB through resistor R4 and capacitor C5.

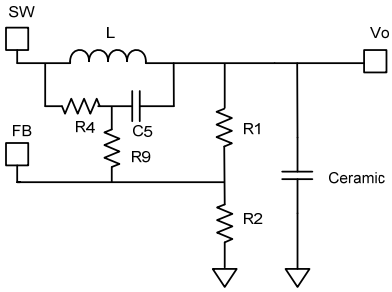

Figure 8: External Ramp Compensation

Figure 8 shows a simplified external ramp compensation for PWM mode. V_{ramp} on FB can be estimated with Equation (5):

$$V_{ramp} = \frac{V_{in} - V_{out}}{R_4 \times C_5} \times T_{on} \quad (5)$$

For better load or line regulation, use a lower V_{ramp}. Usually, V_{ramp} is recommended to be around 20mV.

The MP8759 employs a DC auto-tune loop to balance the DC error between V_{FB} and V_{REF}. V_{FB} can maintain 0.6V, even with an external ramp compensation circuit. Figure 9 shows the DC equivalent circuit with an external ramp circuit.

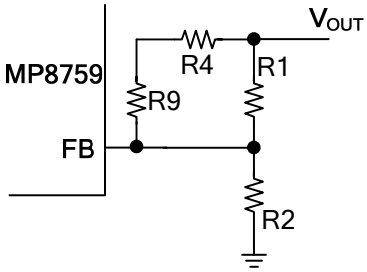

Figure 9: Equivalent DC Circuit

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Calculate R2 first, and then calculate R1 with Equation (6):

$$R_1=\frac{1}{\frac{V_{FB}}{R_2(V_{OUT}-V_{FB})}-\frac{1}{R_4+R_9}} \quad (6)$$

Usually, R9 is set to 499Ω. It should be five times smaller than R1//R2 to minimize its influence on V_{ramp}. R9 can also be set for better noise immunity with Equation (7):

$$R_9=\frac{1}{2\pi\times C_4\times 2F_{SW}} \quad (7)$$

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	R4 (kΩ)	C5 (pF)
1	48.7	66.5	0.68	499	220
1.2	52.3	47	0.95	499	220
1.5	82.5	47	0.95	499	220
1.8	115	47	0.95	499	220
2.5	43.2	12.7	1.2	499	330
3.3	43	9.63	1.5	NS	NS
5	41.2	5.6	1.5	NS	NS

Selecting the Inductor

The inductor is necessary for supplying a constant current to the output load while being driven by the switched input voltage. An inductor with a larger value results in less ripple current and lower output ripple voltage. However, it also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current to ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (8):

$$L=\frac{V_{OUT}}{F_{SW}\times\Delta I_L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (9):

$$I_{LP}=I_{OUT}+\frac{V_{OUT}}{2F_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors placed as close to VIN as possible for best performance. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (10):

$$I_{CIN}=I_{OUT}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})} \quad (10)$$

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, shown in Equation (11):

$$I_{CIN}=\frac{I_{OUT}}{2} \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (12):

$$\Delta V_{IN}=\frac{I_{OUT}}{F_{SW}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Under worst-case conditions where V_{IN} = $2V_{OUT}$, use Equation (13):

$$\Delta V_{IN}=\frac{1}{4}\times\frac{I_{OUT}}{F_{SW}\times C_{IN}} \quad (13)$$

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Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POS capacitors are recommended. The output voltage ripple can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (14)$$

With ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

In the case of POS capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be approximated with Equation (16):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (16)$$

The maximum output capacitor limitation should be also considered during the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitor value (C_{o_MAX}) can be limited approximately with Equation (17):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (17)$$

Where I_{LIM_AVG} is the average start-up current during soft-start period, and T_{ss} is the soft-start time. The inductance value can be calculated with Equation (18):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (18)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, including short currents. I_{sat} is recommended to be greater than 12A.

PCB Layout Guidelines

Efficient PBC layout is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 10 and follow the guidelines below.

1. Place the high current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitors as close to IN and GND as possible.
3. Place the decoupling capacitor as close to VCC and GND as possible.
4. Keep the switching node SW short and away from the feedback network.
5. Keep the BST voltage path as short as possible with traces greater than 50mil.
6. Keep the IN and GND pads connected with large copper traces to achieve better thermal performance.
7. Add several vias with 10mil_drill/18mil_copper_width close to the IN and GND pads to help with thermal dissipation.

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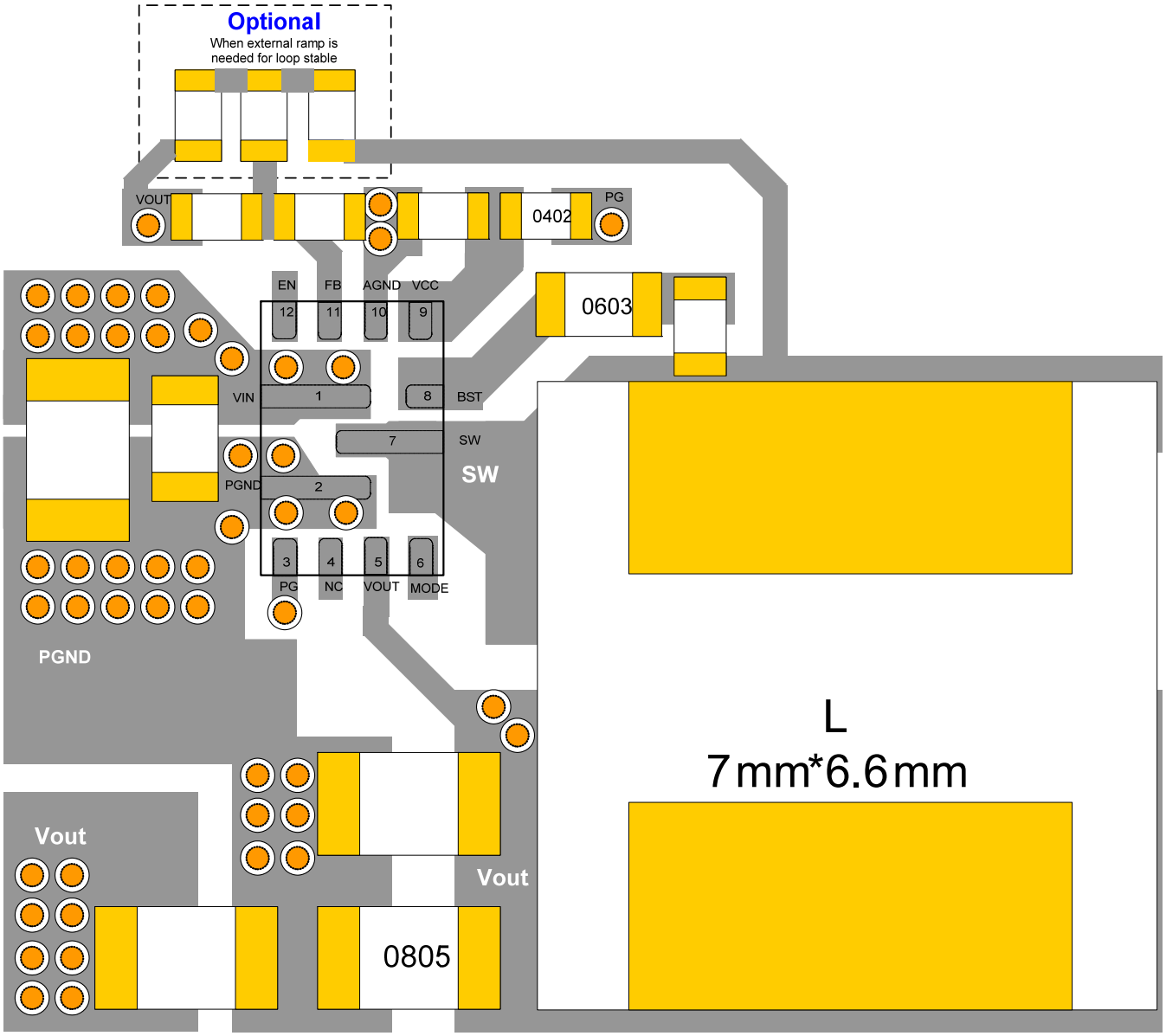

Figure 10: Recommend Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	1V
I_{OUT}	8A

The detailed application schematic for the 1V V_{OUT} is shown in Figure 17. The typical performance and waveforms are shown in the Typical Characteristics section. For more device applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

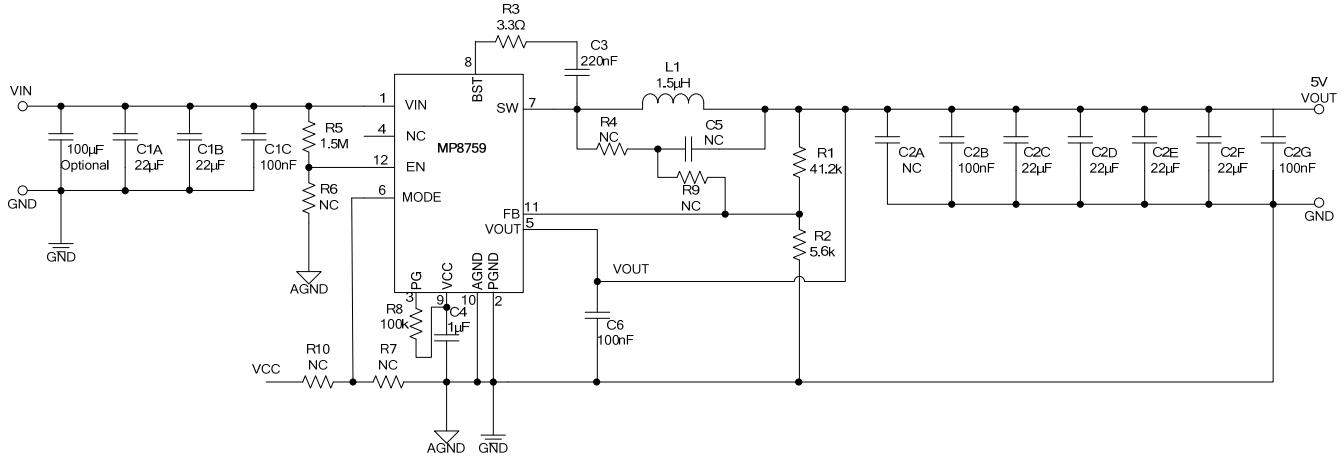

Figure 11: VIN = 12V[6], Vo = 5V, Io = 8A Application Schematic with Ceramic Output Capacitors

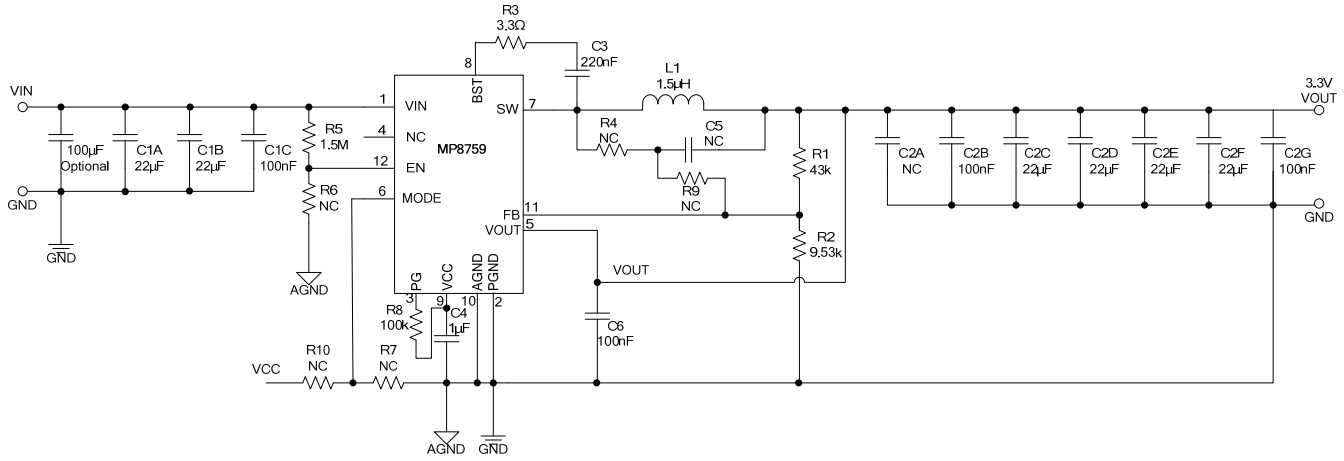

Figure 12: VIN = 12V[6], Vo = 3.3V, Io = 8A Application Schematic with Ceramic Output Capacitors

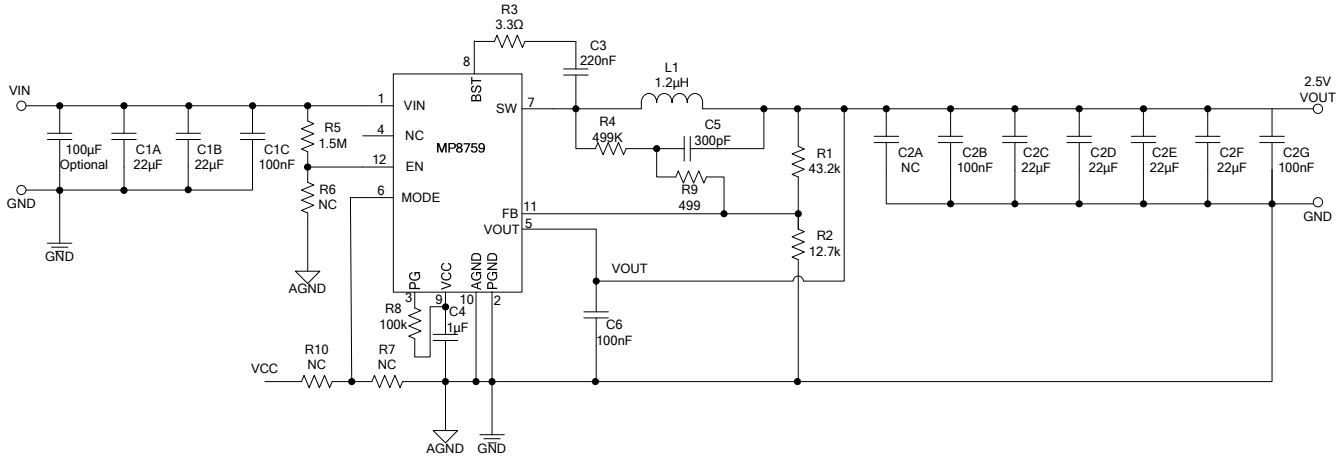

Figure 13: VIN = 12V [6], Vo = 2.5V, Io = 8A Application Schematic with Ceramic Output Capacitors

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TYPICAL APPLICATION CIRCUITS *(continued)*

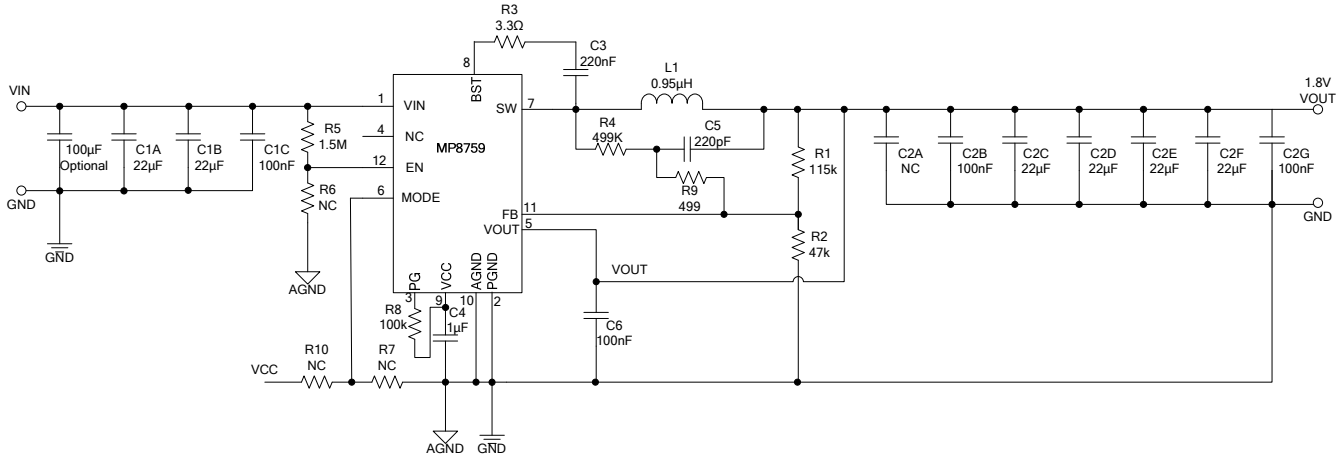

Figure 14: VIN = 12V[6], Vo = 1.8V, Io = 8A Application Schematic with Ceramic Output Capacitors

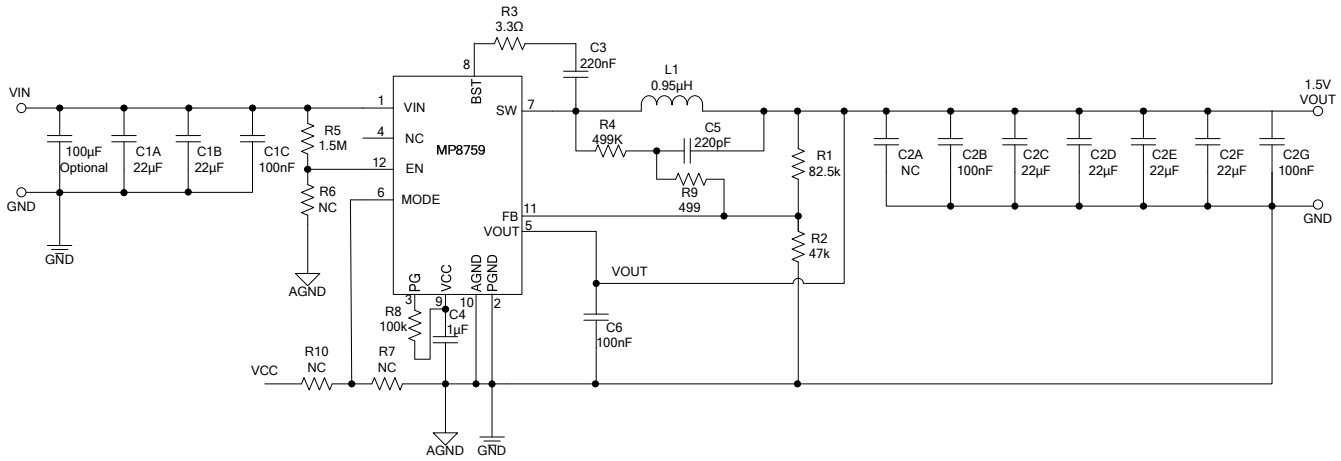

Figure 15: VIN = 12V [6], Vo = 1.5V, Io = 8A Application Schematic with Ceramic Output Capacitors

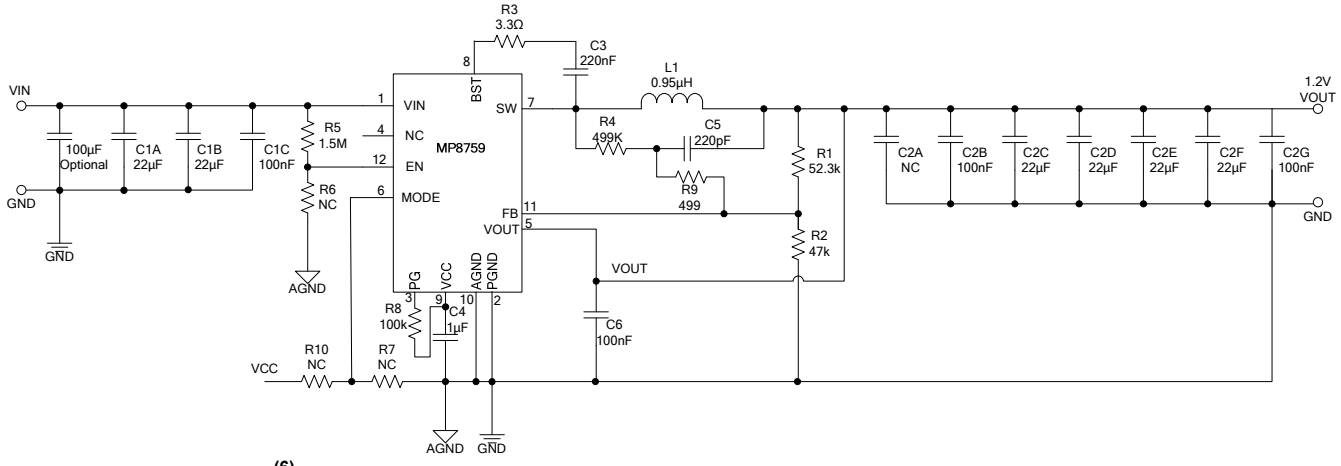

Figure 16: VIN = 12V[6], Vo = 1.2V, Io = 8A Application Schematic with Ceramic Output Capacitors

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TYPICAL APPLICATION CIRCUITS *(continued)*

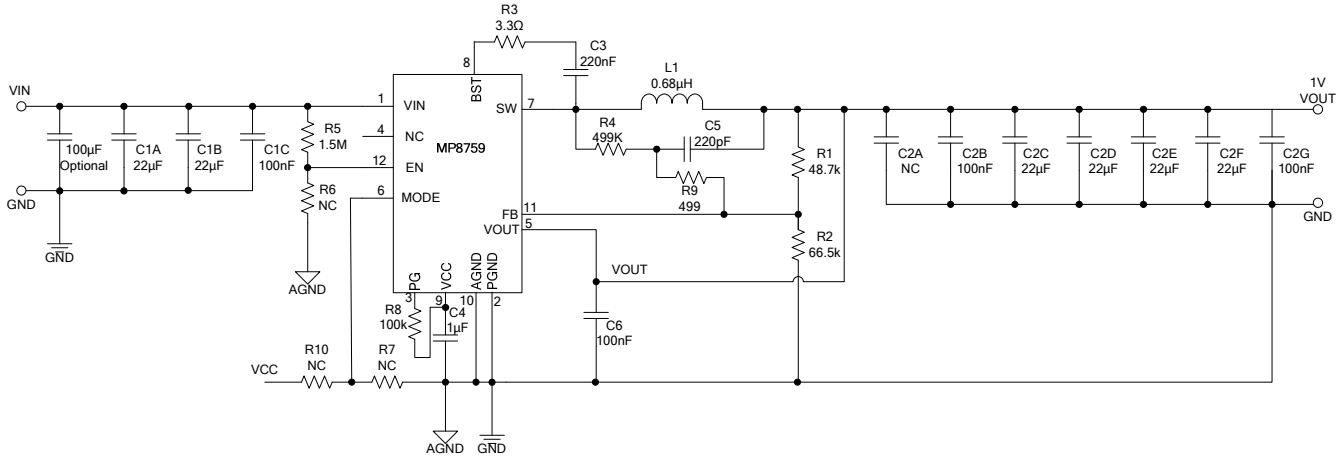

Figure 17: VIN = 12V[(6)], Vo = 1.0V, Io = 8A Application Schematic with Ceramic Output Capacitors

NOTE:

6) The EN resistor divider value should be modified accordingly with different input voltages. Please refer to the UVLO Protection section for details.

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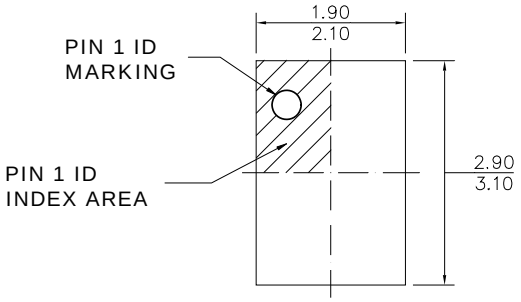
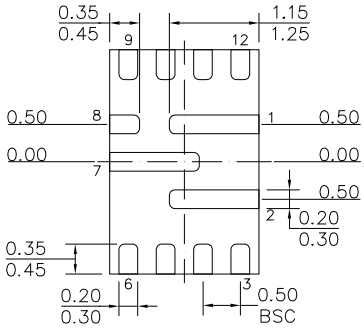
PACKAGE INFORMATION

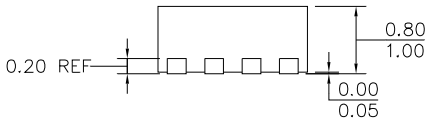
QFN-12 (2mmx3mm)



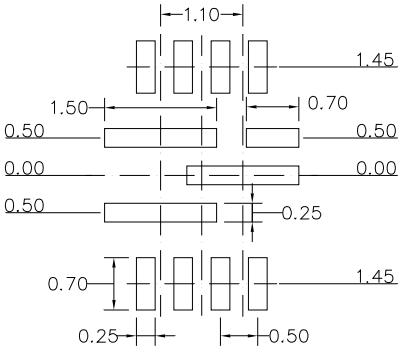
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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