Littelfuse®

Expertise Applied | Answers Delivered

LF2388B

3-Phase Half Bridge Gate Driver

Features

- Three floating high-side drivers in bootstrap operation to 600V
- 420mA source / 750mA sink output current capability
- Logic input 3.3V capability
- Internal deadtime of 315ns to protect MOSFETs
- Matched propagation delay time of 50ns maximum
- Outputs in phase with inputs
- Schmitt triggered logic inputs
- Cross conduction prevention logic
- Under Voltage Lockout (UVLO) for all channels
- Extended temperature range: -40°C to +125°C
- Space saving SOIC-20 package

Applications

- 3-Phase Motor Inverter Driver
- White Goods - Air Conditioner, Washing Machine, Refrigerator
- Industrial Motor Inverter - Power Tools, Robotics
- General Purpose 3-Phase Inverter



SOIC-20

Description

The LF2388B is a three-phase gate driver IC designed for high voltage three-phase applications, driving N-channel MOSFETs and IGBTs in a half-bridge configuration. The high voltage technology enables LF2388B high sides to switch to 600V in a bootstrap operation.

LF2388B logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

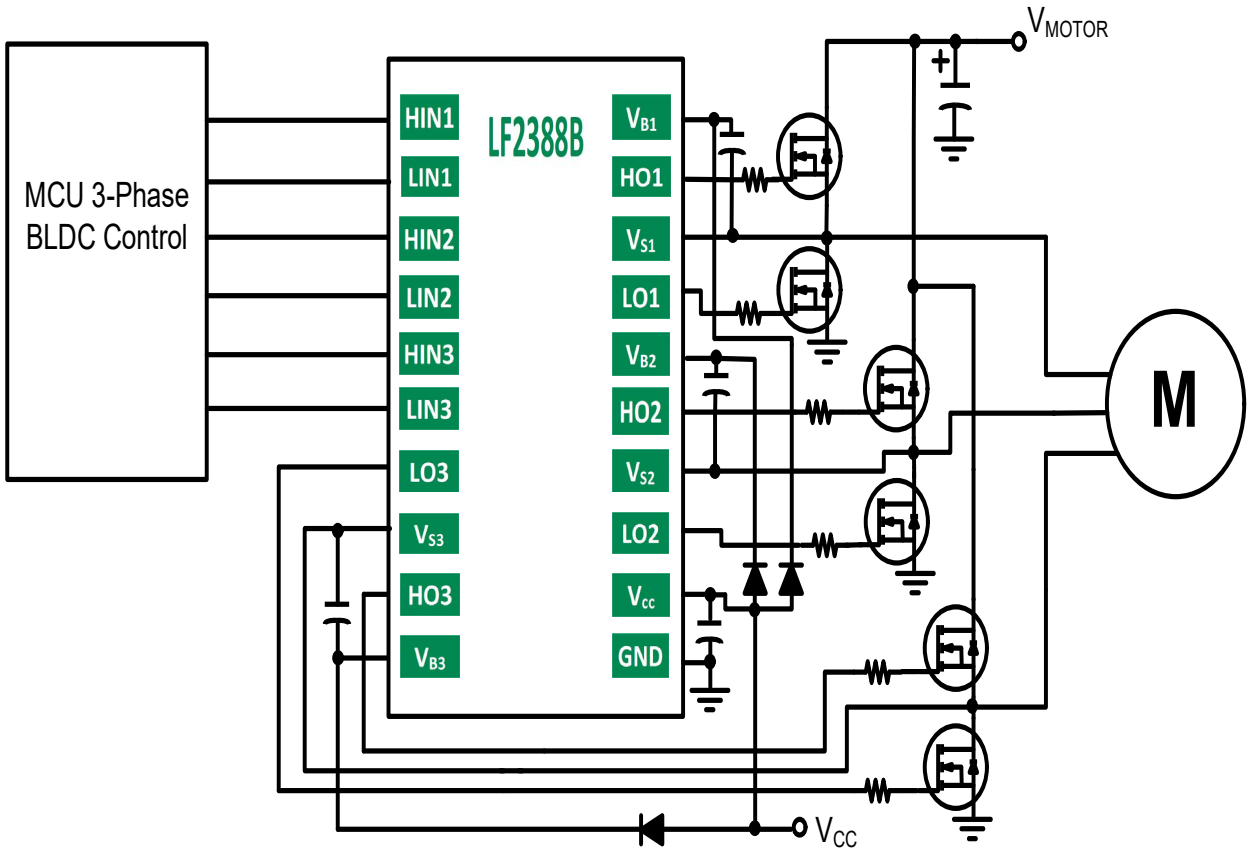
LF2388B offers numerous protection functions. A shoot-through protection logic prevents both outputs being high with both inputs high (fault state), an undervoltage lockout for V_{CC} shuts down all drivers through an internal fault control, and a UVLO for V_{BS} shuts down the respective high side output. LF2388B is offered in SOIC 20 package and operates over the extended temperature range of -40 °C to +125 °C .

Ordering Information

Year Year Week Week

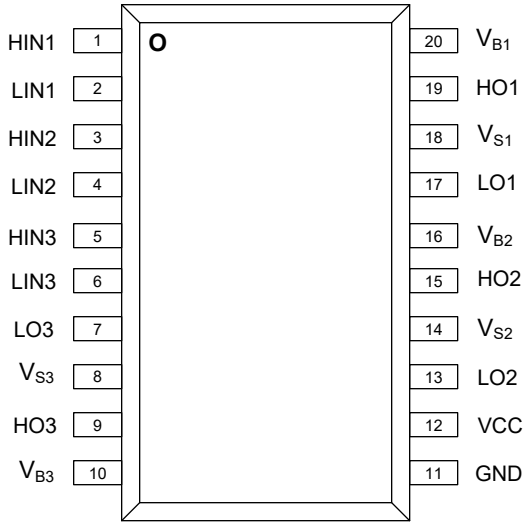
Part#	Package	Pack / Qty	Mark
LF2388BTR	SOIC-20	T&R / 1500	YYWW LF2388B LOT ID

Typical Application



1 Specifications

1.1 Pin Diagrams



Top View: SOIC-20

1.2 Pin Descriptions

Pin#	Pin Name	Pin Type	Pin Description
1, 3, 5	HIN1, HIN2, HIN3	Input	Logic input for high-side gate driver output, in phase with HO.
2, 4, 6	LIN1, LIN2, LIN3	Input	Logic input for low-side gate driver output, in phase with LO.
7, 13, 17	LO3, LO2, LO1	Output	Low-side gate driver output
8, 14, 18	V_{S3},V_{S2},V_{S1}	Power	High-side floating supply return
9, 15, 19	HO3, HO2, HO1	Output	High-side gate driver output
10, 16, 20	V_{B3},V_{B2},V_{B1}	Power	High-side floating supply
11	GND	Power	Low-side driver and logic return
12	V_{CC}	Power	Low-side and logic fixed supply

1.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
High side floating supply voltage	V_B	-0.3	+624	V
High side floating supply offset voltage	V_S	V_B-24	V_B+0.3	V
High side floating output voltage	V_{HO}	V_S-0.3	V_B+0.3	V
Low side output voltage	V_{LO}	-0.3	V_{CC}+0.3	V
Offset supply voltage transient	dV_S/dt	--	50	V/ns
Low side fixed supply voltage	V_{CC}	-0.3	+24	V
Logic input voltage (HINx and LINx)	V_{IN}	-0.3	5.5	V
Package power dissipation	P_D	--	1.47	W
Junction Operating Temperature	T_J	--	+150	°C
Storage Temperature	T_{STG}	-55	+150	° C

Unless otherwise specified all voltages are referenced to GND . All electrical ratings are at T_A= 25 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.4 Thermal Characteristics

Parameter	Symbol	Rating	Unit
Junction to ambient	$\emptyset_{JA}$	85	°C/W

When mounted on a standard JEDEC 2-layer FR-4 board - JESD51-3

1.5 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High side floating supply absolute voltage	V_B	V_S + 10	V_S + 20	V
High side floating supply offset voltage	V_S	***NOTE1***	600	V
High side floating output voltage	V_{HO}	V_S	V_B	V
Low side fixed supply voltage	V_{CC}	10	20	V
Low side output voltage	V_{LO}	0	V_{CC}	V
Logic input voltage (HINx and LINx)	V_{IN}	0	5	V
Ambient temperature	T_A	-40	125	°C

Unless otherwise specified all voltages are referenced to GND

NOTE1 *High-side driver remains operational for V_S transients down to -5V*

1.6 DC Electrical Characteristics

V_{CC}= V_{BS}=15V, T_A = 25 °C and V_{GND} = 0V , unless otherwise specified.

The V_{IN} and I_{IN} parameters are referenced to GND and are applicable to all six channels (HIN1,2,3 and LIN1,2,3). The V_O and I_O parameters are applicable to the outputs (HO1,2,3 and LO1,2,3 and are referenced to GND.

Parameter	Symbol	Conditions	Mln	Typ	Max	Unit
Logic "1" input voltage	V_{IH}	*NOTE2*	2.4	--	--	V
Logic "0 " input voltage	V_{IL}		--	--	0.8	
Logic input voltage hysteresis	$V_{IN(HYS)}$	--	--	0.9	--	
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O = 2mA	--	0.2	0.5	
Low level output voltage, V_O	V_{OL}	I_O = 2mA	--	0.07	0.2	
Offset supply leakage current	I_{LK}	VB = VS = 600V	--	--	10	µA
Quiescent V_{BS} supply current	I_{BSQ}	V_{IN} = 0V or 5V	--	50	80	
Operating V_{BS} supply current	I_{BSO}	fs = 20khz	--	400	--	
Quiescent V_{CC} supply current	I_{CCQ}	V_{IN} = 0V or 5V	--	230	330	
Operating V_{CC} supply current	I_{CCO}	fs = 20khz	--	500	--	
Logic "1" input bias current	I_{IN+}	V_{IN} = 5V	--	25	80	
Logic "0" input bias current	I_{IN-}	V_{IN} = 0V	--	--	2	
Input pull-down resistance	R_{IN}	--	--	200	--	kΩ
V_{CC}, V_{BS} UVLO off, positive going threshold	V_{UV+}	--	7.1	8.5	9.9	V
V_{CC}, V_{BS} UVLO enable, negative going threshold	V_{UV-}	--	6.7	8.1	9.5	
UVLO hysteresis	$V_{UV(HYS)}$	--	--	0.4	--	
Output high, short circuit pulsed current	I_{O+}	V_O = 0V, t ≤ 10 µs	270	420	--	mA
Output low, short circuit pulsed current	I_{O-}	V_O = 15V, t ≤ 10 µs	600	750	--	

NOTE2 *For optimal operation, it is recommended the input pulse (to HINx and LINx) MUST have a minimum amplitude of 2.4V with a minimum pulse width of 600ns.*

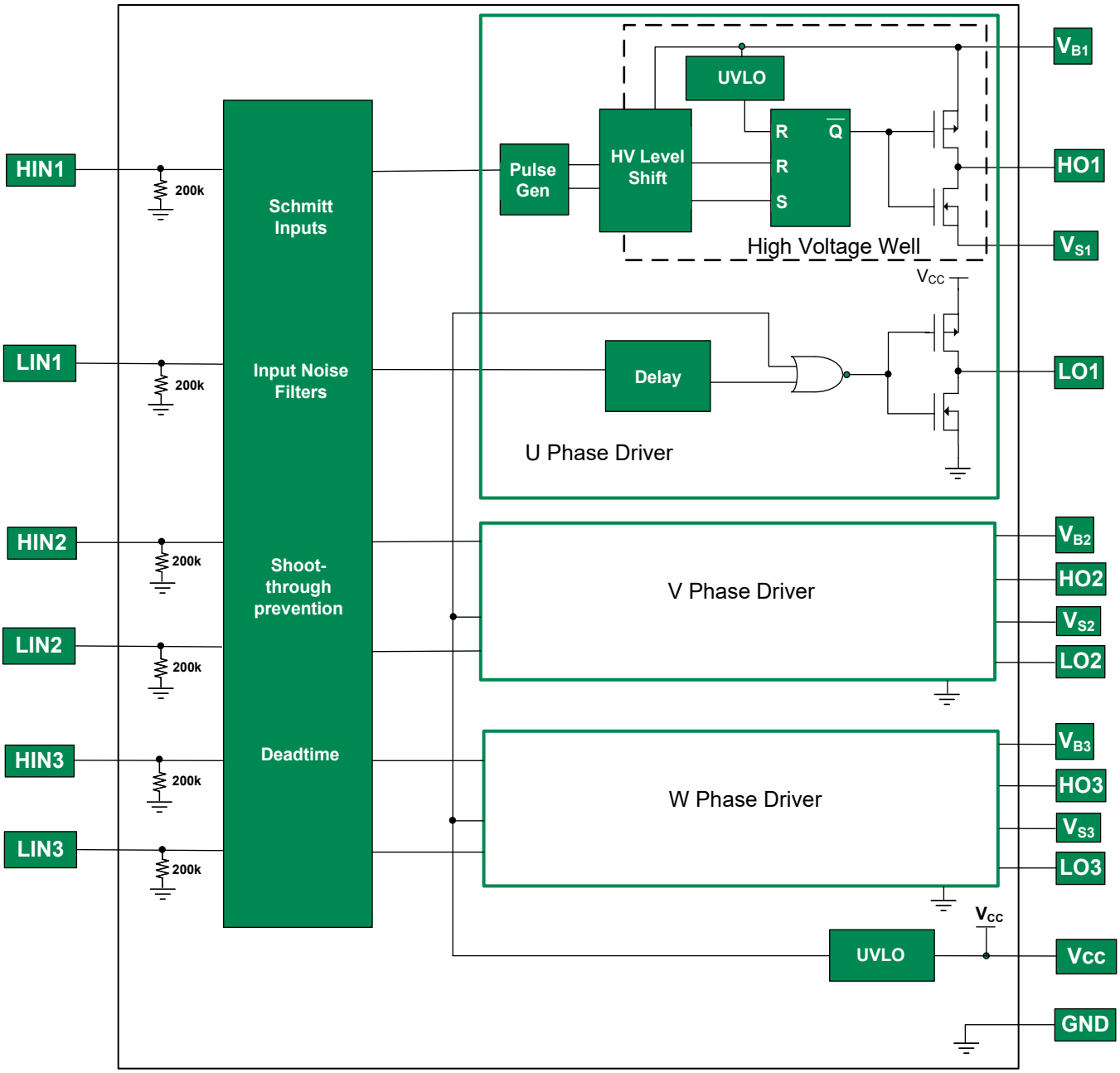
1.7 AC Electrical Characteristics

V_{CC}=V_{BS} = 15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on propogation delay	t_{on}	V_S = 0V	70	120	170	ns
Turn-off propogation delay	t_{off}	V_S = 0V	70	120	170	
Turn-on rise time	t_r	V_S = 0V	--	45	75	
Turn-off fall time	t_f		--	25	40	
Propagation delay matching	t_{DM}	--	--	--	50	
Deadtime	t_{DT}	--	200	315	430	
Deadtime matching	t_{DTM}	--	--	--	50	

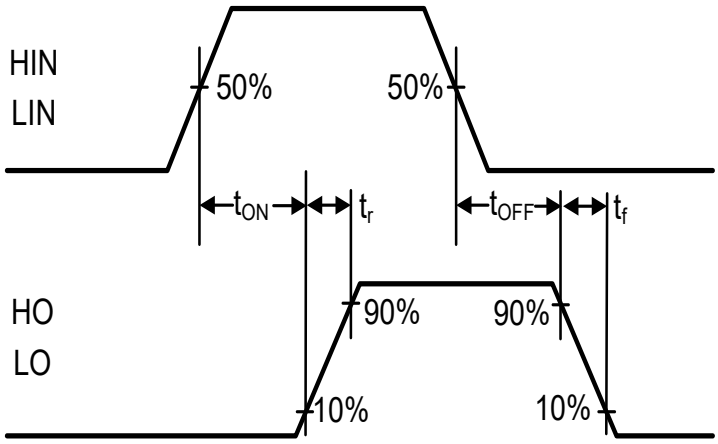
2 Functional Description

2.1 Functional Block Diagram



2.2 Timing Waveforms

Figure 1. Input-to-Output Delay Timing

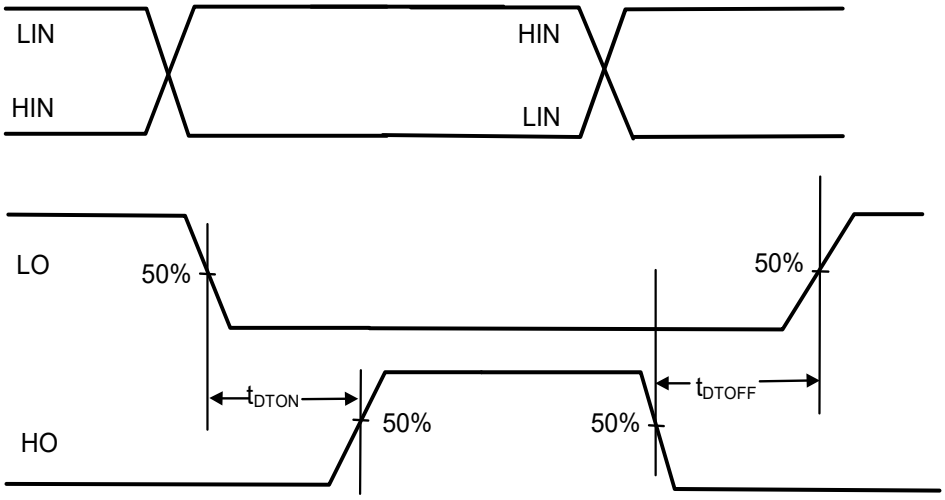


Delay Matching :

$t_{DM\ OFF} = |t_{OFF\ LO} - t_{OFF\ HO}|$

$t_{DM\ ON} = |t_{ON\ LO} - t_{ON\ HO}|$

Figure 2. Deadtime Waveform Dagram



Deadtime :

$t_{DT\ LO\text{-}HO} = t_{ON\ HO} - t_{OFF\ LO}$

$t_{DT\ HO\text{-}LO} = t_{ON\ LO} - t_{OFF\ HO}$

Deadtime Matching : $t_{DT\ MT} = |t_{DT\ LO\text{-}HO} - t_{DT\ HO\text{-}LO}|$

2.3 Application Information

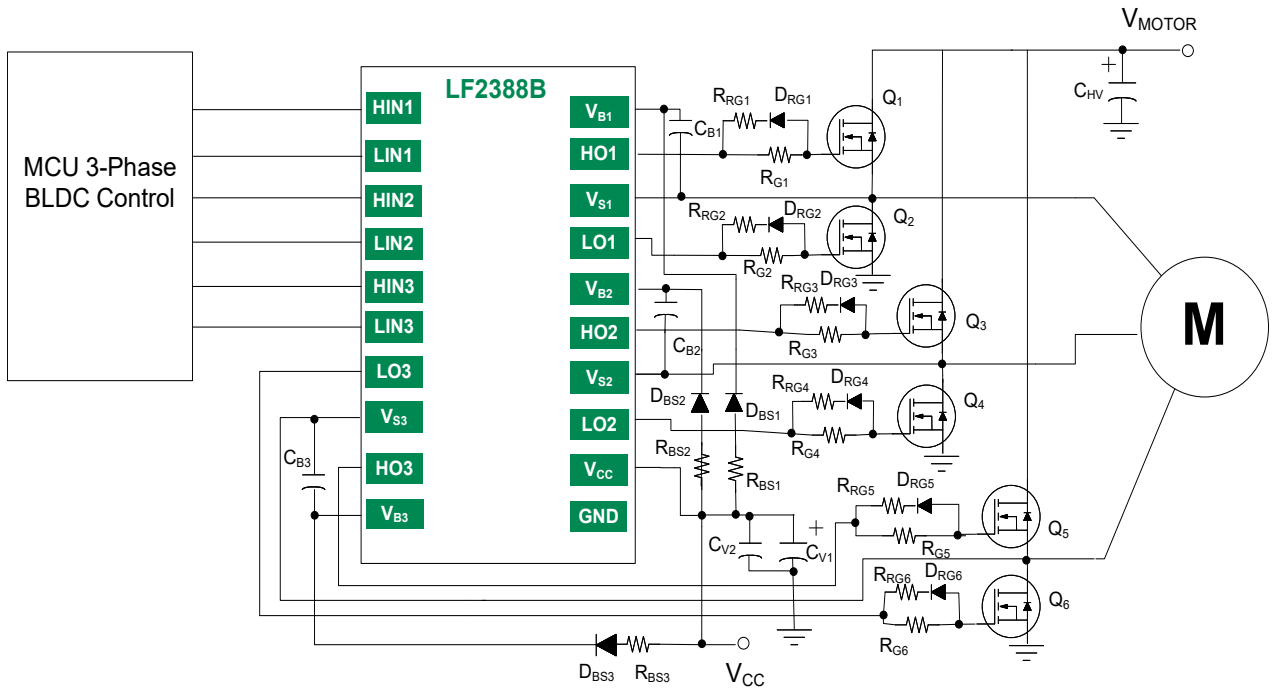


Figure 3. LF2388B in a 3 phase motor drive application.

- RRG1 - RRG6 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

- It is **highly recommended** that the input pulse (to HINx and LINx) should have a minimum amplitude of 2.4V and a minimum pulse width of 600ns.

- RG1 - RG6 values are typically between 20Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

- RBS1 - RBS3 values are typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DBS1 - DBS3 should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

3 Performance Data

Unless otherwise noted V_{CC}= V_{BS} =15V, T_A = 25 °C, V_{GND} = 0V and values are typical.

Figure 4. Turn On Propagation delay vs Supply Voltage

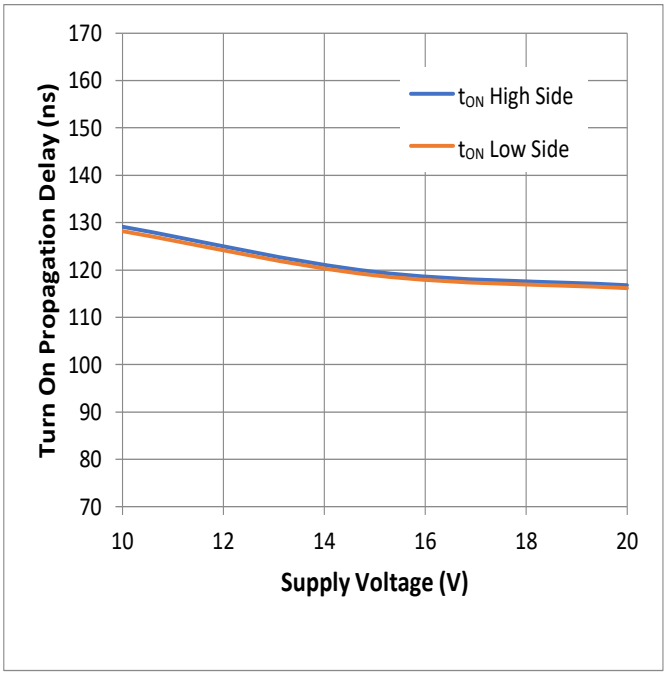


Figure 5. Turn On Propagation delay vs Temperature

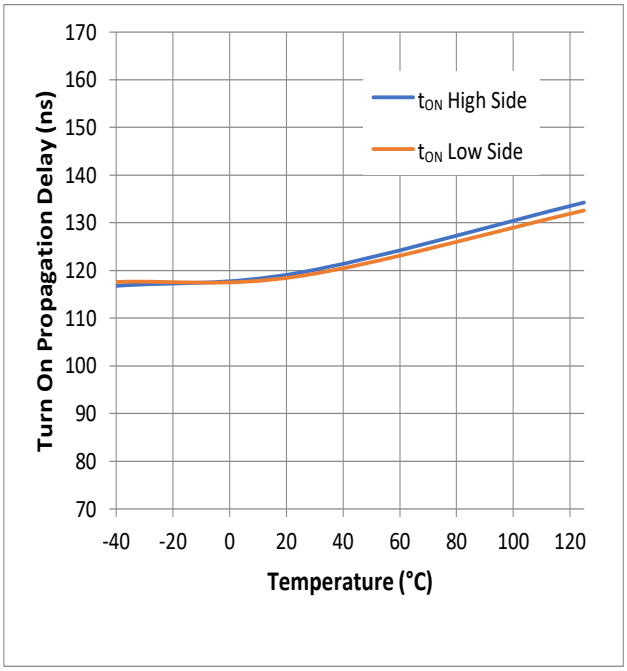


Figure 6. Turn Off Propagation delay vs Supply Voltage

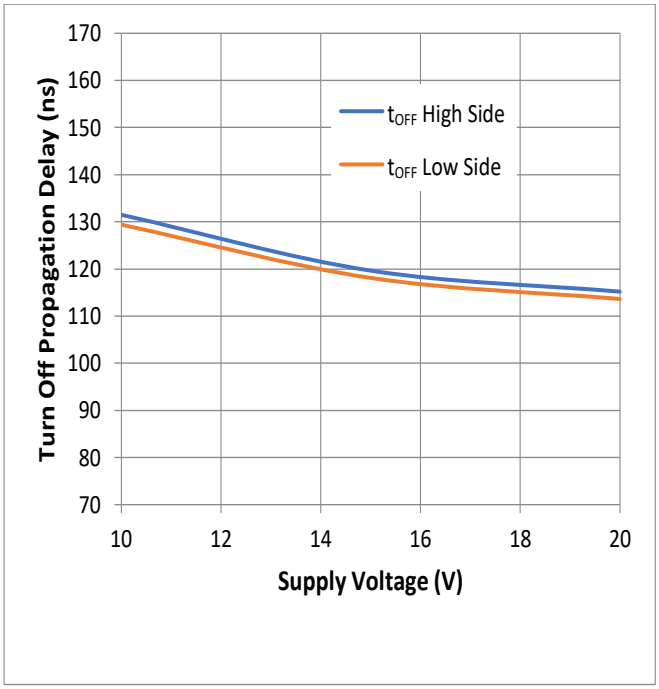


Figure 7. Turn Off Propagation delay vs Temperature

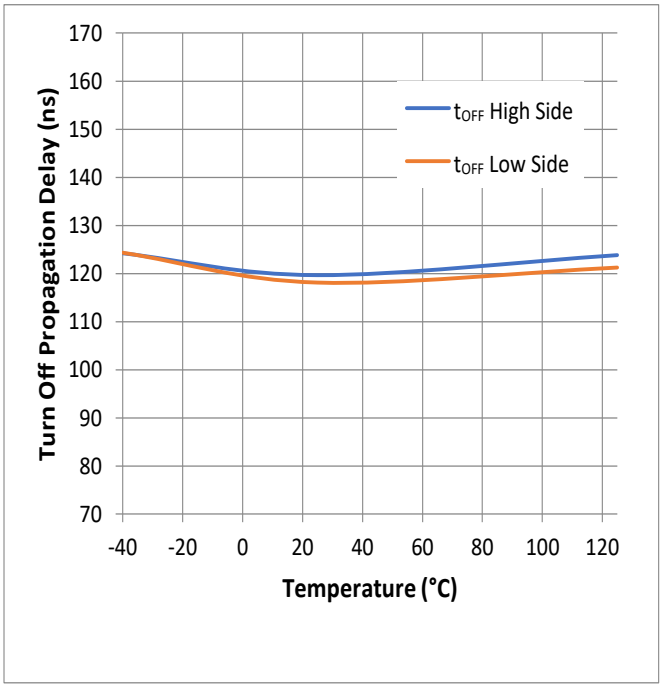


Figure 8. Rise time vs Supply voltage

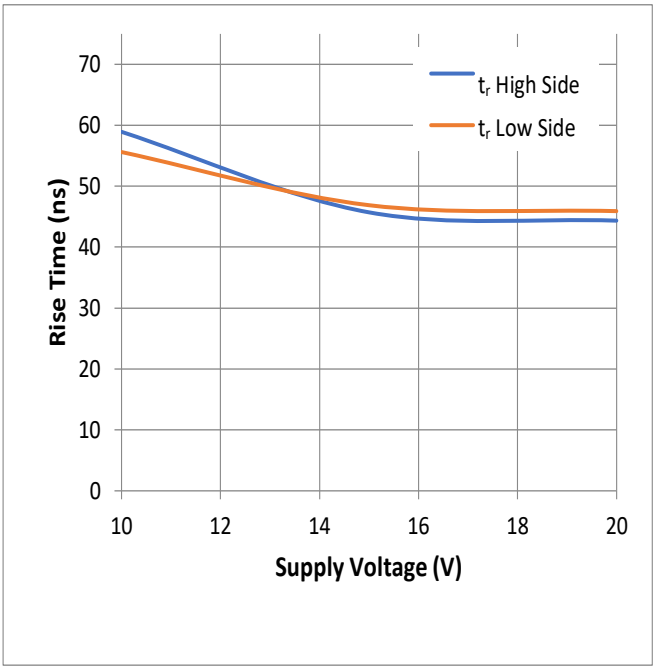


Figure 9. Rise time vs Temperature

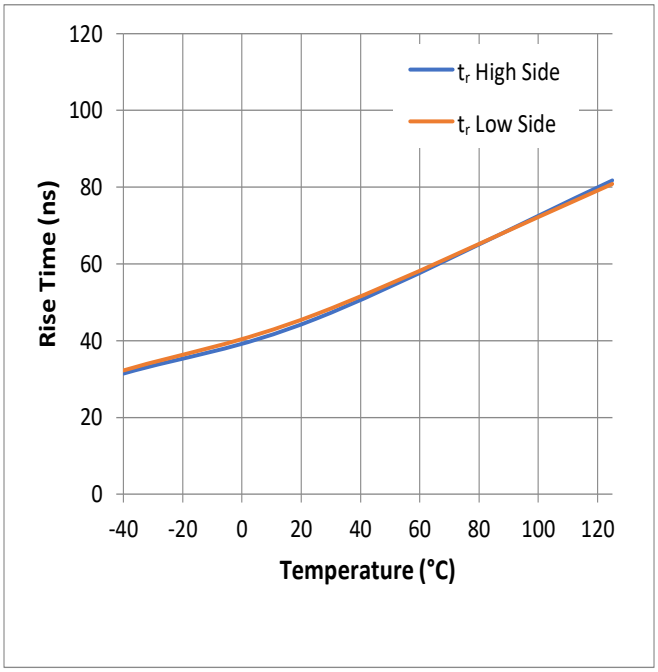


Figure 10. Fall time vs Supply voltage

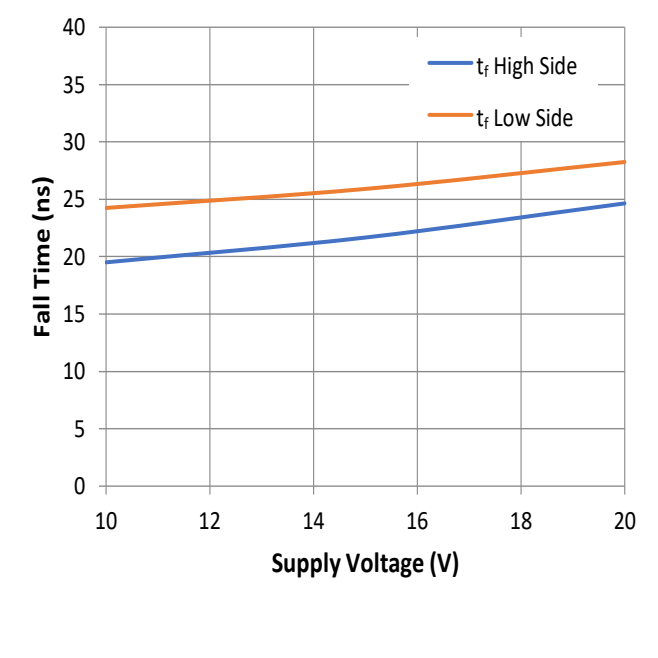


Figure 11. Fall time vs Temperature

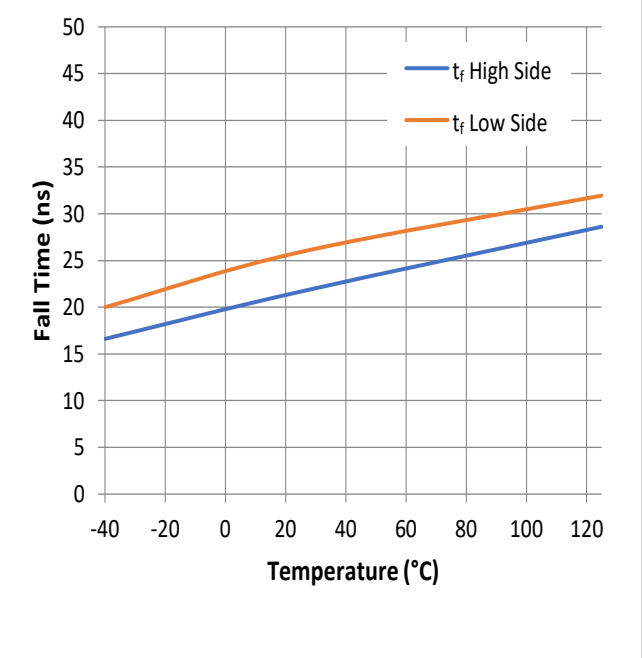


Figure 12. Quiescent current vs Supply voltage

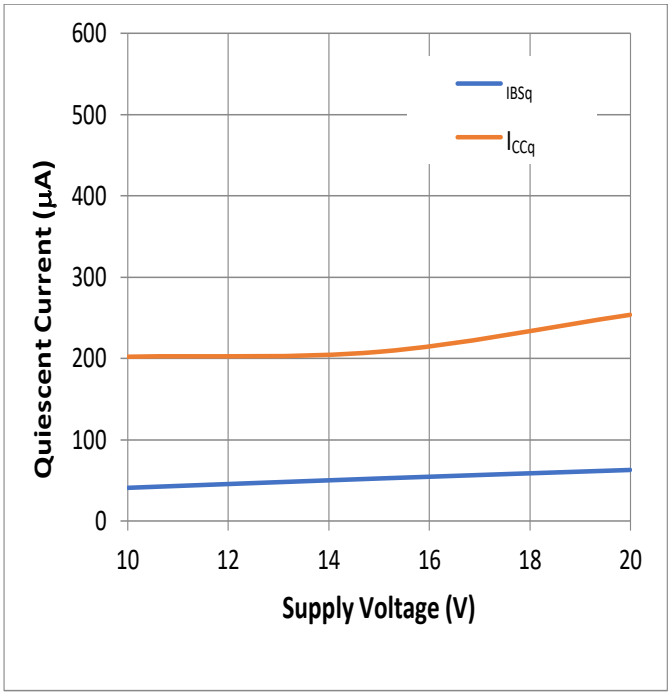


Figure 13. Quiescent current vs Temperature

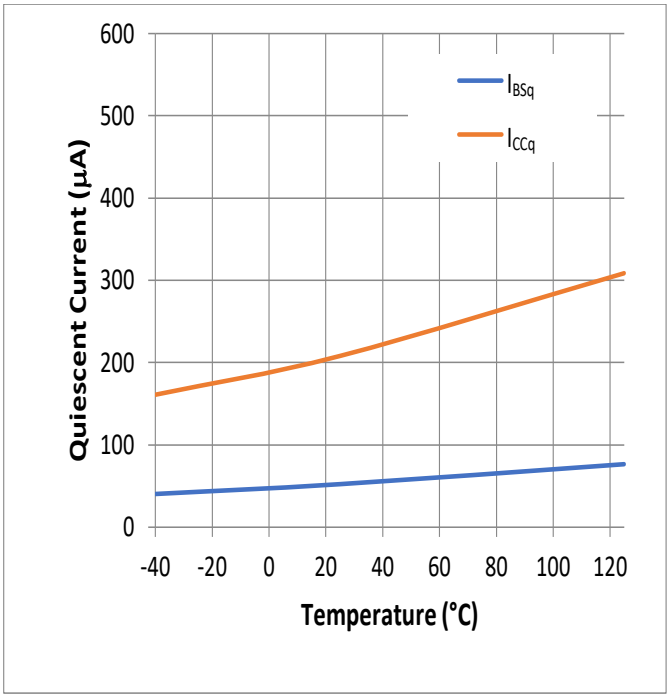


Figure 14. Delay Matching vs Supply voltage

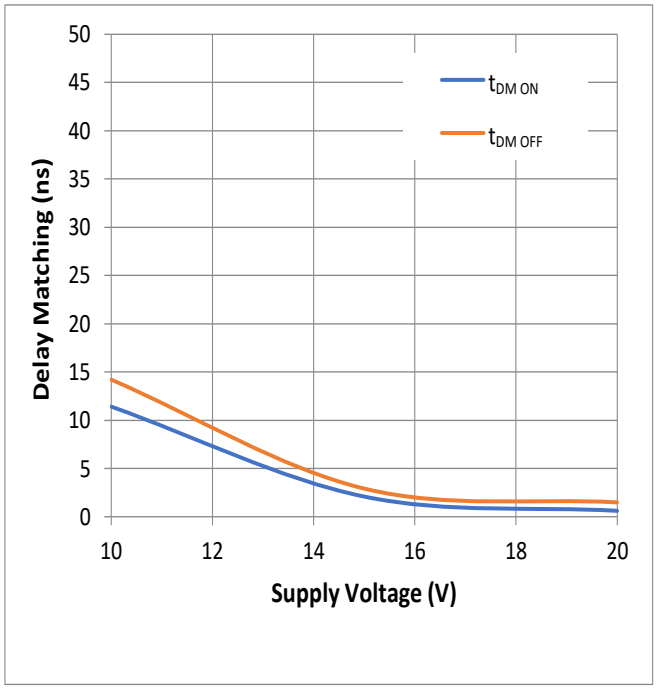


Figure 15. Delay Matching vs Temperature

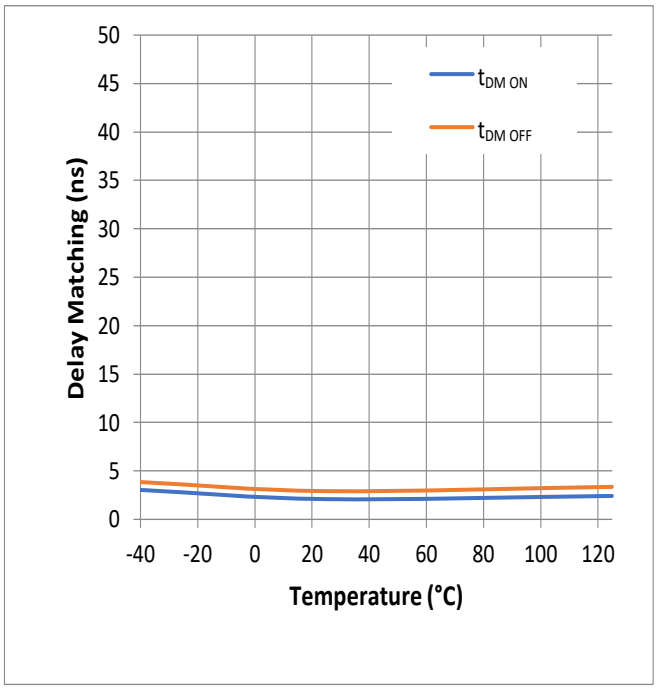


Figure 16. Source Current vs Supply voltage

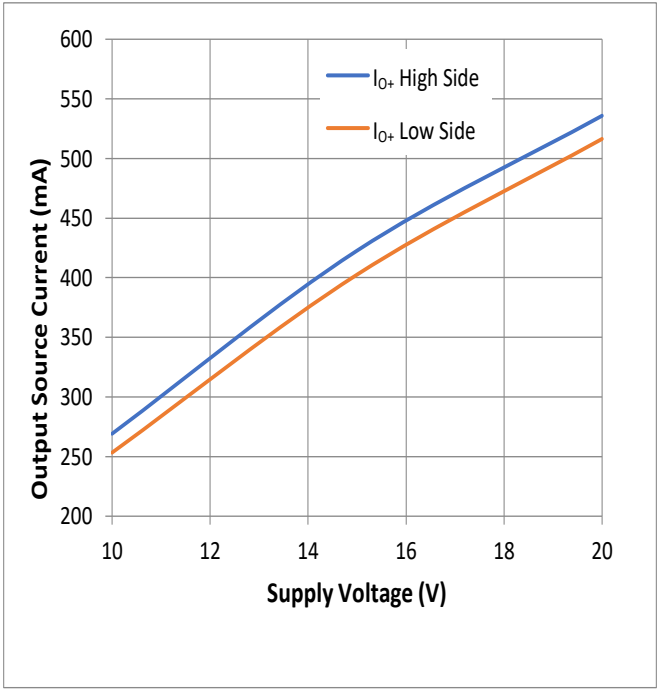


Figure 17. Source Current vs Temperature

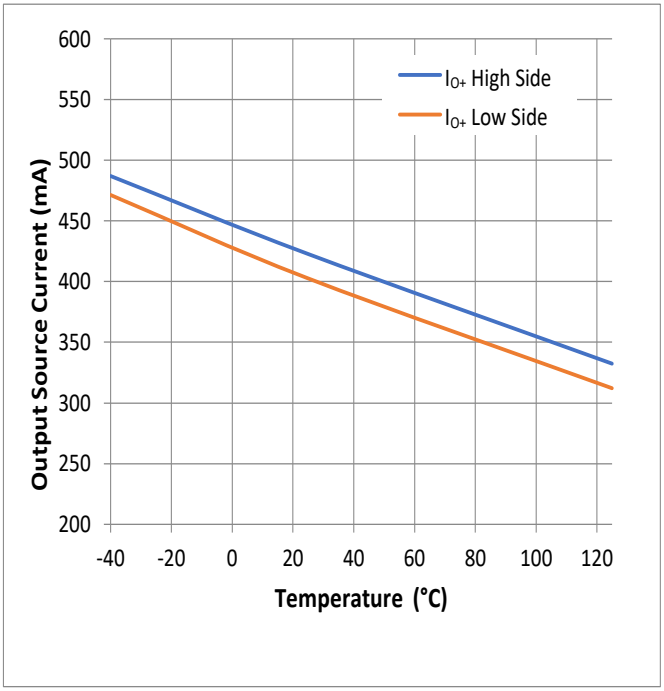


Figure 18. Sink Current vs Supply voltage

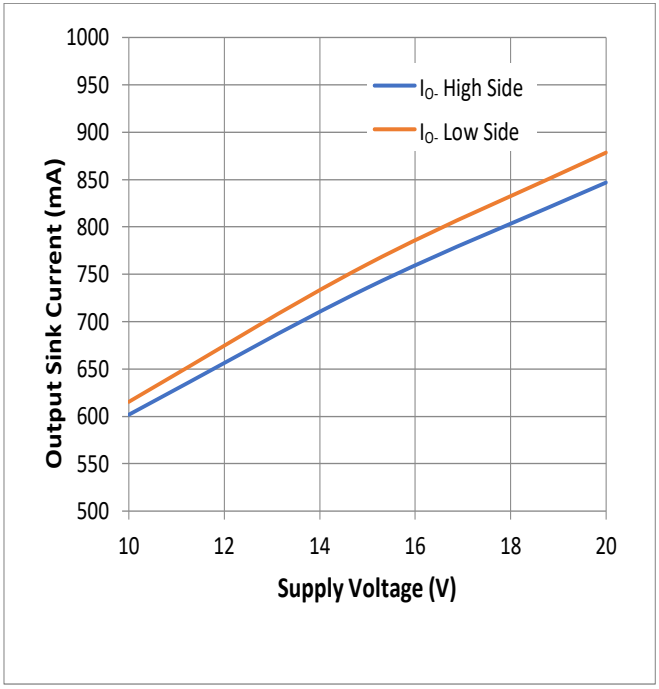


Figure 19. Sink Current vs Temperature

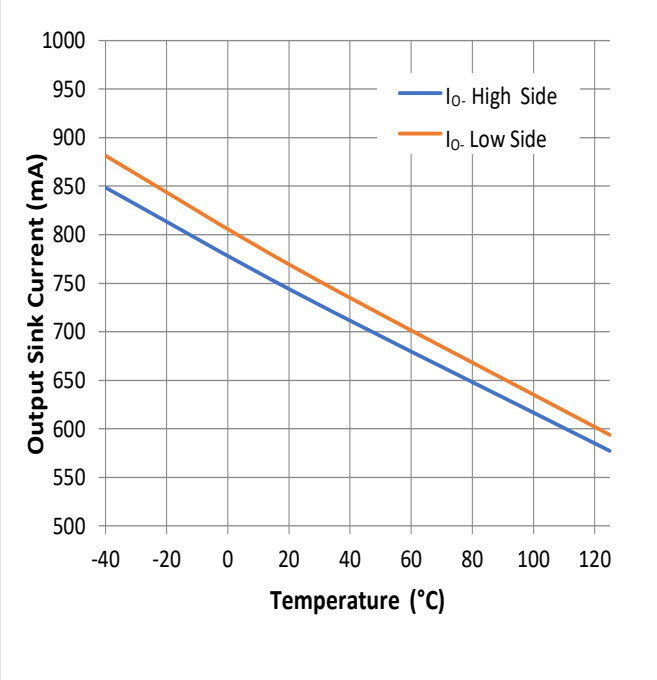


Figure 20 Logic 1 Input Voltage vs Supply voltage

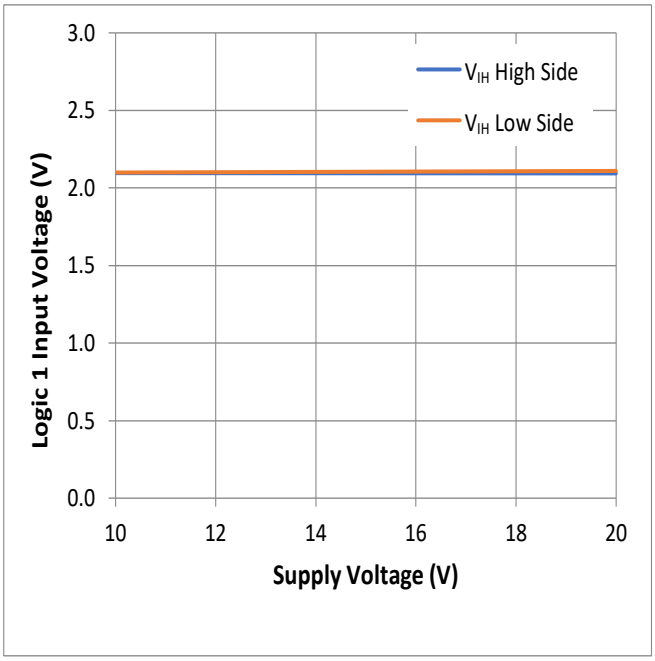


Figure 21. Logic 1 Input Voltage vs Temperature

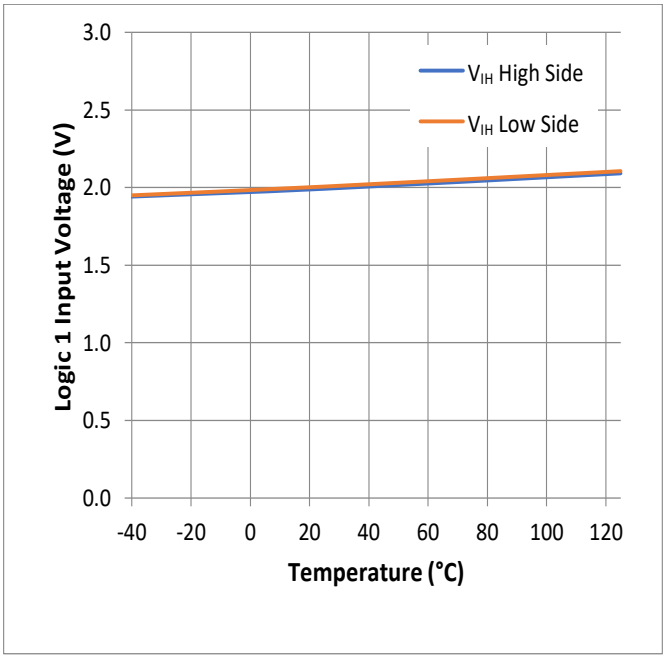


Figure 22. Logic 0 Input Voltage vs Supply voltage

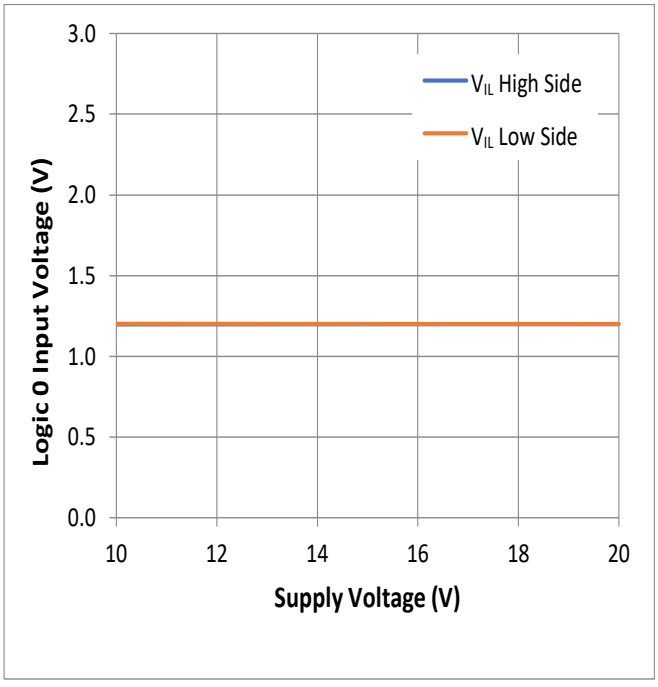


Figure 23. Logic 0 Input Voltage vs Supply voltage

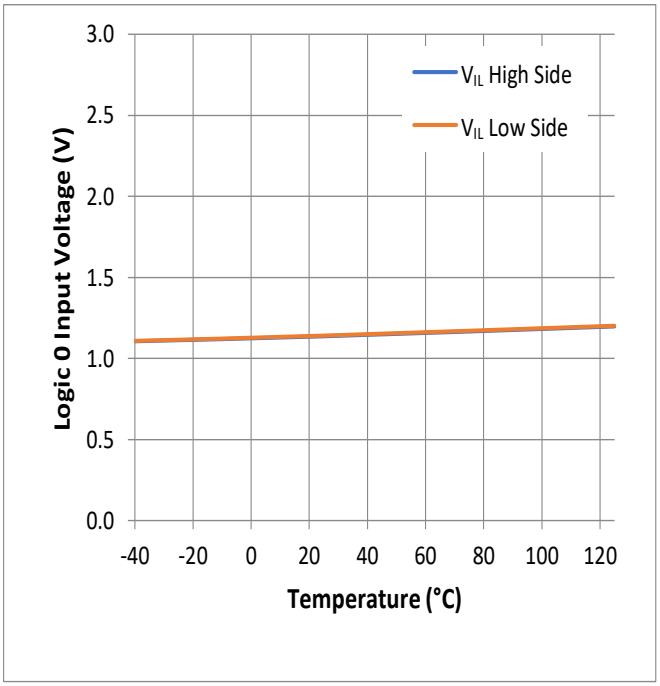


Figure 24. Deadtime vs Supply voltage

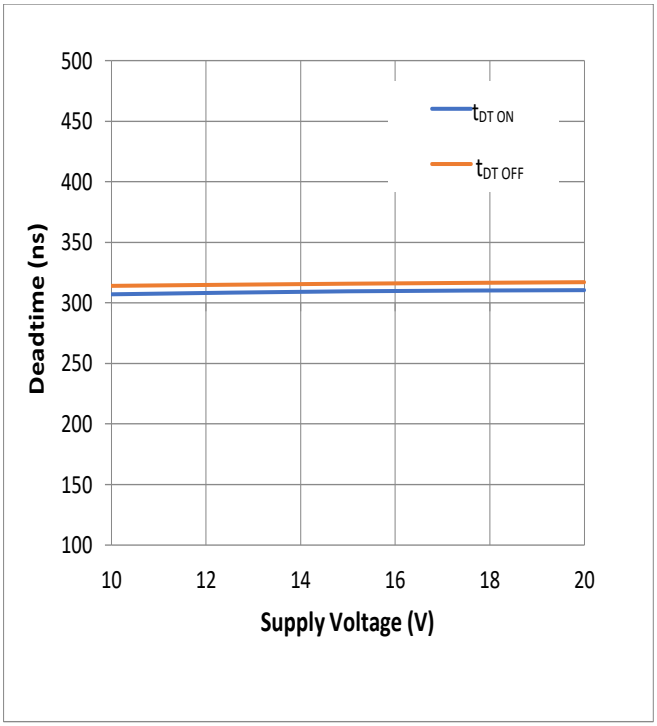


Figure 25. Deadtime vs Temperature

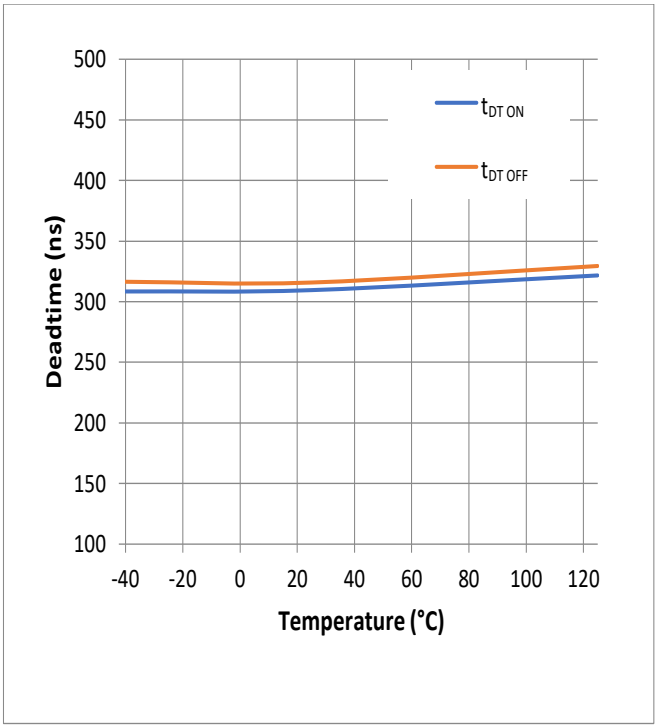


Figure 26. V_{CC} UVLO vs Temperature

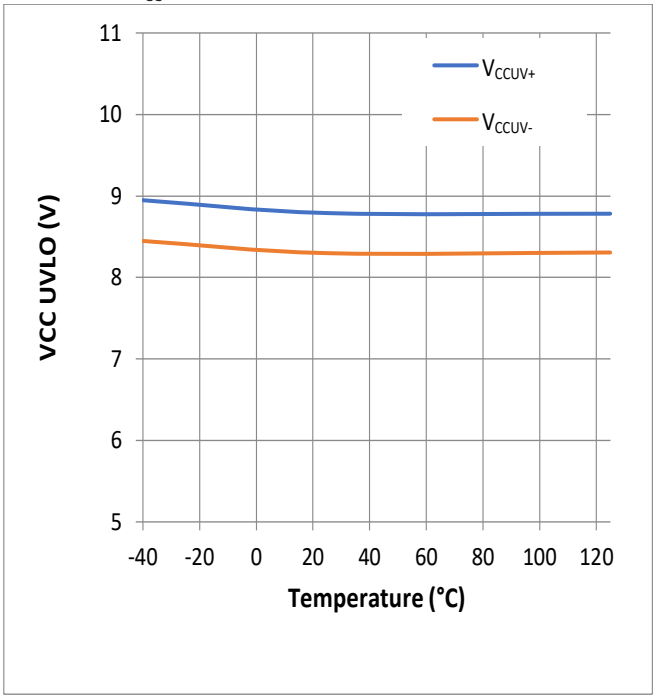


Figure 27. V_{BS} UVLO vs Temperature

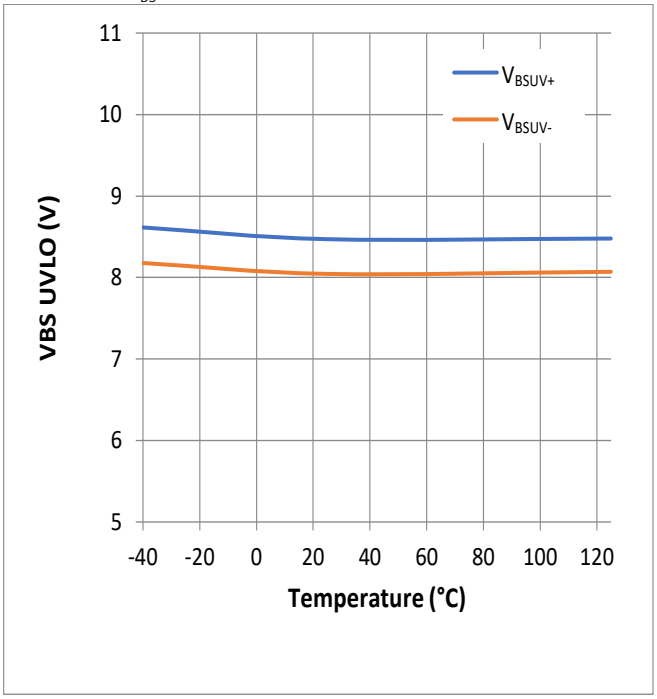
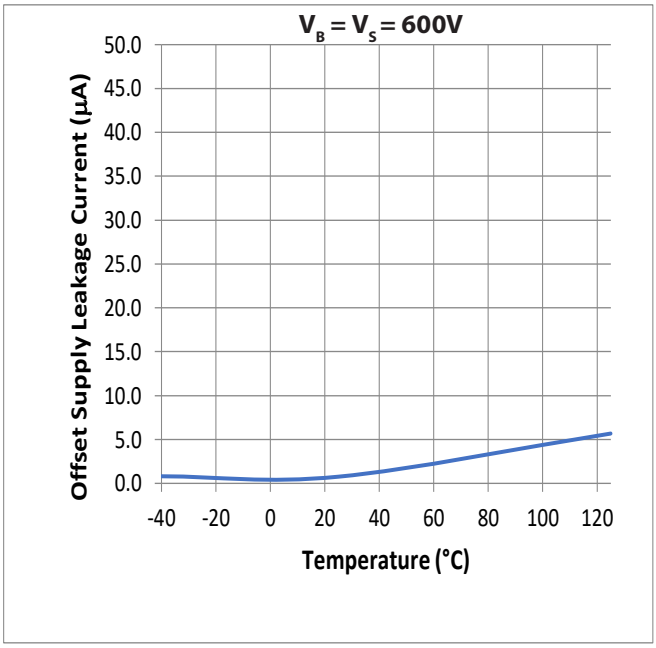


Figure 28. Offset Supply Leakage Current vs Temperature



4 Manufacturing Information

4.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** rating as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033.**

Device	Moisture Sensitivity Level (MSL) Classification
LF2388B	MSL3

4.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Reflow Profile

Provided in the table below is the IPC/JEDEC J-STD-020 Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

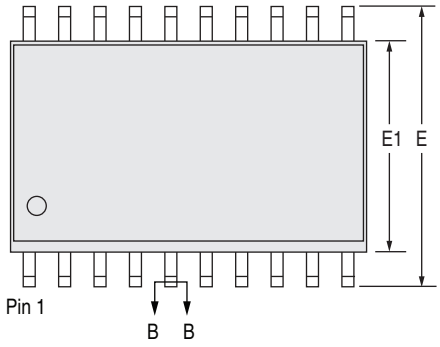
Device	Classification Temperature(Tc)	Dwell Time (tp)	Max Reflow Cycles
LF2388B	260°C	30 seconds	3

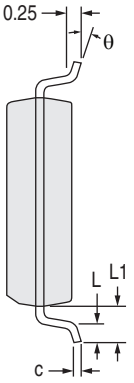


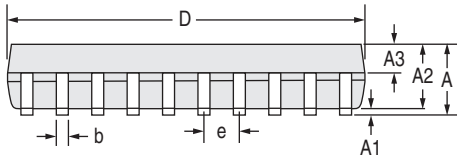
4.4 Board Wash

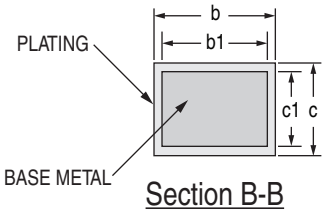
Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

5 Package Dimensions: SOIC-20





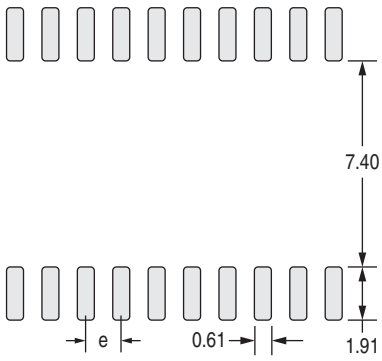




Section B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	-	0.43
b1	0.34	0.37	0.40
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 BSC		
L	0.70	-	1.00
L1	1.40 REF		
θ	0°	-	8°

PCB Land Pattern



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